PRODUCT SPECIFICATION

7.0” α -Si TFT LCD MODULE
MODEL: T070800128-A2WMN-002 Ver:1.0

ROHS

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER’S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2016.04.20	ZFY	Initial Release	

Table of Contents

1. General Description

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs, and a backlight unit.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	7.0”	
LCD type	α-Si TFT	
Display Mode	Transmissive /normally black	
Resolution	800 RGB x 1280	Pixels
View Direction	FULL VIEW	Best Image
POL surface	Anti-glare	
Module Outline	103.46(H) x162.03 (V) x 2.30(T) (Note1)	mm
Active Area	94.2(H) x150.72(V)	mm
Pixel Size	117.75(H)x117.75(V)	um
Pixel Arrangement	R.G.B. Stripe	
Display Colors	16.7M	
Interface	MIPI	
With or Without TP	Without	
Operating Temperature	**-10~50**	ºC
Storage Temperature	**-20~60**	ºC
Weight	TBD	g

Note 1: Exclusive hooks, posts , FFC/FPC tail etc.

3. Absolute Maximum Ratings

V_{SS}=0V, Ta=25ºC

Item	Symbol	Min.	Max.	Unit
Power voltage	VDDIN	-0.3	5.5	V
	AVDD	-0.3	6.6	V
	AVEE	+0.3	-6.6	V
Storage temperature	T_{stg}	**-20**	**+60**	ºC
Operating temperature	T_{op}	**-10**	**+50**	ºC

Note 1: If Ta below 50ºC, the maximal humidity is 90%RH, if Ta over 50ºC, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Power voltage	VDDIN	3.0	3.3	3.6	V
	I(vddin)		(35)		mA
	AVDD	5.2	(5.8)	6.0	V
	I(avdd)		(35)		mA
	AVEE	-6.0	(-5.8)	-5.2	V
	I(avee)		(30)		mA
Input logic high voltage	V_{IH}	0.7*VDDIN	-	VDDIN	V
Input logic low voltage	V_{IL}	0	-	0.3VDDIN	V
Panel power consumption		-	0.4	-	W

Note: Typical Vcom is only a reference value. It must be optimized according to each LCM. Be sure to use VR.

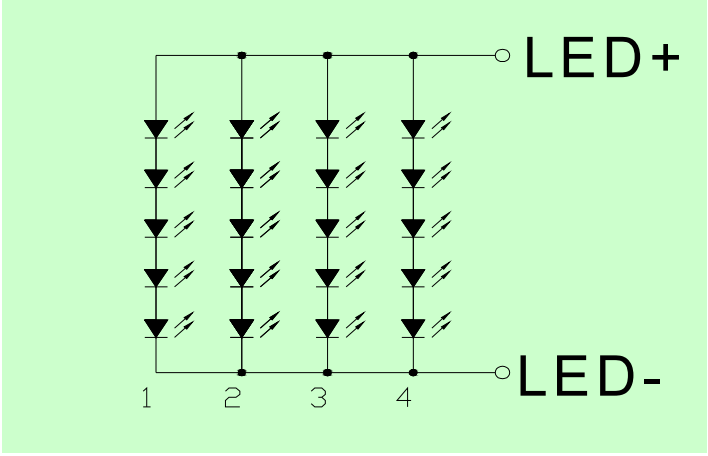
5. Backlight Characteristic

5.1. Backlight Characteristic

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Voltage	V_F	Ta=25 ºC, I_F=20mA/LED	14	16	17.5	V
Forward Current	I_F	Ta=25 ºC, V_F=3.1V/LED	-	80	-	mA
Power dissipation	Pd		-	1280	-	W
Uniformity	Avg		70	75	-	%
LED working life(25℃)	-		-	20000	-	hours
Drive method	Constant current					
LED Configuration	20 White LEDs(5 LEDs in one string and 4 groups in parallel)					

Note1：LED life time defined as follows: The final brightness is at 50% of original brightness.
The environmental conducted under ambient air flow, at Ta=25±2 ºC,60%RH±5%, I_F=20mA.

5.2. Backlighting circuit



6. ptical Characteristics

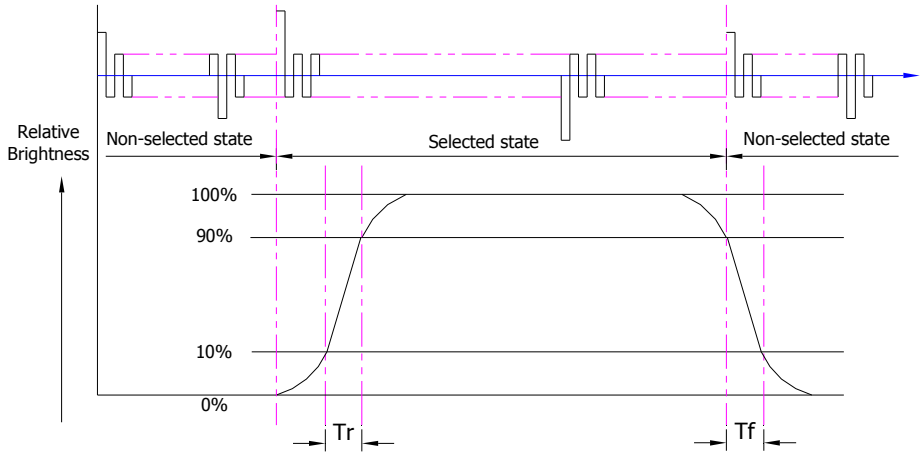
6.1. Optical Characteristics

Ta=25ºC, VDDIN=3.3V

	Item		Symbol	Condition	Specification			Unit
					Min.	Typ.	Max.	
Backlight On (Transmissive Mode)	Luminance on TFT(I_f =20mA/LED)		Lv	Normally viewing angle θX = φY =0º	**270**	**330**	-	cd/m²
	Contrast ratio(See 6.3)		CR		600	800	-	
	Response time (See 6.2)		TR		-	11	14	ms
			TF		-	9	11	
	Chromaticity Transmissive (See 6.5)	Red	XR		**-**	**TBD**	**-**	
			YR		**-**	**TBD**	**-**	
		Green	XG		**-**	**TBD**	**-**	
			YG		**-**	**TBD**	**-**	
		Blue	XB		**-**	**TBD**	**-**	
			YB		**-**	**TBD**	**-**	
		White	XW		**0.26**	**0.31**	**0.36**	
			YW		**0.28**	**0.33**	**0.38**	
	Viewing Angle (See 6.4)	Horizontal	θX+	Center CR≥10	80	89	-	Deg.
			θX-		80	89	-	
		Vertical	φY+		80	89	-	
			φY-		80	89	-	
	NTSC				45	60		%

6.2. Definition of Response Time

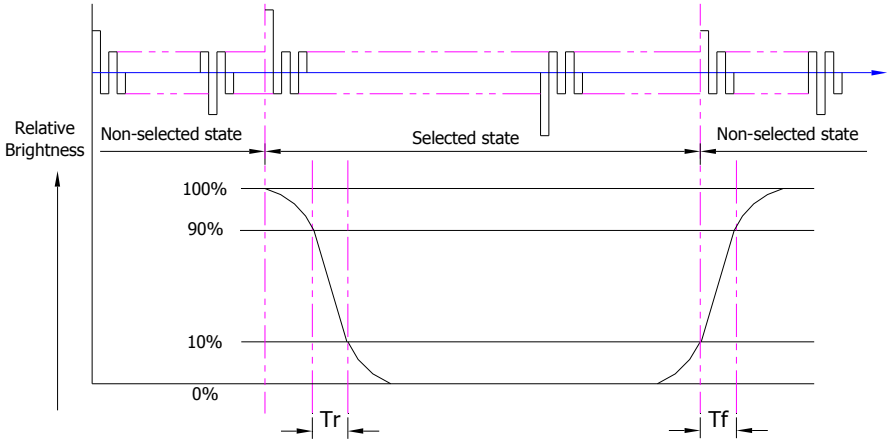
6.2.1. Normally Black Type (Negative)



Tr is the time it takes to change form non-selected stage with relative luminance 10% to selected state with relative luminance 90%;
Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note : Measuring machine: LCD-5100

6.2.2. Normally White Type (Positive)



Tr is the time it takes to change form non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note : Measuring machine: LCD-5100 or EQUI

6.3. Definition of Contrast Ratio

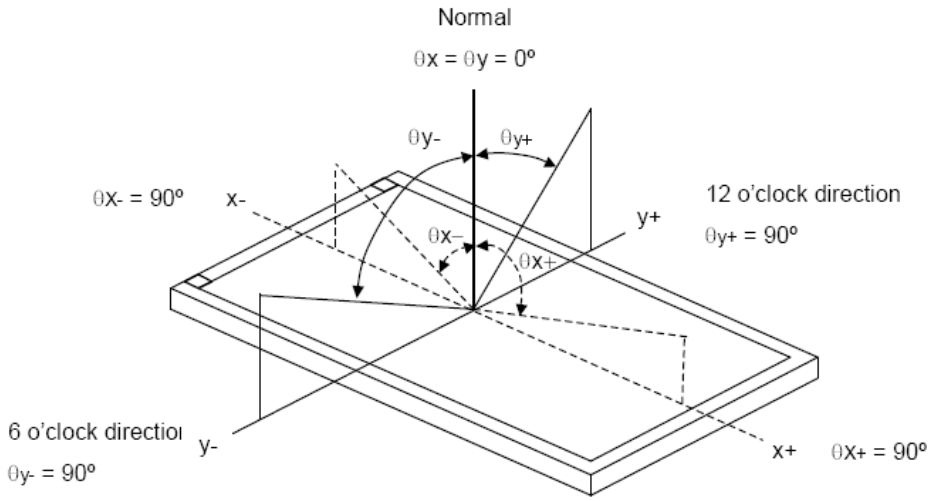
Contrast is measured perpendicular to display surface in reflective and transmissive mode.

The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

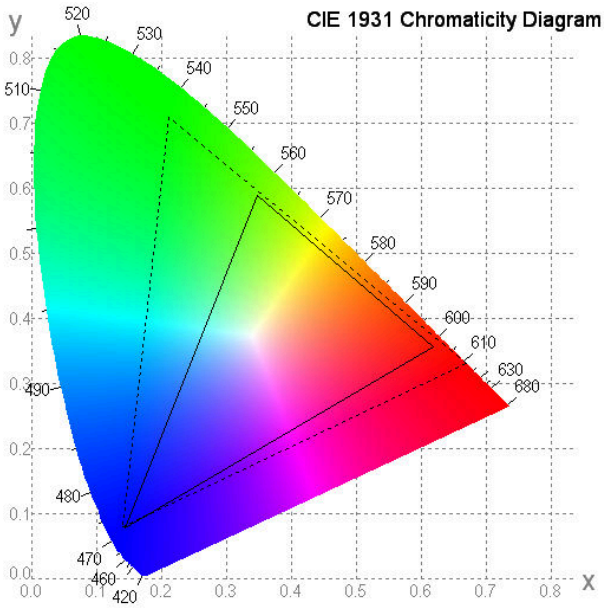
6.4. Definition of Viewing Angles



Measuring machine: LCD-5100 or EQUI

6.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram
NTSC=area of RGB triangle/area of NTSC triangleX100%
Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



6.6. Definition of Surface Luminance, Uniformity and Transmittance

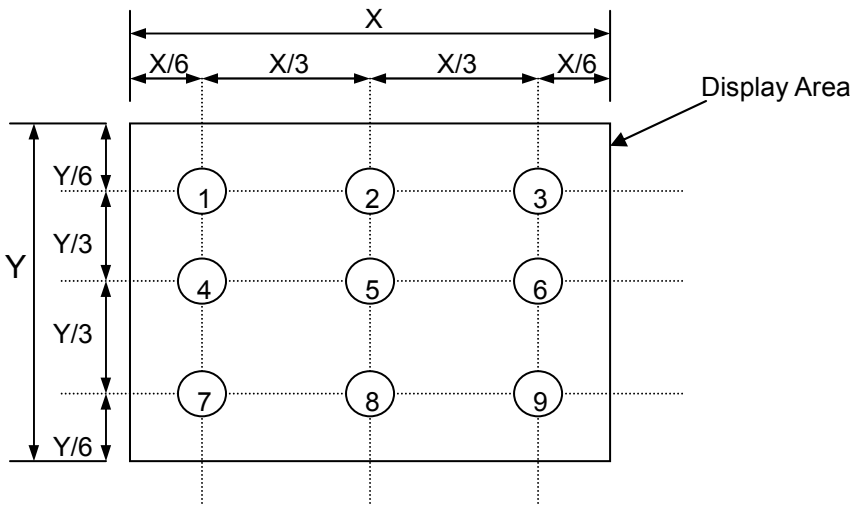
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

6.6.1. Surface Luminance: L_V = average (L_{P1}:L_{P9})

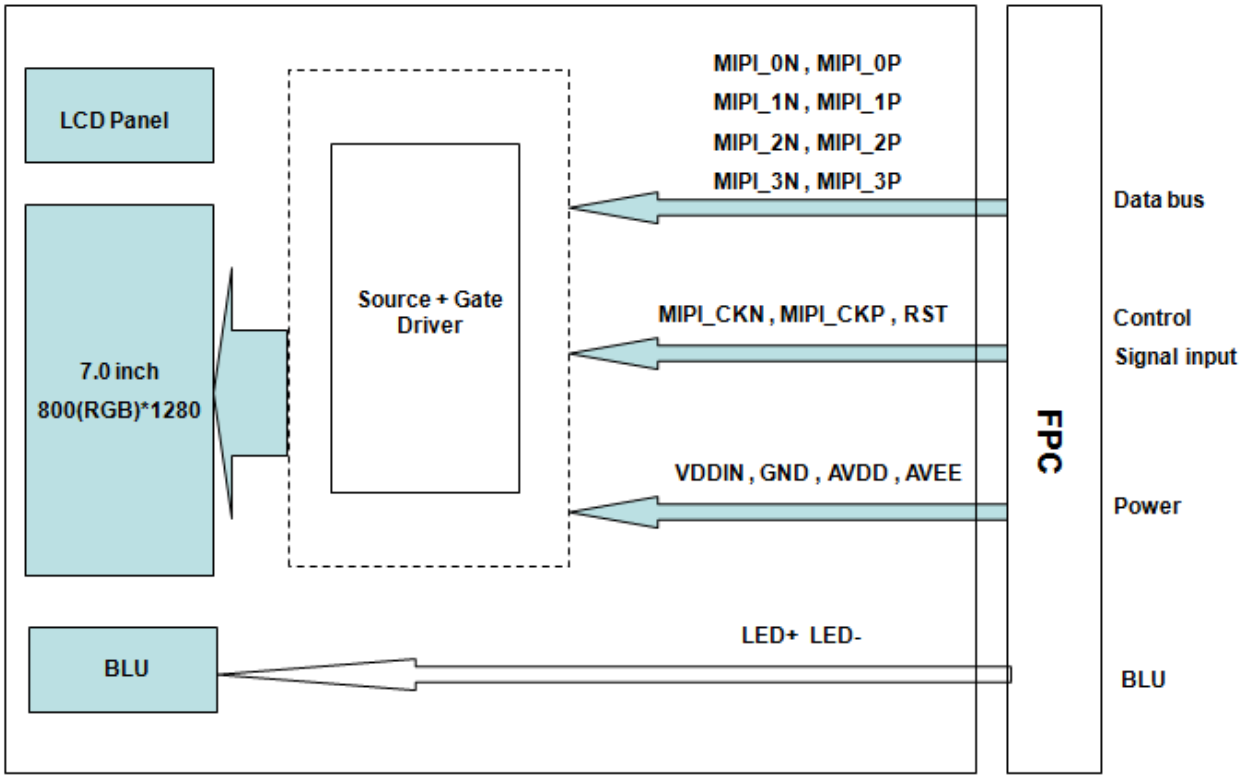
6.6.2. Uniformity = Minimal (L_{P1}:L_{P9}) / Maximal (L_{P1}:L_{P9}) * 100%

6.6.3. Transmittance = L_V on LCD / L_V on Backlight * 100%

Note : Measuring machine: BM-7



7. Block Diagram and Power Supply



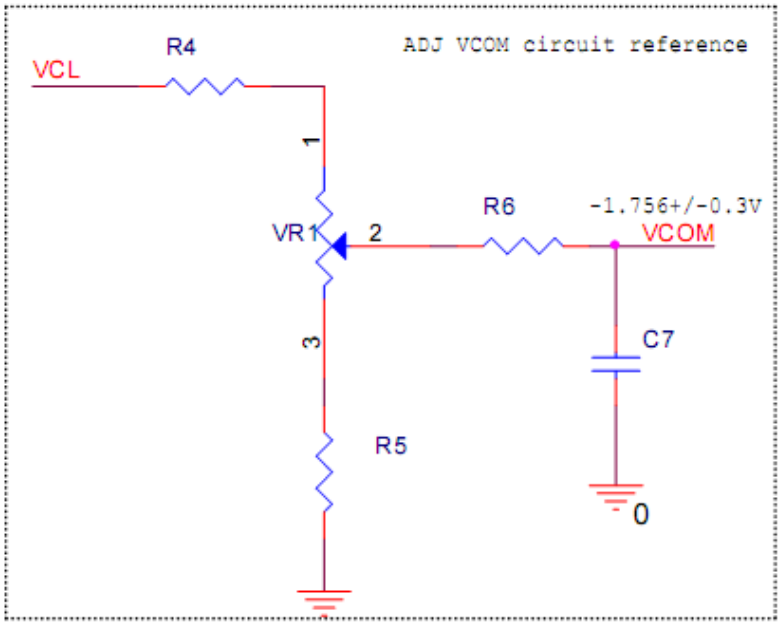
8. Interface Pins Definition

A 40pin connector is used for the module electronics interface.In this model used "FH33J-40S-0.5SH(10)" manufactured by Hirose or the same package connector.

No.	Symbol	Function	Remark
1	VCOM	Common Voltage(-1.756 ± 0.3 V)	
2	VDDIN	Power supply for interface system except MIPI interface pin,VDDIN=3.3V	
3	VDDIN		
4	GND	Ground	
5	RST	Global reset pin	
6	NC	No connect	
7	GND	Ground	
8	MIPI_0N	MIPI Negative data signal (-)	
9	MIPI_0P	MIPI Positive data signal (+)	
10	GND	Ground	
11	MIPI_1N	MIPI Negative data signal (-)	
12	MIPI_1P	MIPI Positive data signal (+)	
13	GND	Ground	
14	MIPI_CKN	MIPI Negative clock signal (-)	
15	MIPI_CKP	MIPI Positive clock signal (+)	
16	GND	Ground	
17	MIPI_2N	MIPI Negative data signal (-)	
18	MIPI_2P	MIPI Positive data signal (+)	
19	GND	Ground	
20	MIPI_3N	MIPI Negative data signal (-)	
21	MIPI_3P	MIPI Positive data signal (+)	
22	GND	Ground	
23	NC	No connect	
24	NC	No connect	
25	GND	Ground	
26	NC	No connect	
27	PWMO	PWM control signal for LED driver (CABC)	
28	NC	No connect	
29	VCL	Output voltage pin,use it to generate Vcom voltage by a VR circuit (output voltage -2.5V)	
30	GND	Ground	
31	LED-	LED cathode	
32	LED-	LED cathode	
33	NC	No connect	
34	NC	No connect	
35	AVEE	Analog supply negative voltage	
36	NC	No connect	

37	NC	No connect	
38	AVDD	Analog supply positive voltage	
39	LED+	LED Anode	
40	LED+	LED Anode	

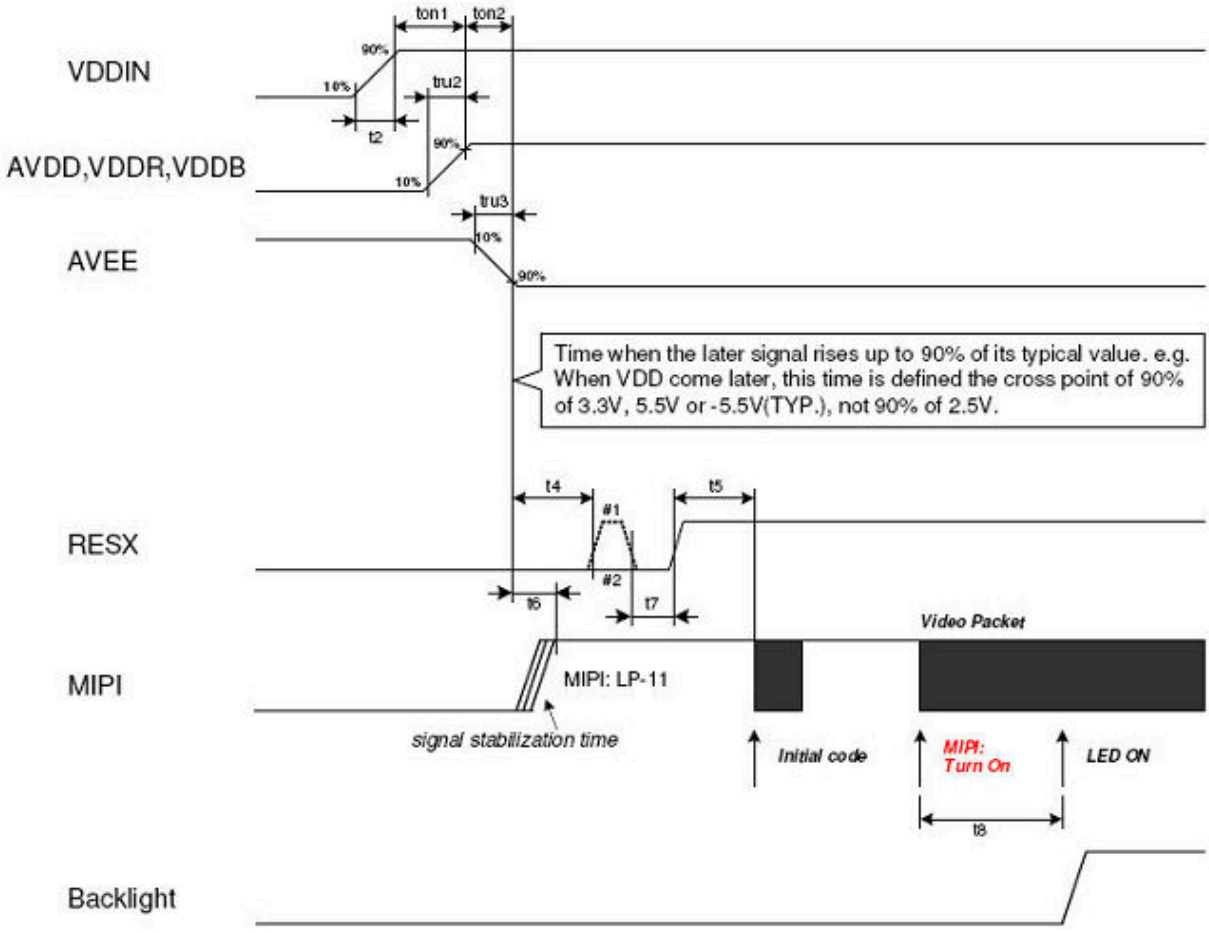
Note1:Typical VCOM is only a reference value,it must be optimized according to each LCM,Be sure to use VR



Note 2: Global reset pin.Active Low to enter Reset State.Normally pull high.suggest to connecting withan RC reset circuit for stability.

9. Power Sequence

a) Power ON



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

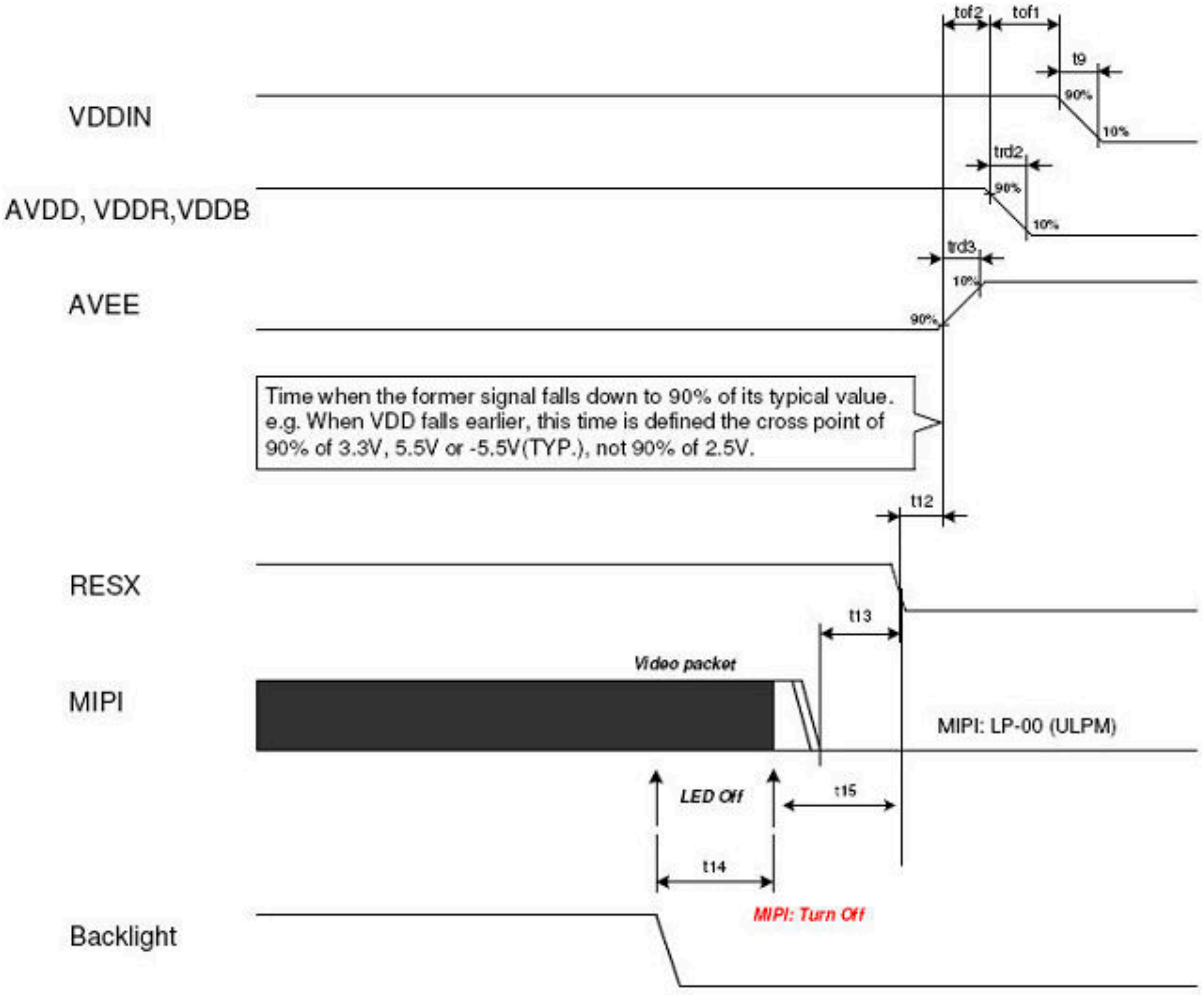
Note 2: This power-on sequence is based on adding schottky diode on VGLX pin to ground.

Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1		No limit		ms	
ton2		0(Note)		ms	
ton3		No limit	-	ms	
ton4		No limit	-	ms	
t2			150	μs	
tru1			150	μs	
tru2			150	μs	
tru3			150	μs	
tru4			150	μs	
t4	40	-	-	ms	

t5	120			ms	
t6	0			ms	
t7	10			µs	
t8	8			VS	Keep data more than 8 frames (VS)

a) Power OFF



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150			µs	
tof1		No limit		ms	
tof2		0(Note)	-	ms	
tof3		No limit	-	ms	
tof4		No limit		ms	
trd1	150			µs	
trd2	150			µs	
trd3	150			µs	
trd4	150			µs	
t12	0		-	ms	
t13	0			ms	
T14	0			ms	
T15	10			ms	

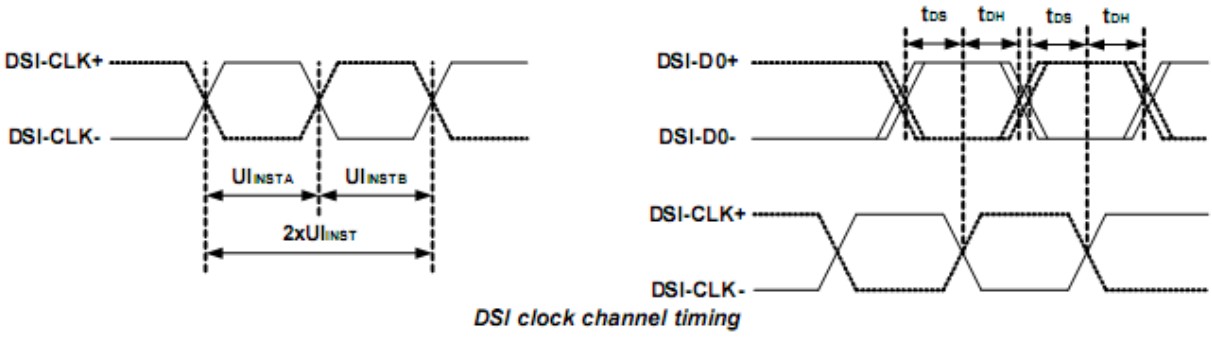
10. Timing Characteristics

11.1 AC Electrical Characteristics

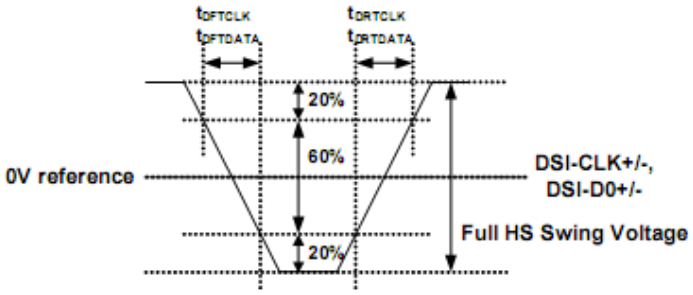
1) High Speed mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	tDS	Data to clock setup time	0.15x UI	-	-	ps	
DSI-Dn+/-	tDH	Data to clock hold time	0.15x UI	-	-	ps	
DSI-CLK+/-	tDRTCLK	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDRTDATA	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	tDFTCLK	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDFTDATA	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.
Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.
Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.



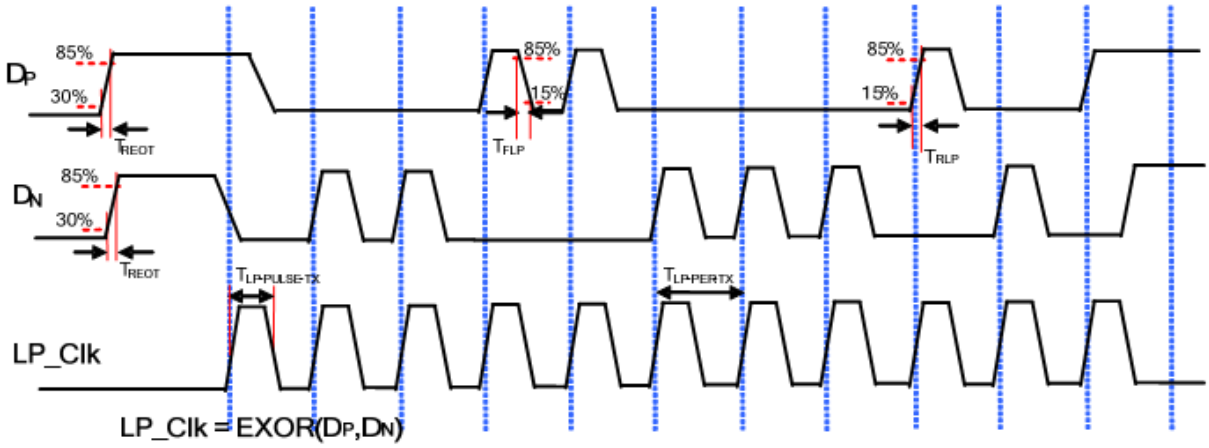
DSI clock channel timing



Rising and fall time on clock and data channel

2) LP transmission

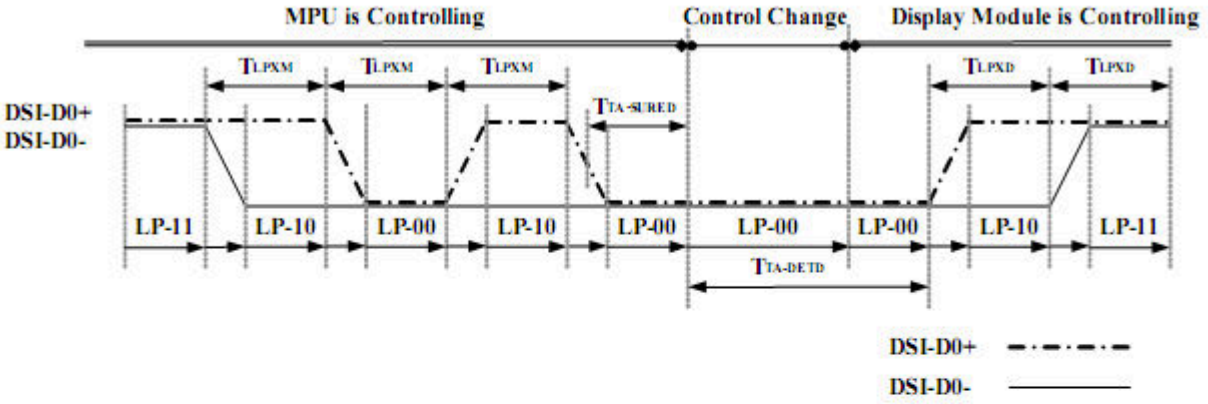
Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DSI CLK frequency(LP)	F_{DSICLK_LP}			10	MHz	
DSI CLK Cycle Time(LP)	t_{CLKC_LP}	100			ns	
DSI Data Transfer Rate(LP)	t_{DSIR_LP}			10	Mbps	
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	35	ns	
30%-85% rise time(from HS to LP)	T_{REOT}	-	-	35	ns	
Pulse width of the LP exclusive-OR clock	$t_{LP\text{-}PULSE\text{-}TX}$	50	65	-	ns	
Period of the LP exclusive-OR clock	$t_{LP\text{-}PRE\text{-}TX}$	100	130	-	ns	

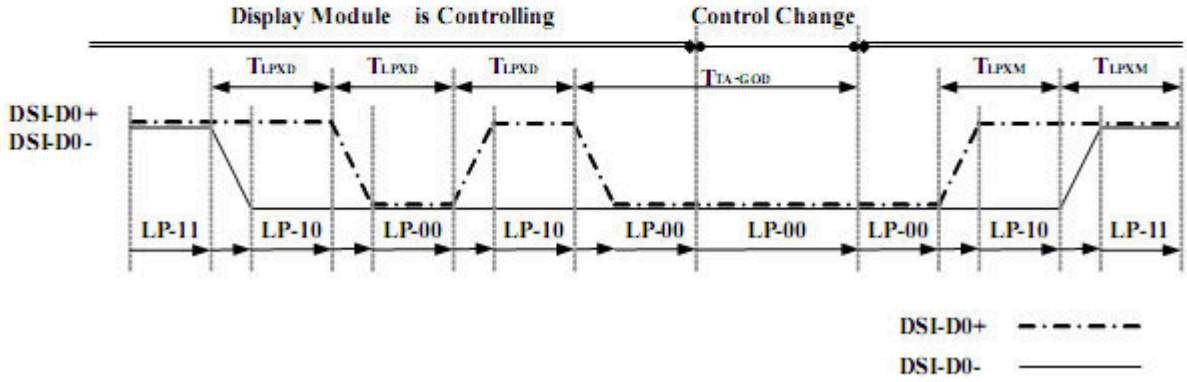


3) Low power mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+ /-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU (Display Module	50	-	75	ns	Input
DSI-D0+ /-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (MPU	50	-	75	ns	Output
DSI-D0+ /-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2xTLPXD	ns	Output
DSI-D0+ /-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD	-	-	ns	Input
DSI-D0+ /-	TTA-GOD	Time to drive LP-00 after turnaround request - MPU	4xTLPXD	-	-	ns	Output

Bus Turnaround (BAT) from MPU to display module Timing



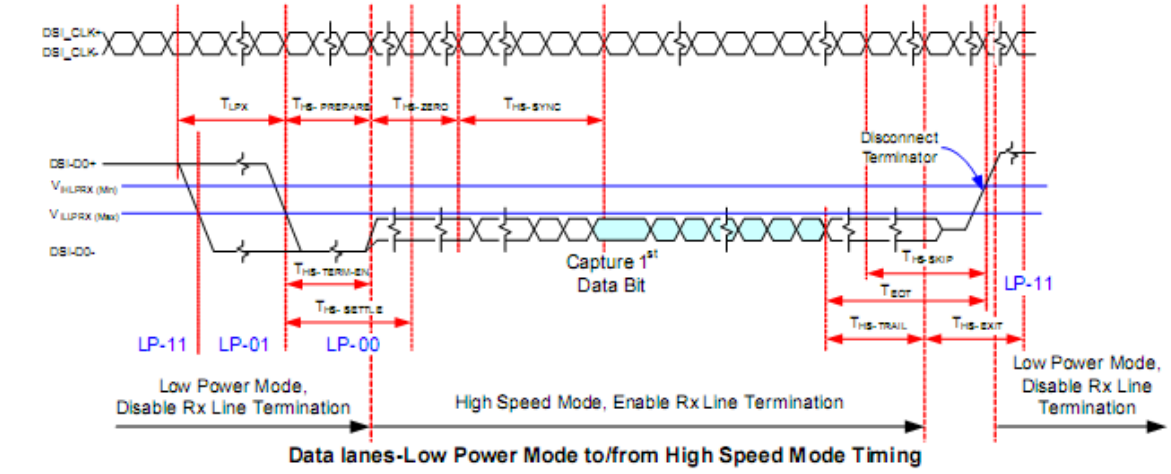


Bus Turnaround (BAT) from display module to MPU Timing

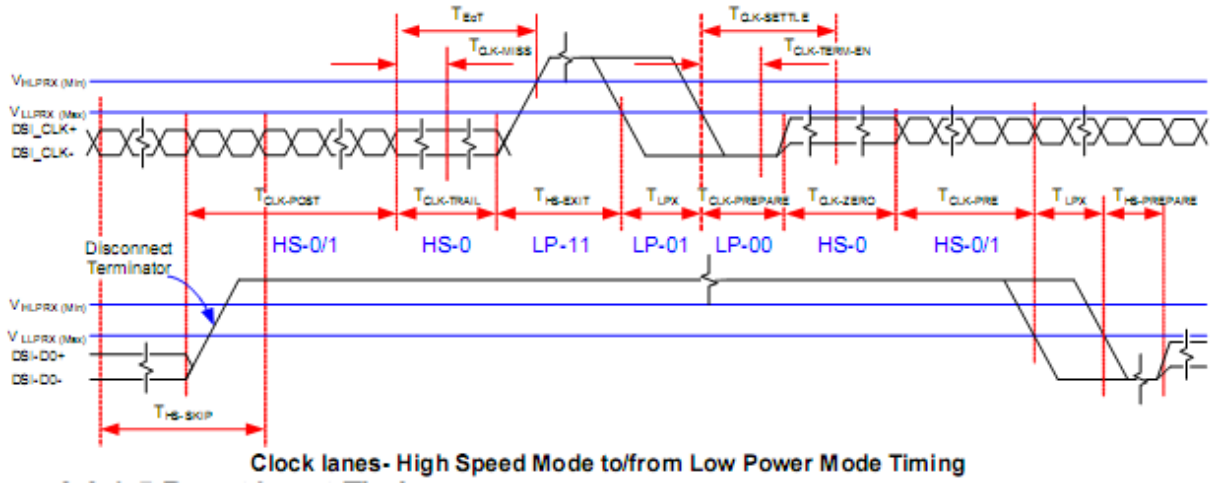
4) DSI bursts

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.
Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before activity in clock and data lanes again.

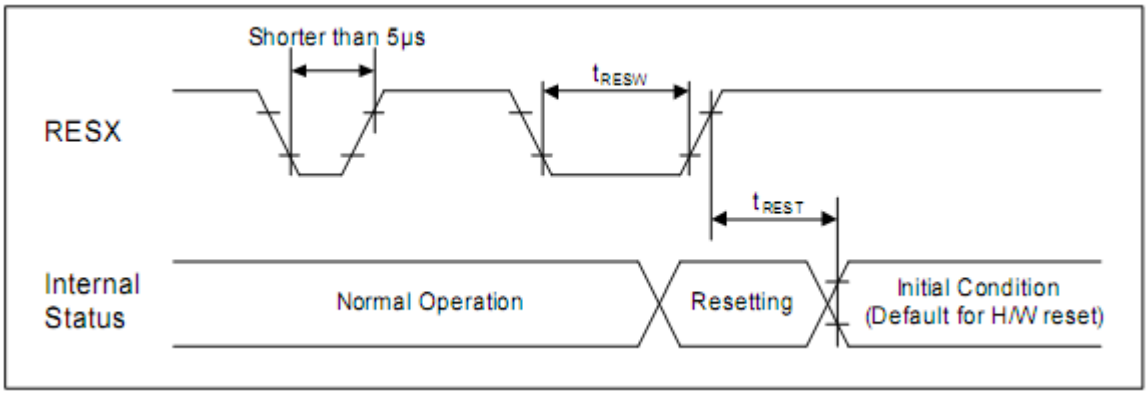


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

11.2 Reset input timing



Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_{RESW}	Reset "L" pulse width (Note 1)	10	-	-	µs	
	t_{REST}	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

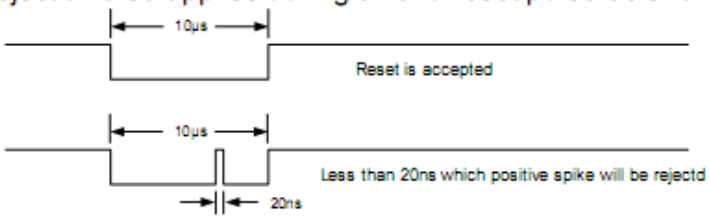
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:

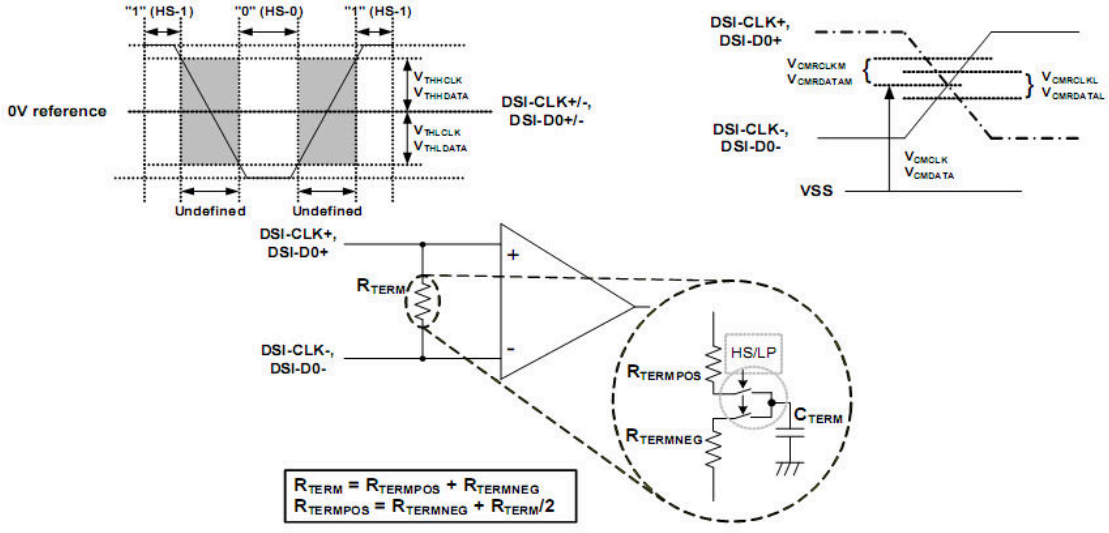


Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

11.3 DC characteristic for DSI HS mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	VCMCLK VCMDATA	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	VCMRCLKL VCMRDATAL	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	VCMRCLKM VCMRDATAM	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	VTHLCLK VTHLDATA	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	VTHHCLK VTHHDATA	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	VILHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	VIHHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	RTERM	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	VTERM-EN	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	CTERM	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 °C (to +85 °C no damage).
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without VCMRCLKM / VCMRDATAM.
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.



Differential voltage range, termination resistor and Common mode voltage

11. Quality Assurance

11.1. Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

11.2. Standard for Quality Test

11.2.1. Sampling Plan:
GB2828.1-2012
Single sampling, normal inspection.

11.2.2. Sampling Criteria:
Visual inspection: AQL 1.5%
Electrical functional: AQL 0.65%.

11.2.3. Reliability Test:
Detailed requirement refer to Reliability Test Specification.

11.3. Nonconforming Analysis & Disposition

11.3.1. Nonconforming analysis:

11.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

11.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

11.3.1.3. If can not finish the analysis on time, customer will be notified with the progress status.

11.3.2. Disposition of nonconforming:

11.3.2.1. Non-conforming product over PPM level will be replaced.

11.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

11.4. Agreement Items

Shall negotiate with customer if the following situation occurs:

11.4.1. There is any discrepancy in standard of quality assurance.

11.4.2. Additional requirement to be added in product specification.

11.4.3. Any other special problem.

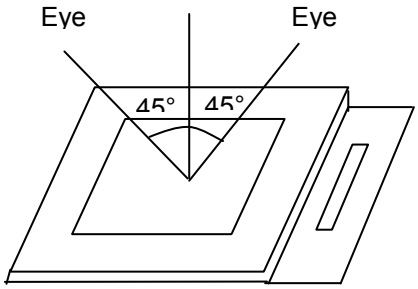
11.5. Standard of the Product Visual Inspection

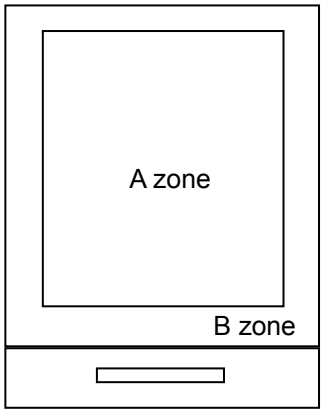
11.5.1. Appearance inspection:

11.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

11.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

11.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,



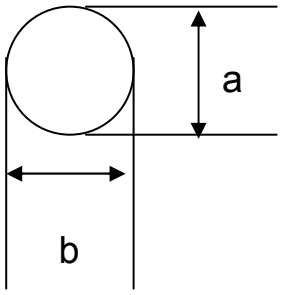


11.5.2. Basic principle:

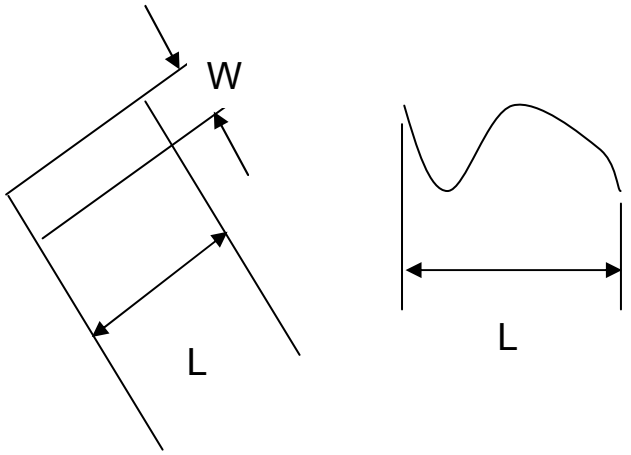
11.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

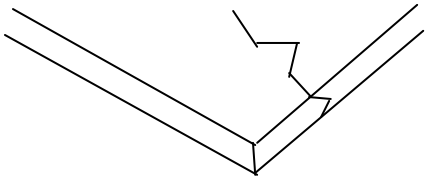
11.5.2.2. New item must be added on time when it is necessary.

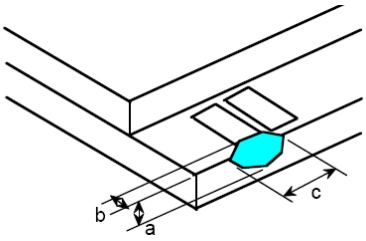
11.6. Inspection Specification for the TFT module

<table>
<tr><th>No.</th><th>Item</th><th>Criteria (Unit: mm)</th></tr>
<tr><td>01</td><td>Black / White spot
Foreign material (Round type)
Pinholes
Stain
Particles inside cell.
(Minor defect)</td><td>


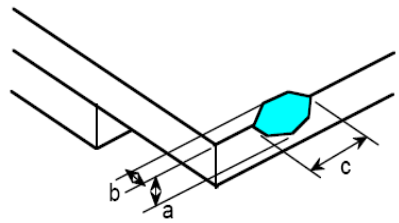
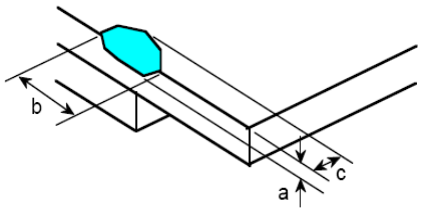
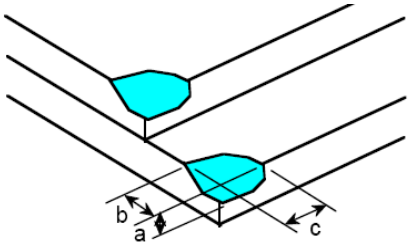
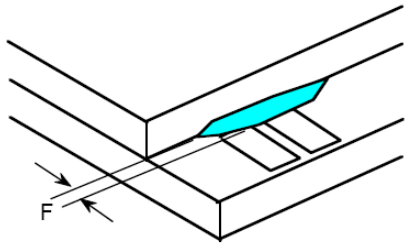
φ= (a + b) /2
<table>
<tr><th>Area / Size</th><th>Acc. Qty</th></tr>
<tr><td>φ≤0.20</td><td>Ignore</td></tr>
<tr><td>0.20<φ≤0.50</td><td>N≤3</td></tr>
<tr><td>0.50<φ</td><td>0</td></tr>
</table>
Distance between 2 defects should more than 5mm apart.
</td></tr>
<tr><td>02</td><td>Electrical Defect (Minor defect)</td><td>
<table>
<tr><td rowspan="2">Bright dot</td><td>Display Area</td><td>Total</td><td rowspan="3">Note1</td></tr>
<tr><td>N≤2</td><td>N≤2</td></tr>
<tr><td>Dark dot</td><td>N≤4</td><td>N≤4</td></tr>
<tr><td>Total dot</td><td>N≤4</td><td>N≤4</td><td></td></tr>
<tr><td>Mura</td><td colspan="2">Not visible through 5% ND filters.</td><td>Note2</td></tr>
</table>
Remark:
1. Bright dot caused by scratch and foreign object accords to item 1.
</td></tr>
</table>

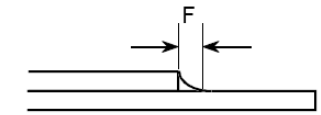
<table>
<tr>
<td>03</td>
<td>Black and White line Scratch Foreign material (Line type) (Minor defect)</td>
<td>


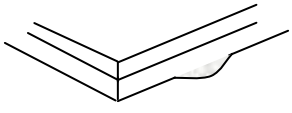
<table>
<tr><th>Length</th><th>Width</th><th>Acc. Qty</th></tr>
<tr><td>/</td><td>W ≦ 0.1</td><td>Ignore</td></tr>
<tr><td>L ≦ 2.5</td><td>0.1 ＜ W ≦ 0.2</td><td>3</td></tr>
<tr><td>L＞2.5</td><td>0.2 ＜ W</td><td>0</td></tr>
<tr><td colspan="2">Total</td><td>3</td></tr>
</table>
Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.
</td>
</tr>
<tr>
<td>04</td>
<td>Glass Crack (Minor defect)</td>
<td>

Crack is potential to enlarge, any type is not allowed.
</td>
</tr>
</table>

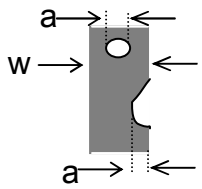
<table>
<tr>
<td>05</td>
<td>Glass Chipping Pad Area:
(Minor defect)


</td>
<td>
<table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>3</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr>
<td>06</td>
<td>Glass Chipping Rear of Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>07</td>
<td>Glass Chipping Except Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>08</td>
<td>Glass Corner Chipping:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c < 3.0, b< 3.0</td><td>Ignore</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>09</td>
<td>Glass Burr:
(Minor defect)
 

  </td>
<td><table>
<tr><th>Length</th><th>Acc. Qty</th></tr>
<tr><td>F < 1.0</td><td>Ignore</td></tr>
</table>
Glass burr don’t affect assemble and module dimension.</td>
</tr>
</table>

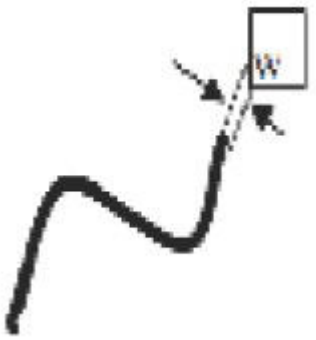
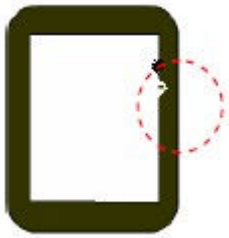
<table>
<tr><td>10</td><td>FPC Defect:
(Minor defect)
 
</td><td>10.1 Dent, pinhole width a<w/3.
(w: circuitry width.)
10.2 Open circuit is unacceptable.
10.3 No oxidation, contamination and distortion.</td></tr>
<tr><td>11</td><td>Bubble on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.30</td><td>Ignore</td></tr><tr><td>0.30 <φ≤0.50</td><td>N≤2</td></tr><tr><td>0.50 < φ</td><td>N=0</td></tr></table></td></tr>
<tr><td>12</td><td>Dent on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.25</td><td>Ignore</td></tr><tr><td>0.25 <φ≤0.50</td><td>N≤4</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>13</td><td>Bezel</td><td>13.1 No rust, distortion on the Bezel.
13.2 No visible fingerprints, stains or other contamination.</td></tr>
<tr><td>14</td><td>Touch Panel</td><td>D: Diameter W: width L: length
14.1 Spot: D<0.25 is acceptable
0.25≤D≤0.4
2dots are acceptable and the distance between defects should more than 10 mm.
D>0.4 is unacceptable
14.2 Dent: D>0.40 is unacceptable
14.3 Scratch: W≤0.03, L≤10 is acceptable,
0.03<W≤0.10, L≤10 is acceptable
Distance between 2 defects should more than 10 mm.
W>0.10 is unacceptable.</td></tr>
<tr><td>15</td><td>PCB</td><td>15.1 No distortion or contamination on PCB terminals.
15.2 All components on PCB must same as documented on the BOM/component layout.
15.3 Follow IPC-A-600F.</td></tr>
</table>

16	Soldering	Follow IPC-A-610C standard
17	Electrical Defect (Major defect)	The below defects must be rejected. 17.1 Missing vertical / horizontal segment, 17.2 Abnormal Display. 17.3 No function or no display. 17.4 Current exceeds product specifications. 17.5 LCD viewing angle defect. 17.6 No Backlight. 17.7 Dark Backlight. 17.8 Touch Panel no function.

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

11.7. Inspection Specification for the Cover LENS

<table>
<tr><td>01</td><td>Tempered hardness</td><td>Drop ball test ,Dropping 64g, φ25.4mm steel ball from 45cm height, will not damage glass</td></tr>
<tr><td>02</td><td colspan="2">Cover lens must be without any chips, cracks or other damage when viewed from the front.</td></tr>
<tr><td>03</td><td>Same/Different color spot
  </td><td>D: Diameter W: width L: length
<table>
<tr><th>Diameter</th><th>Acc. Qty</th></tr>
<tr><td>D < 0.20</td><td>Ignore</td></tr>
</table>
Active Area：
<table>
<tr><th>Diameter</th><th>Acc. Qty</th></tr>
<tr><td>0.20 ＜ D ≦ 0.30</td><td>2</td></tr>
<tr><td>0.30 ＜ D ≦ 0.50</td><td>1</td></tr>
<tr><td>D>0.5</td><td>NG</td></tr>
</table>
Viewing Area：
<table>
<tr><th>Diameter</th><th>Acc. Qty</th></tr>
<tr><td>D<0.20</td><td>Ignore</td></tr>
<tr><td>0.20 ＜ D ≦ 0.5</td><td>3</td></tr>
<tr><td>D>0.5</td><td>NG</td></tr>
</table>
Distance between 2 defects should more than15mm apart.</td></tr>
</table>

<table>
<tr>
<td>04</td>
<td>Cover lens line Scratch
  </td>
<td>
<table>
<tr><th>Length</th><th>Width</th><th>Acc. Qty</th></tr>
<tr><td>/</td><td>W ≦ 0.08mm</td><td>Ignore</td></tr>
<tr><td>L ≦ 5</td><td>0.08 ＜ W ≦ 0.15</td><td>2</td></tr>
<tr><td>L ≦ 3</td><td>0.15 ＜ W ≦ 0.20</td><td>1</td></tr>
<tr><td>-</td><td>W>0.2</td><td>NG</td></tr>
<tr><td>L>5</td><td>-</td><td>NG</td></tr>
</table>
Distance between 2 defects should more than15mm apart.
</td>
</tr>
<tr>
<td>05</td>
<td>Printing sawtooth
  </td>
<td>
<table>
<tr><th>Length</th><th>Width</th><th>Acc. Qty</th></tr>
<tr><td>/</td><td>W ≦ 0.2mm</td><td>2</td></tr>
<tr><td>L ≦ 2</td><td>0.2 ＜ W ≦ 0.3</td><td>1</td></tr>
<tr><td>L ≦ 2</td><td>W>0.3</td><td>NG</td></tr>
</table>
</td>
</tr>
</table>

11.8. Classification of Defects

11.8.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

11.8.2. Two minor defects are equal to one major in lot sampling inspection.

11.9. Identification/marking criteria

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

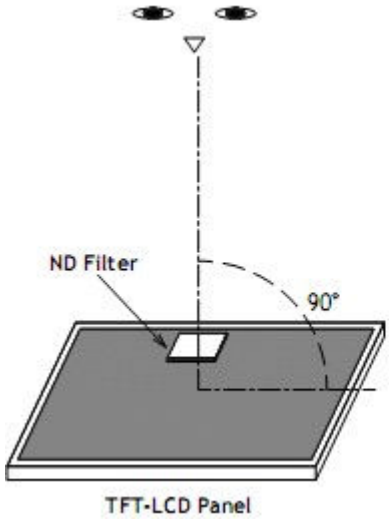
11.10. Packaging

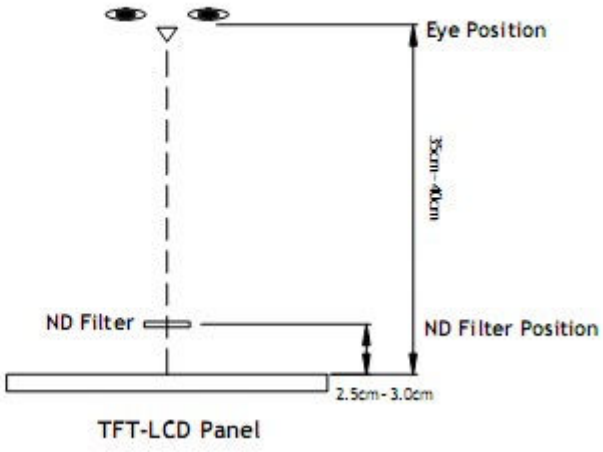
11.10.1. There should be no damage of the outside carton box, each packaging box should have one identical label.

11.10.2. Modules inside package box should have compliant mark.

11.10.3. All direct package materials shall offer ESD protection

Note1: Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.





Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is 350mm±50mm.
Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Note2: Mura on display which appears darker / brighter against background brightness on parts of display area.

12. Reliability Specification

No	Item	Condition	Quantity	Criteria
1	**High Temperature Operating**	**50℃, 96Hrs**	2	GB/T2423.2 -2008
2	**Low Temperature Operating**	**-10℃, 96Hrs**	2	GB/T2423.1 -2008
3	**High Humidity**	**40℃, 90%RH, 96Hrs**	2	GB/T2423.3 -2006
4	**High Temperature Storage**	**60℃, 96Hrs**	2	GB/T2423.2 -2008
5	**Low Temperature Storage**	**-20℃, 96Hrs**	2	GB/T2423.1 -2008
6	**Thermal Cycling Test**	**-10℃, 60min~50℃, 60min, 20 cycles.**	2	GB/T2423.22 -2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X, Y, Z 30 min for each direction.	2	GB/T5170.14 -2009
8	Electrical Static Discharge	Air:±4KV 150pF/330Ω 5 times	2	GB/T17626.2 -2006
		Contact:±2KV 150pF/330Ω 5 times		
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	2	GB/T2423.8 -1995

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

13. Precautions and Warranty

13.1. Safety

13.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

13.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

13.2. Handling

13.2.1. Reverse and use within ratings in order to keep performance and prevent damage.

13.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

13.3. Storage

13.3.1. Do not store the LCD module beyond the specified temperature ranges.

13.4. Metal Pin (Apply to Products with Metal Pins)

13.4.1. Pins of LCD and Backlight

13.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

13.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

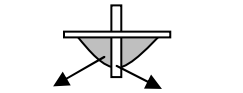
Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

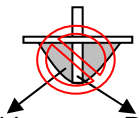
Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

13.4.1.3. Solder Wetting



Recommended



Not Recommended

13.4.2. Pins of EL

13.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

13.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

13.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270～290℃

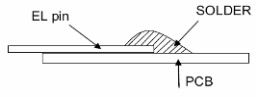
Typical Soldering Time: ≤2s

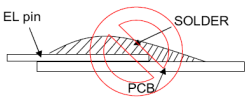
Minimum solder distance from EL lamp (body):2.0mm

13.4.2.4. No horizontal press on the EL leads during soldering.

13.4.2.5. 180° bend EL leads three times is not allowed.

13.4.2.6. Solder Wetting



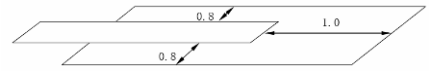


Recommended Not Recommended

13.4.2.7. The type of the solder iron:

Recommended Not Recommended

13.4.2.8. Solder Pad



13.5. Operation

13.5.1. Do not drive LCD with DC voltage

13.5.2. Response time will increase below lower temperature

13.5.3. Display may change color with different temperature

13.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.

13.6. Static Electricity

13.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

13.6.2. The normal static prevention measures should be observed for work clothes and benches.

13.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

13.7. Limited Warranty

13.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.

13.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

13.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

15.Packaging

TBD

16 Outline Drawing