Project No. 项目编号	JT60190-01
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	Standard LCD Module 480x 3RGB x 272 Dots 4.3”TFT LCD
Signature by customer: 客户确认签章：	

PREPARED BY	CHECKED BY	APPROVED BY
Jin Wang	Mayan Zhang	Xinyong Li

PREPAREDBY: CHENZHOU JENSON DISPLAY TECHNOLOGY CO.,LTD
Jeson Tech Park,Demonstration Garden for National Recycle Economy,
YongXing County,HuNan,China
Tel:0755-29556135 Fax:0755-29556126

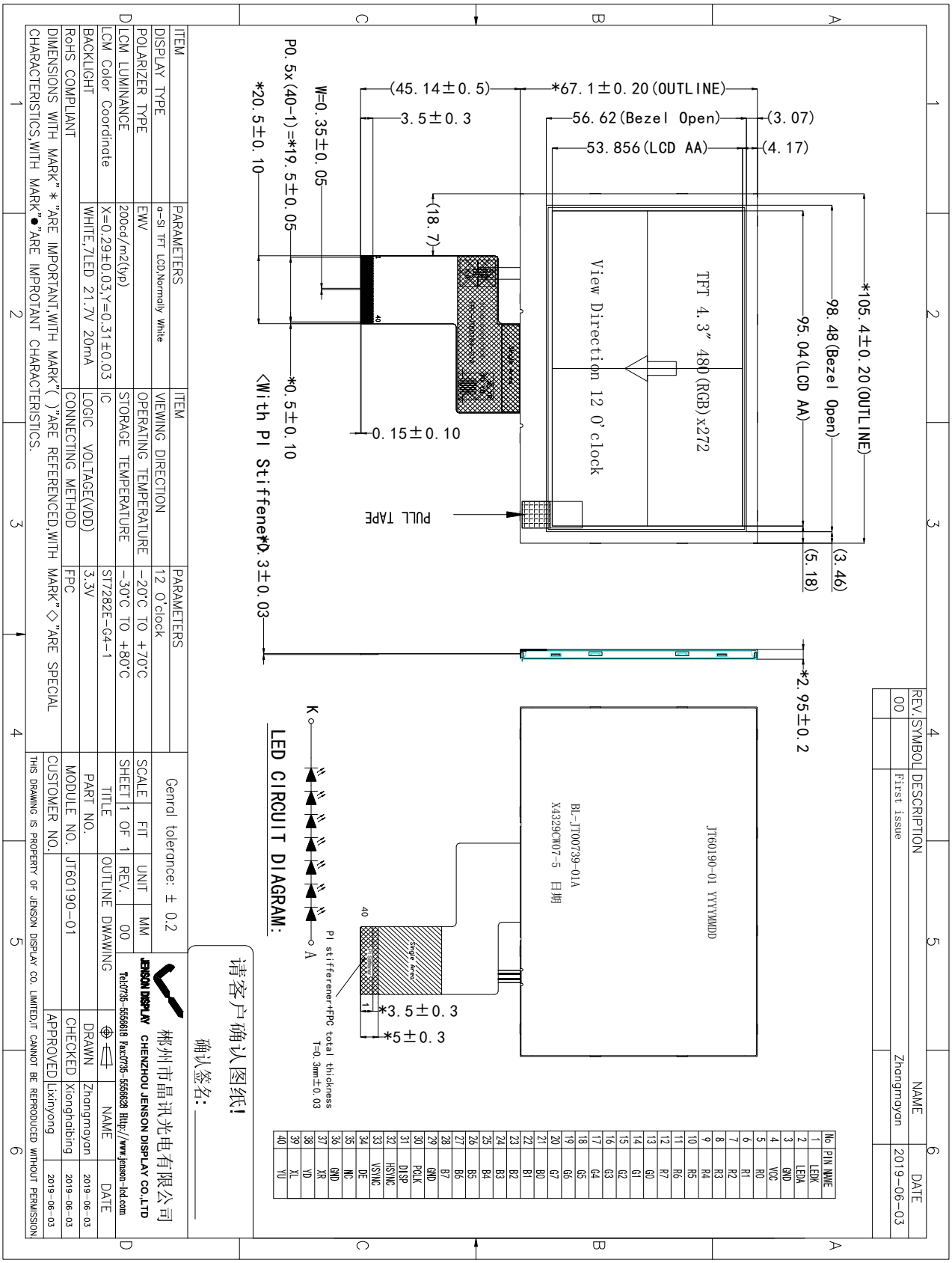
1 Document revision history :

DOCUMENT REVISION	DATE	DESCRIPTION	PREPARED BY	APPROVED BY
V00	2019.06.21	First Release.	Jin Wang	Xinyong Li

1. General Feature:

Item	Standard Value	Unit
Display Size	4.3”	--
Number of Pixels	480(H)x3(RGB)x272(V)	--
Active Area	95.04(L) *53.856W)	mm
Pixel pitch	0.1506(L) × 0.1432(W)	mm
Outline Dimension	105.4(L) ×67.1(W) ×2.95(T)	mm
Pixel Arrangement	RGB vertical stripe	-
Display Mode	Normally White	-
Number of color	16.7M	-
Viewing Direction	12’ O clock	-
Surface Treatment	Anti-Dazzle	-
Interface	RGB interface	-
Driver IC	ST7282E	-
Driver Condition	3.3	V
Backlight	White LED	-
Touch Panel	No touch screen	-
Touch Panel Config Version	-	-
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃
Weight	TBD	g

2.Mechanical Dimension



No	PIN NAME
1	LEDK
2	LEDA
3	GND
4	VCC
5	R0
6	R1
7	R2
8	R3
9	R4
10	R5
11	R6
12	R7
13	G0
14	G1
15	G2
16	G3
17	G4
18	G5
19	G6
20	G7
21	B0
22	B1
23	B2
24	B3
25	B4
26	B5
27	B6
28	B7
29	GND
30	PCLK
31	DISP
32	HSYNC
33	VSYNC
34	DE
35	NC
36	GND
37	XR
38	YD
39	XL
40	YU

REV.	SYMBOL	DESCRIPTION	NAME	DATE
00		First issue	Zhangmoyan	2019-06-03

ITEM	PARAMETERS	ITEM	PARAMETERS
DISPLAY TYPE	a-Si TFT LCD,Normally White	VIEWING DIRECTION	12 O'clock
POLARIZER TYPE	EWV	OPERATING TEMPERATURE	-20°C TO +70°C
LCM LUMINANCE	200cd/m2(typ)	STORAGE TEMPERATURE	-30°C TO +80°C
LCM Color Coordinate	X=0.29±0.03,Y=0.31±0.03	IC	ST7282E-G4-1
BACKLIGHT	WHITE,7LED 21.7V 20mA	LOGIC VOLTAGE(VDD)	3.3V
RoHS COMPLIANT		CONNECTING METHOD	FPC

Genral tolerance: ± 0.2

SCALE	FIT	UNIT	MM
SHEET 1 OF 1	REV.	00	
TITLE	OUTLINE DWAWING		
PART NO.			
MODULE NO.	JT60190-01		
CUSTOMER NO.			

DIMENSIONS WITH MARK"＊"ARE IMPORTANT,WITH MARK"( )"ARE REFERENCED,WITH MARK"◇"ARE SPECIAL CHARACTERISTICS,WITH MARK"●"ARE IMPROTANT CHARACTERISTICS.

请客户确认图纸!

确认签名:_____

郴州市晶讯光电有限公司
CHENZHOU JENSON DISPLAY CO.,LTD
Tel:0735-5556618 Fax:0735-5556828 Http://www.jenson-lcd.com

	NAME	DATE
DRAWN	Zhangmoyan	2019-06-03
CHECKED	Xionghaibing	2019-06-03
APPROVED	Lixinyong	2019-06-03

3.Pin Description

3-1 TFT LCD Pin Description

Pin No.	Symbol	Function
1	LEDK	Cathode for back light power supply.
2	LEDA	Anode for back light power supply.
3	GND	Ground pins.
4	VCC	Analog power Supply 3.3V.
5-12	R0-R7	Red pixel data.
13-20	G0-G7	Green pixel data.
21-28	B0-B7	Blue pixel data.
29	GND	Ground pins.
30	PCLK	Pixel clock input in RGB interface
31	DISP	Sets the display mode
32	HSYNC	Horizontal sync input in RGB interface
33	VSYNC	Vertical sync input in RGB interface
34	DE	Data enable input in RGB interface
35	NC	No connect.
36	GND	Ground pins.
37	XR	No connect.
38	YD	No connect.
39	XL	No connect.
40	YU	No connect.

4. Electrical Characteristics

4-1 TFT LCD Module Operating Conditions

Item	Symbol	Condition	Min	Type	Max	Uint
Supply Voltage	VCC	-	3.0	3.3	3.6	V
TFT Gate on voltage	VGH	-	-	16	-	V
TFT Gate off voltage	VGL	-	-7	-	-10	V
Analog Supply voltage	AVDD	-	9.4	9.6	9.8	V
TFT Common voltage	VCOM	-	1.7	-	2.7	V

4-2 LED back light specification (per a chip)

Item	Symbol	Condition	Min	Type	Max	Uint
Forward voltage	Vt	If=20mA	21	22.4	23.8	V
Forward current	Ipn	/1-chip	-	20	-	mA
Reverse voltage	Vr	Per chip	-	-	4.0	V
Reverse Current	Ir	Vr=4V	-	-	15	uA
Uniformity(with L/G)	-	If=20mA	75	-	-	%
Luminance with CTP	Lv	If=20mA	150	200	-	cd/m2
LED Life time	20000H Min					

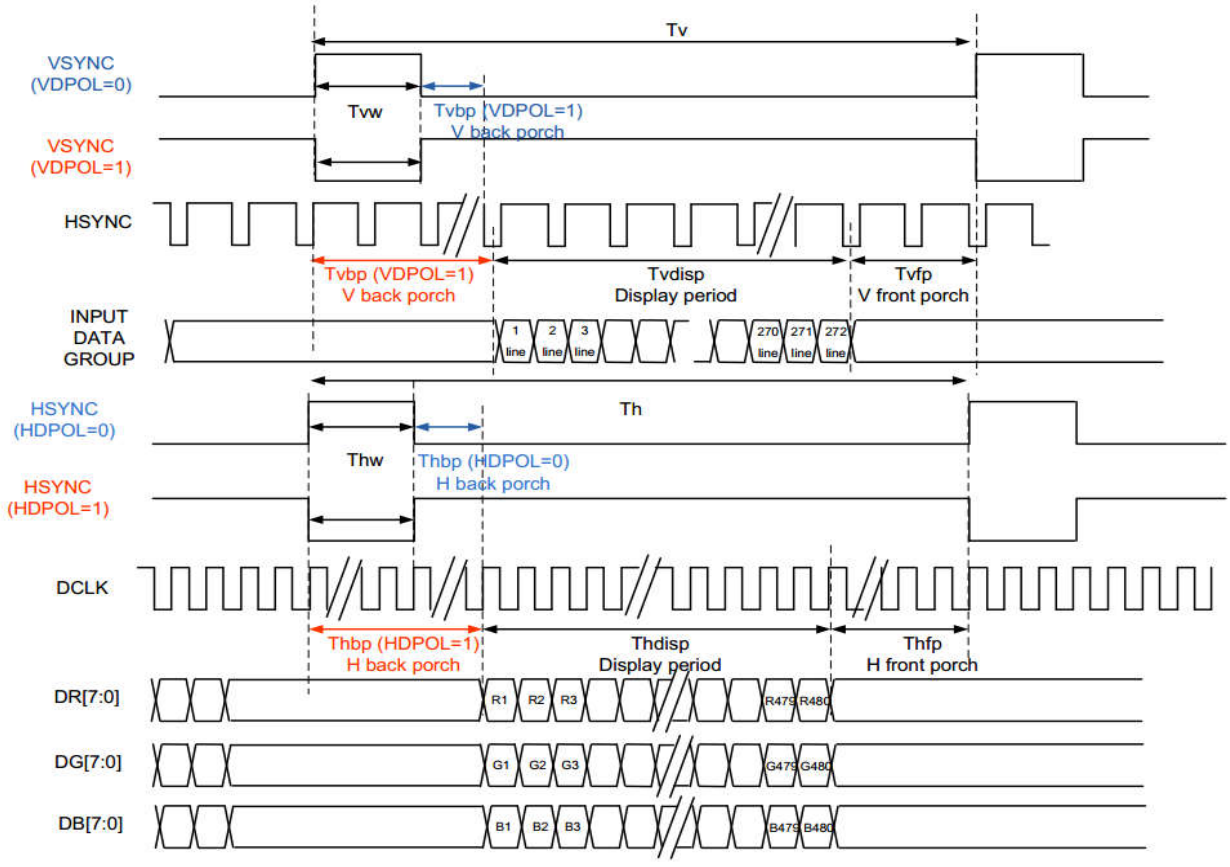
5. RGB Timing Characteristics

5-1 Parallel 24-bit RGB Timing Table

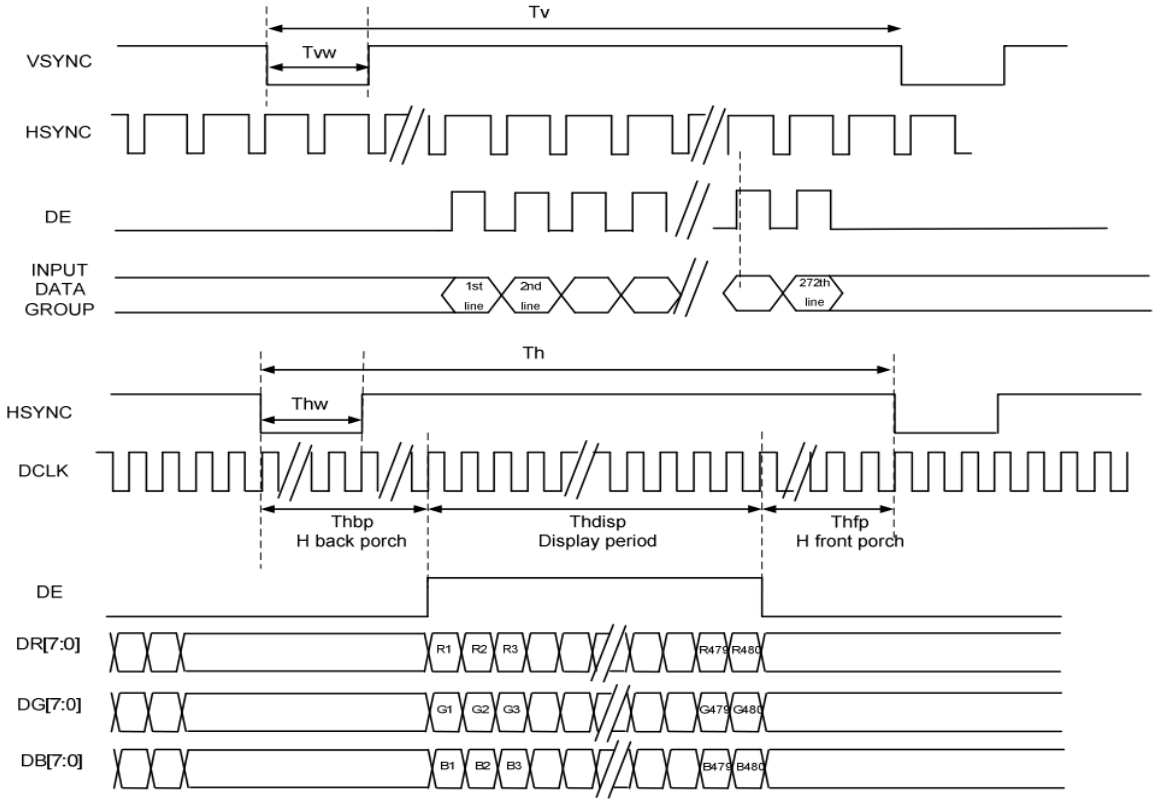
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK Frequency		Fclk	8	9	12	MHz	
DCLK Period		Tclk	83	111	125	Ns	
HSYNC	Period Time	Th	485	531		DCLK	
	Display Period	Thdisp		480		DCLK	
	Back Porch	Thbp	3	43		DCLK	By H_Blanking setting
	Front Porch	Thfp	2	8		DCLK	
	Pulse Width	Thw	2	4		DCLK	
VSYNC	Period Time	Tv	276	292		H	
	Display Period	Tvdisp		272		H	
	Back Porch	Tvbp	2	12		H	By V_Blanking setting
	Front Porch	Tvfp	2	8		H	
	Pulse Width	Tvw	2	4		H	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

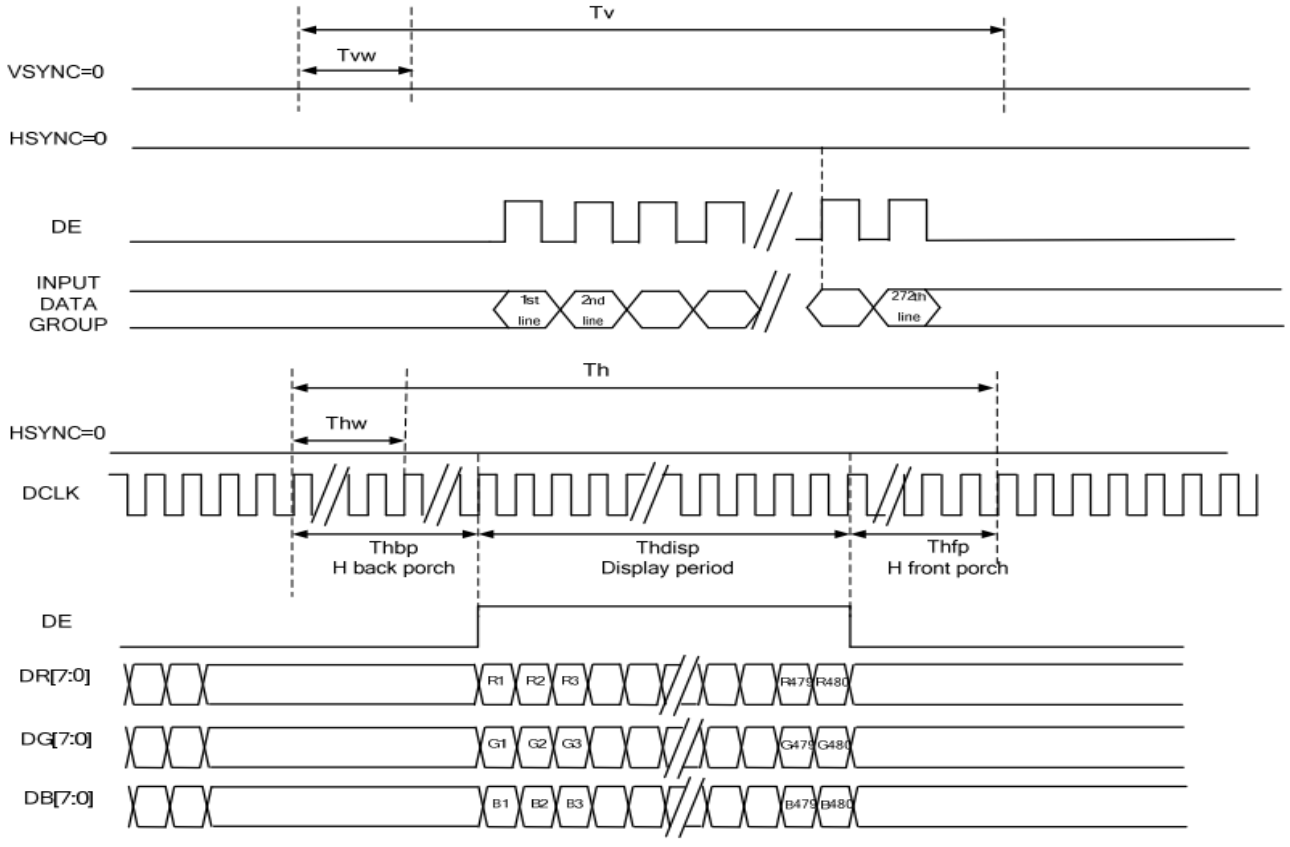
5-2 SYNC Mode Timing Diagram



5-3 SYNC-DE Mode Timing Diagram



5-4 DE Mode Timing Diagram

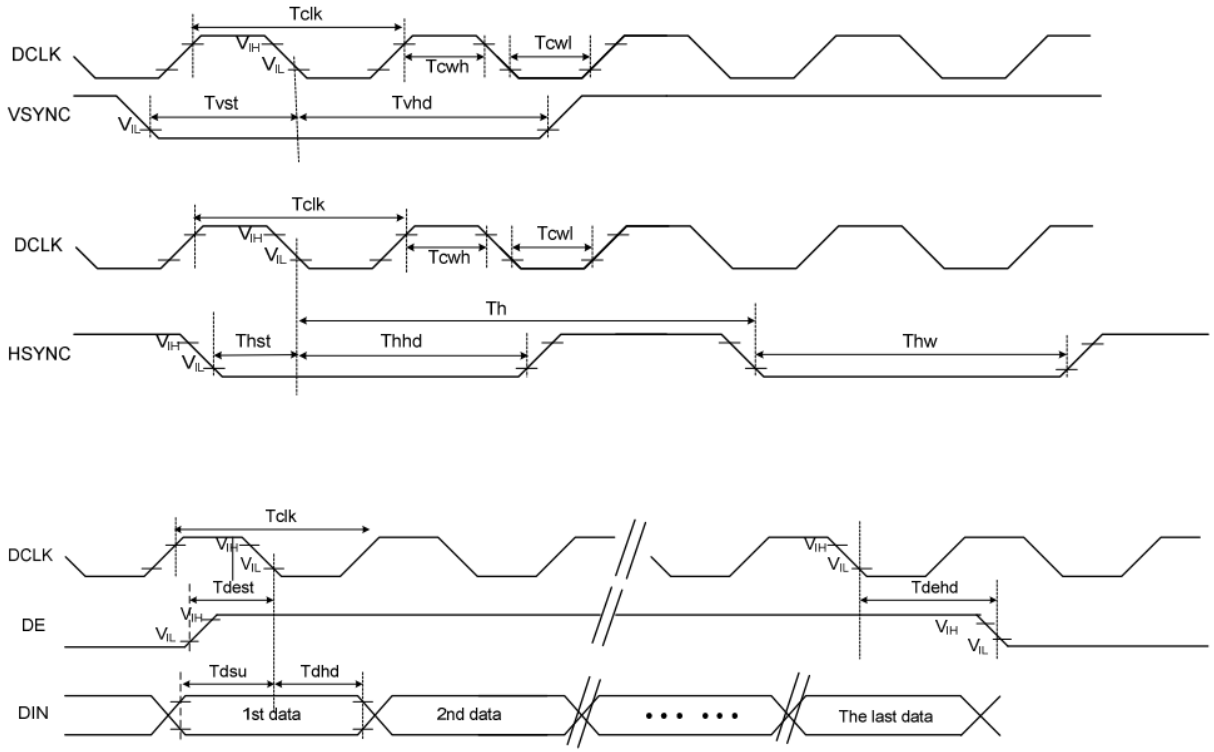


5-5 AC Electrical Characteristics

VCC=VDD=VDDI= 3.3V, AGND= 0V

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
System operation timing						
VDD power source slew time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB pulse width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
Input/ Output timing						
CLK pulse duty	Tcw	40	50	60	%	
Hsync width	Thw	1	-	-	DCLK	
Hsync period	Th	55	60	65	us	
Vsync setup time	Tvst	12	-	-	ns	
Vsync hold time	Tvhd	12	-	-	ns	
Hsync setup time	Thst	12	-	-	ns	
Hsync hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	
Data hold time	Tdhd	12	-	-	ns	
DE setup time	Tdest	10	-	-	ns	
DE setup time	Tdehd	10	-	-	ns	
SD output stable time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD output rise and fall time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF

5-6 Clock and Data Input Timing Diagram



5-7 DC Characteristics for Digital Circuit

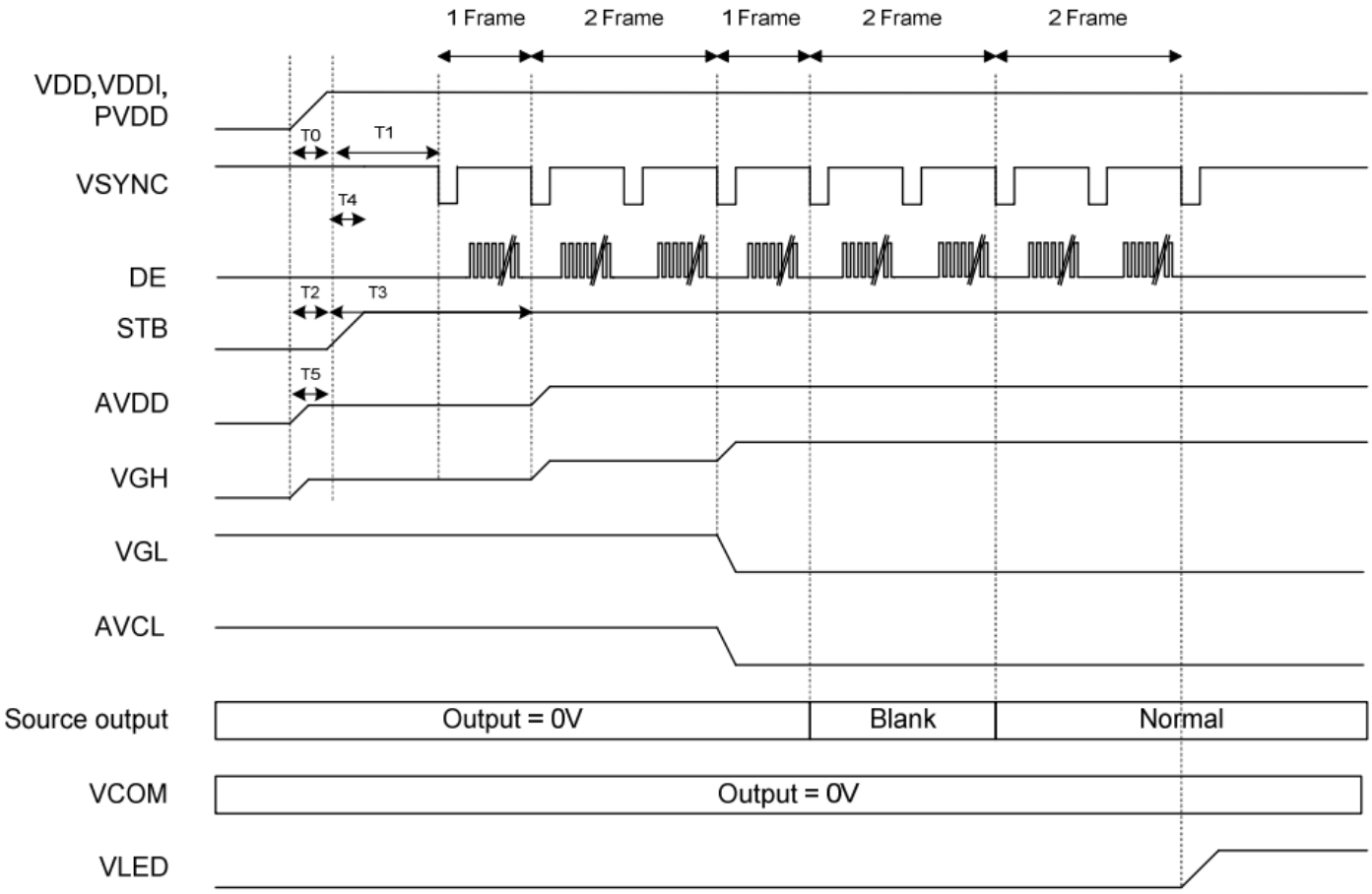
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	VDDI=3.3V
Logic-Low Input Voltage	Vil	DGND	-	0.3VDDI	V	VDDI=3.3V
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	VDDI=3.3V
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	VDDI=3.3V

5-8 DC Characteristics for Analog Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-voltage power	VGH	13	15	16	V	PVDD=3.3V
Negative High-voltage power	VGL	-11	-10	-7	V	PVDD=3.3V
Output Voltage Deviation	Vod		±35	±45	mV	
Standby Current	Isc			50	uA	VDD=PVDD=3.3V
Operation Current	Ioc		20		mA	No Load, VDD=VDDI=PVDD=3.3V @ FR=60Hz

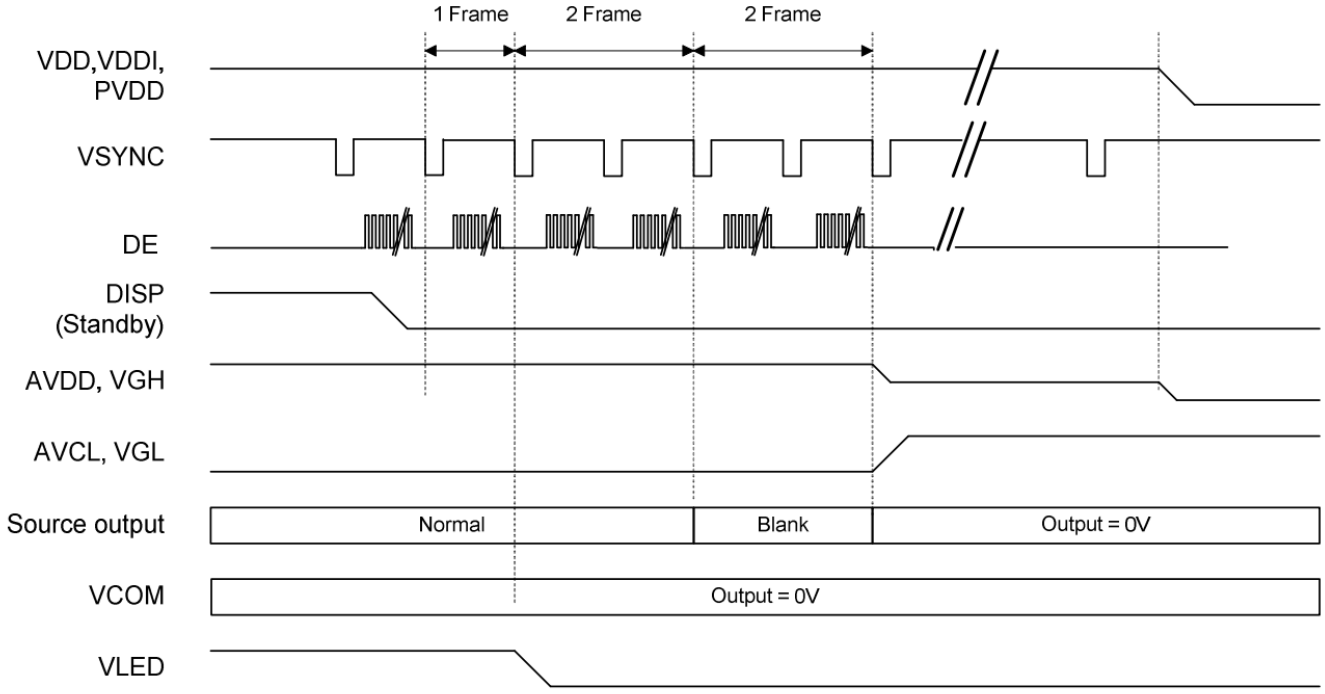
6. Power On/Off Sequence

6.1 Power On sequence



	Description	Min. Time
T0	Determined by the external power	
T1	Time from stable VDD, VDDI, PVDD set-up to the first VSYNC	T1=0
T2	Time from AVDD=0V to AVDD=3.3V	T2=T0
T3	Time from AVDD=3.3V to AVDD=6.0V	T3=T1+ (1*Frame)
T4	Time from stable VDD, VDDI, PVDD set-up to DISP asserted	T4=0
T5	Time from VGH=0V to VGH=3.3V	T5=T0

6.2 Power Off sequence



7. Optical Characteristics

Item	Symbol		Condition	Min	Type	Max	Uint
Transmittance	Tr		-	-	6.85	-	%
Contrast Ratio	CR			500	700	-	-
Response time	tr+tf			-	20	30	ms
Viewing Angle	Top		CR≧10	50	60	-	Deg.
	Bottom			60	70		
	Left			70	80		
	Right			70	80		
Color of CIE Coordinate	W	x	θ=0° Φ=0°	Typ -0.03	0.301	Typ +0.03	
		y			0.337		
	R	x			0.605		
		y			0.324		
	G	x			0.303		
		y			0.562		
	B	x			0.144		
		y			0.172		

8. RELIABILITY TEST

8-1 Temperature and Humidity

TEST ITEMS	CONDITIONS	NOTE
High Temperature Operation	70℃ ; 48hrs	
High Temperature Storage	80℃ ; 96hrs	
High Temperature High Humidity Operation	60℃; 90%RH ; 48hrs (No condensation)	
Low Temperature Operation	-20℃ ; 48hrs	
Low Temperature Storage	-30℃ ; 96hrs	
Thermal Shock	-20℃ (0.5hr) ~ 70℃ (0.5hr) ; 10 Cycles	Non-Operating
ESD Test (Non-operation)	150pF,330Ω， Contact±4KV,Air :±8KV.Note 1	
	200pF,0Ω， ±200V Contact test.Note 2	

Note:Measure Point:

1.LCD glass and metal bezel

2.IF connector pins

- END -