

Version :1.0

<p style="text-align: center;"><b>TECHNICAL SPECIFICATION</b></p> <p style="text-align: center;"><b>MODEL NO : PM090WY2</b></p>
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Please contact PVI or its agent for further information.

Customer's Confirmation

Customer \_\_\_\_\_

Date \_\_\_\_\_

By \_\_\_\_\_

PVI's Confirmation

Confirmed By Frank Shm

Prepared By 任欣蒙

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***Revision History***

<b>Rev.</b>	<b>Eng.</b>	<b>Date</b>	<b>Revised</b>	<b>Contents</b>
1.0	Tim Jen	Apr. 22, 2010	New	

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# ***TECHNICAL SPECIFICATION***

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1. Application

This data sheet applies to a color TFT LCD module, PM090WY2.

If you use in severe reliability environment, please don't extend over PVI's reliability test conditions.

If you use PM090WY2, Prime View advises to use PVI's timing controller IC (PVI-2003A) on your system which will generate proper timing signals to control PM090WY2.

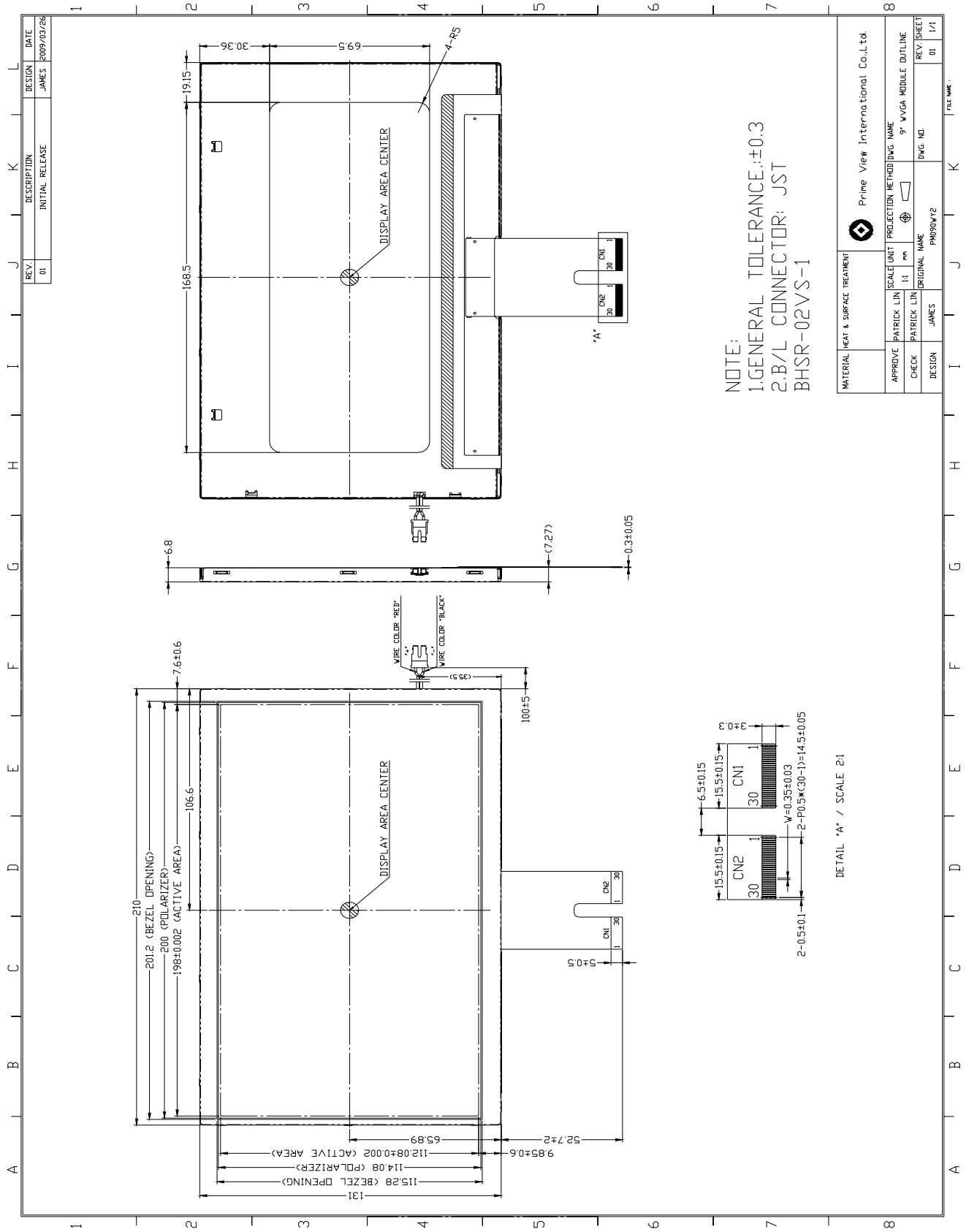
2. Features

- . Pixel in stripe configuration
- . Display Colors : 262K colors
- . Optimum Viewing Direction : 6 o'clock
- . WVGA (800 x 480 pixels) resolution

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	9" (Diagonal)	inch
Display Format	800x(R, G, B)x480	dot
Display Colors	262K	
Active Area	198 (H)x112.08(V)	mm
Pixel Pitch	0.2475(H)x0.2335(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	210(W)x131(H)x6.8 (typ.) (D) 210(W)x131(H)x7.27 (FPC side) (D)	mm
Weight	268±15	g
Back-light	42-LED	
Surface treatment	AG + WV	
Display mode	Normally white	
Gray scale inversion direction	6 o'clock	Note 13-1

4. Mechanical Drawing of TFT-LCD Module



NOTE:  
 1. GENERAL TOLERANCE: ±0.3  
 2. B/L CONNECTOR: JST  
 BHSR-02VS-1

MATERIAL HEAT & SURFACE TREATMENT		Prime View International Co., Ltd.	
APPROVE	PATRICK LIN	SCALE UNIT	PROJECTION METHOD DWG. NAME
CHECK	PATRICK LIN	1:1	9" W/VGA MODULE OUTLINE
DESIGN	JAMES	ORIGINAL NAME	DWG. NO.
		PM090WY2	REV. SHEET
			01 / 1

DETAIL "A" / SCALE 2:1

**5. Input / Output Terminals**
**5-1) TFT-LCD Panel Driving**
**CN1**

Pin No.	Symbol	I/O	Function	Remark
1	DIO1	I	Horizontal Start Pulse Signal Input	
2	VSS1	I	Ground	
3	VDD1	I	Power Supply	Note 5 - 10
4	CLK	I	Horizontal Shift Clock	Note 5 - 4
5	VSS1	I	Ground	
6	NC	-	NC	
7	R0	I	Red Data (LSB)	
8	R1	I	Red Data	
9	R2	I	Red Data	
10	R3	I	Red Data	
11	R4	I	Red Data	
12	R5	I	Red Data (MSB)	
13	VSS1	I	Ground	
14	G0	I	Green Data (LSB)	
15	G1	I	Green Data	
16	G2	I	Green Data	
17	G3	I	Green Data	
18	G4	I	Green Data	
19	G5	I	Green Data (MSB)	
20	VSS1	I	Ground	
21	B0	I	Blue Data (LSB)	
22	B1	I	Blue Data	
23	B2	I	Blue Data	
24	B3	I	Blue Data	
25	B4	I	Blue Data	
26	B5	I	Blue Data (MSB)	
27	LD	I	Load output signal	Note 5 - 6
28	REV	I	Data invert control	Note 5 - 7
29	POL	I	Polarity selection	Note 5 - 8
30	DIO2	O	Horizontal Start Pulse Signal Output	

**CN2**

Pin No.	Symbol	I/O	Function	Remark
1	VSS2	I	Ground	
2	V1	I	Gamma Voltage 1	Note 5 - 11
3	V2	I	Gamma Voltage 2	
4	V3	I	Gamma Voltage 3	
5	V4	I	Gamma Voltage 4	
6	V5	I	Gamma Voltage 5	
7	V6	I	Gamma Voltage 6	
8	V7	I	Gamma Voltage 7	
9	VSS2	I	Ground	
10	V8	I	Gamma Voltage 8	Note 5 - 11
11	V9	I	Gamma Voltage 9	
12	V10	I	Gamma Voltage 10	
13	V11	I	Gamma Voltage 11	
14	V12	I	Gamma Voltage 12	
15	V13	I	Gamma Voltage 13	
16	V14	I	Gamma Voltage 14	
17	VSS2	I	Ground	
18	VDD2	I	Voltage for analog circuit	Note 5 - 11
19	VCOM	I	Common Voltage	
20	NC	-	NC	
21	OE	I	Output Enable	Note 5 - 5
22	U/D	I	Up / Down Selection	Note 5 - 3
23	CKV	I	Vertical Shift Clock	Note 5 - 6
24	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note 5 - 3
25	STVD	I/O	Vertical Shift Pulse Signal Input or Output	Note 5 - 3
26	VGG	I	Gate On Voltage	Note 5 - 2
27	GND	I	Ground	
28	VCC	I	Voltage for logic circuit	Note 5 - 9
29	GND	I	Ground	
30	VEE	I	Gate Off Voltage	Note 5 - 1

Note 5 - 1 : Gate off voltage,  $V_{EE(TYP.)} = -6.3\text{ V}$

Note 5 - 2 : Gate on voltage,  $V_{GG(TYP.)} = +18.6\text{ V}$

Note 5 - 3 : Select up or down shift

U/D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down

Note 5 - 4 : Gate driver shift clock

Note 5 - 5 : When OE is connected to high "1", the driver outputs are disabled (Gate output = VEE). Under this condition, the operation of registers will not be affected.

Note 5 - 6 : Latch the polarity of outputs and switch the new data to outputs. At the rising edge (LD), latch the "POL" signal to control the polarity of the outputs.

Note 5 - 7 : Control whether the Data R0~G5 are inverted or not. (PVI suggests connecting to GND)  
When "REV=1", these data will be inverted.  
EX: "00"→"3F", "07"→"38", "15"→"2A"

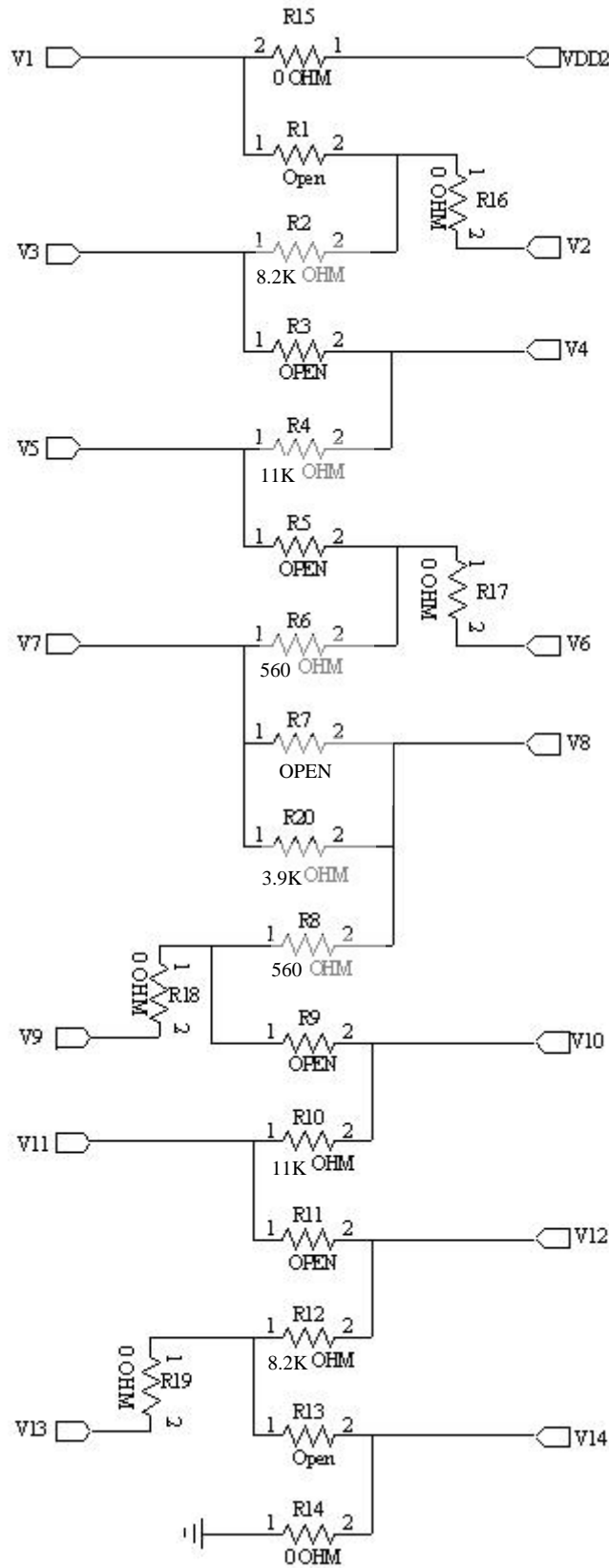
Note 5 - 8 : Polarity selector for dot-inversion control. Available at the rising edge of LD.  
When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14;  
When POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 5 - 9 :  $V_{CC(TYP.)} = 3.3\text{ V}$

Note 5 - 10 :  $V_{DD1(TYP.)} = 3.3\text{ V}$



Note 5 - 11 : Typical Application Circuit (When VDD2 (TYP.) = +9.9 V)



## 5-2) Backlight driving

Connector type: JST BHSR-02VS-1

PIN NO.	Symbol	Description	Remark
1	+	Input terminal (Anode)	Red
2	-	Input terminal (Cathode)	Black

## 6. Absolute Maximum Ratings:

 $V_{ss1}=V_{ss2}=GND=0V, T_a=25^{\circ}C$ 

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	VDD1	-0.5	5.0	V	
	VDD2	-0.5	13.5	V	
	VCC	-0.3	6.0	V	
	VGG	-0.3	40	V	
	VEE	-20	0.3	V	
	VGG-VEE	-0.3	40	V	
Operating Temperature	Top	-30	+85	$^{\circ}C$	
Storage Temperature	Tst	-40	+95	$^{\circ}C$	

## 7. Electrical Characteristics

## 7-1) Recommended Operating Conditions

 $V_{ss1}=V_{ss2}=GND=0V, T_a=25^{\circ}C$ 

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	VDD1	3	3.3	3.6	V	
	VDD2	8.9	9.9	10.9	V	
Supply Voltage for Gate Driver	VCC	3	3.3	3.6	V	
	VGG	16.6	18.6	20.6	V	
	VEE	-7.3	-6.3	-5.3	V	
V <sub>COM</sub> Voltage	VCOM	-	4.1	-	V	
Digital Input Voltage	VIH	0.7VDD1	-	VDD1	V	
	VIL	0	-	0.3VDD1	V	

## 7-2) Recommended driving condition for LED back light

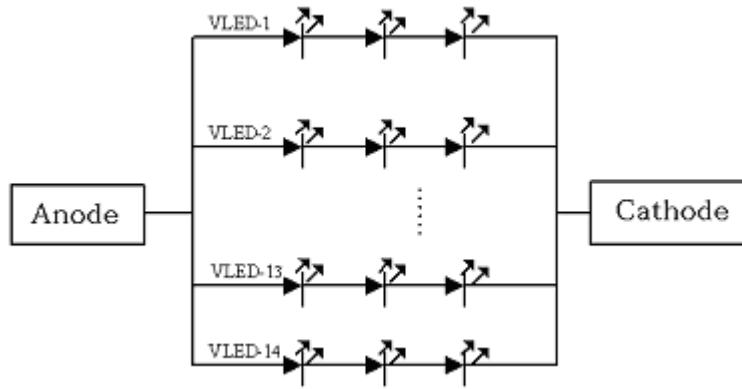
 $T_a=25^{\circ}C$ 

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V <sub>LED</sub>	-	-	(10.5)	V	Note 7 - 1
Supply current of LED backlight	I <sub>LED</sub>	-	15	-	mA	Note 7 - 2
Backlight Power Consumption	P <sub>LED</sub>	-	-	2.21	W	Note 7 - 1/ Note 7 - 3

 Note 7 - 1: I<sub>LED</sub>= 15mA, constant current

 Note 7 - 2: The LED driving condition is defined for each LED module. (3 LED Serial)  
 Input current = 15mA \* 14 = 210mA

 Note 7 - 3:  $P_{LED} = V_{LED-1} * I_{LED-1} + V_{LED-2} * I_{LED-2} \dots + V_{LED-13} * I_{LED-13} + V_{LED-14} * I_{LED-14}$

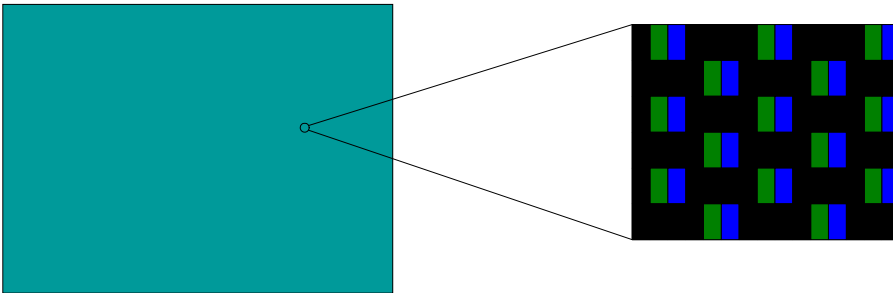


7-3) Power Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	IGG	VGG= 18.6 V	0.2	0.6	mA	Note 7 - 5
Supply Current for Gate Driver (Low level)	IEE	VEE= -6.3 V	0.2	0.6	mA	Note 7 - 5
Supply Current for Gate Driver (Digital)	ICC	VCC= +3.3V	0.1	0.3	mA	Note 7 - 5
Supply Current for Source Driver (Digital)	IDD1	VDD1= +3.3V	5.0	10.0	mA	Note 7 - 5
Supply Current for Source Driver (Analog)	IDD2	VDD2= 9.9 V	23.1	46.2	mA	Note 7 - 5
LCD Panel Power Consumption	-	-	253.2	504.5	mW	Note 7 - 4

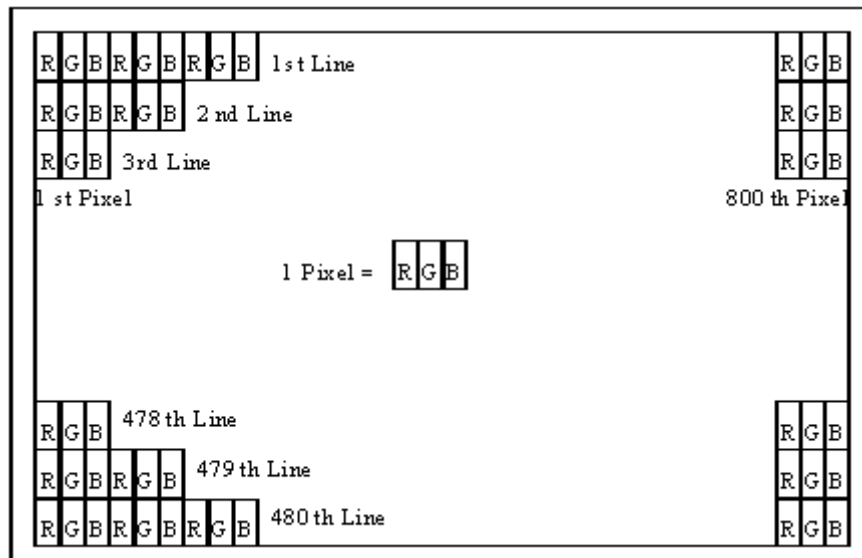
Note 7 - 4: The power consumption for back light is not included.

Note 7 - 5: Test Pattern for dissipative current.



8. Pixel Arrangement

The LCD module pixel arrangement is the stripe.

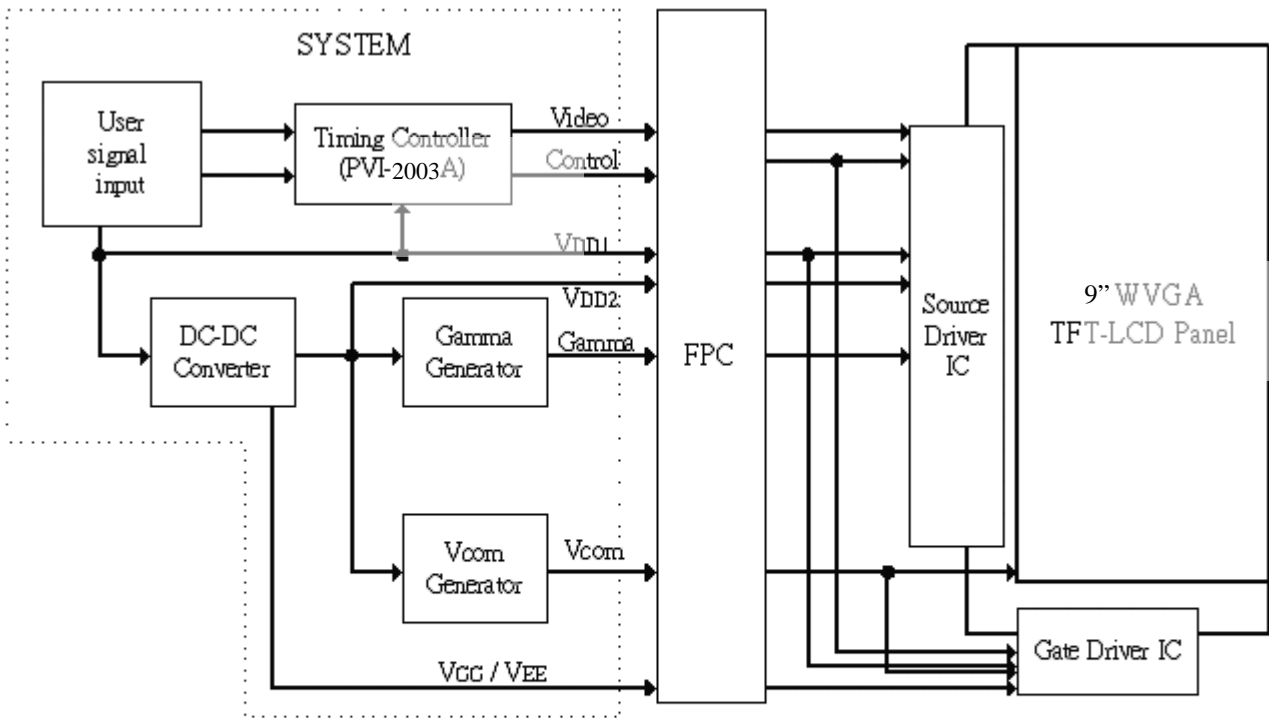


9. Display Color and Gray Scale Reference

Color		Input Color Data																	
		Red					Green						Blue						
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0		
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (01)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	
	Green (02)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	
Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0		
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

10. Block Diagram

10-1) TFT-module Block Diagram



If you use PM090WY2 , you can apply PVI-2003A (Timing controller) which will generate timing signals to support PM090WY2 .

## 11. Interface Timing

## 11-1) Timing Parameters

AC Electrical Characteristics ( $V_{CC}=V_{DD1}=3.3V$ ,  $V_{DD2}=9.9V$ ,  $GND=0V$ ,  $T_a=25^{\circ}C$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency	Fclk	-	32	40	MHz
CLK Pulse Width	Tcw	25	-	-	ns
Data Set-up Time	Tsu	4	-	-	ns
Data Hold Time	Thd	2	-	-	ns
Propagation Delay of DIO2/1	Tphl	6	10	15	ns
Time That The Last Data to LD	Tld	1	-	-	Tcw
Pulse width of LD	Twld	2	-	-	Tcw
Time That LD to DIO1/2	Tlds	5	-	-	Tcw
POL Set-up Time	Tpsu	6	-	-	ns
POL Hold Time	Tphd	6	-	-	ns
OE Pulse Width	T <sub>OE</sub> V	1	-	-	μs
CKV Pulse Width	T <sub>CKV</sub>	500	-	-	ns
STV Set-up Time	T <sub>SUV</sub>	400	-	-	ns
STV Hold Time	T <sub>H<sub>DV</sub></sub>	400	-	-	ns
Horizontal Display Period	T <sub>HDP</sub>	-	800	-	Tcw
Horizontal Period Timing Range	T <sub>HP</sub>	-	1056	-	Tcw
Horizontal Lines Per Field	T <sub>V</sub>	484	508	620	T <sub>HP</sub>
Vertical Display Timing Range	T <sub>DV</sub>	-	480	-	T <sub>HP</sub>

11-2) Timing Diagram

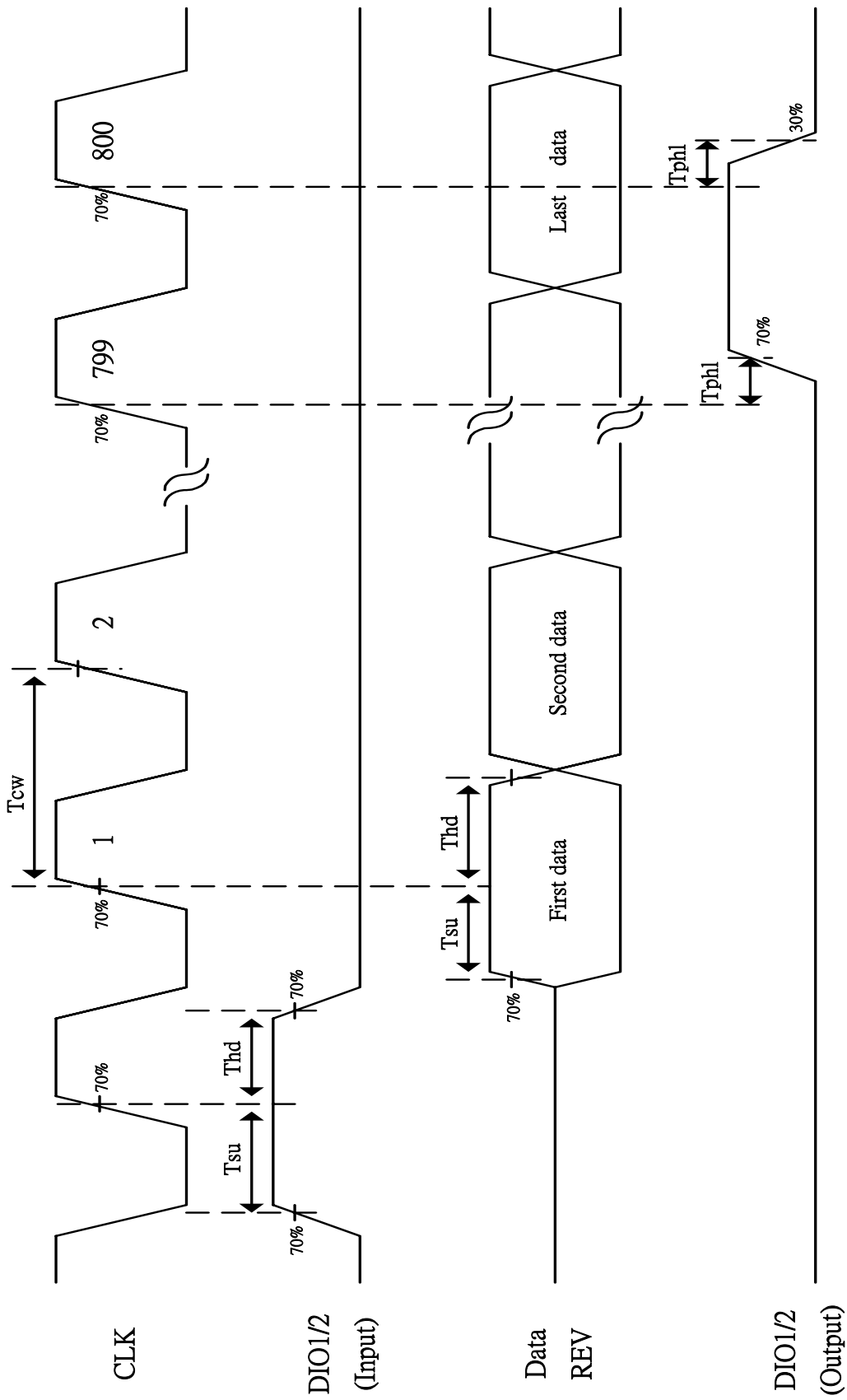


Fig. 11-1 Horizontal timing (1)



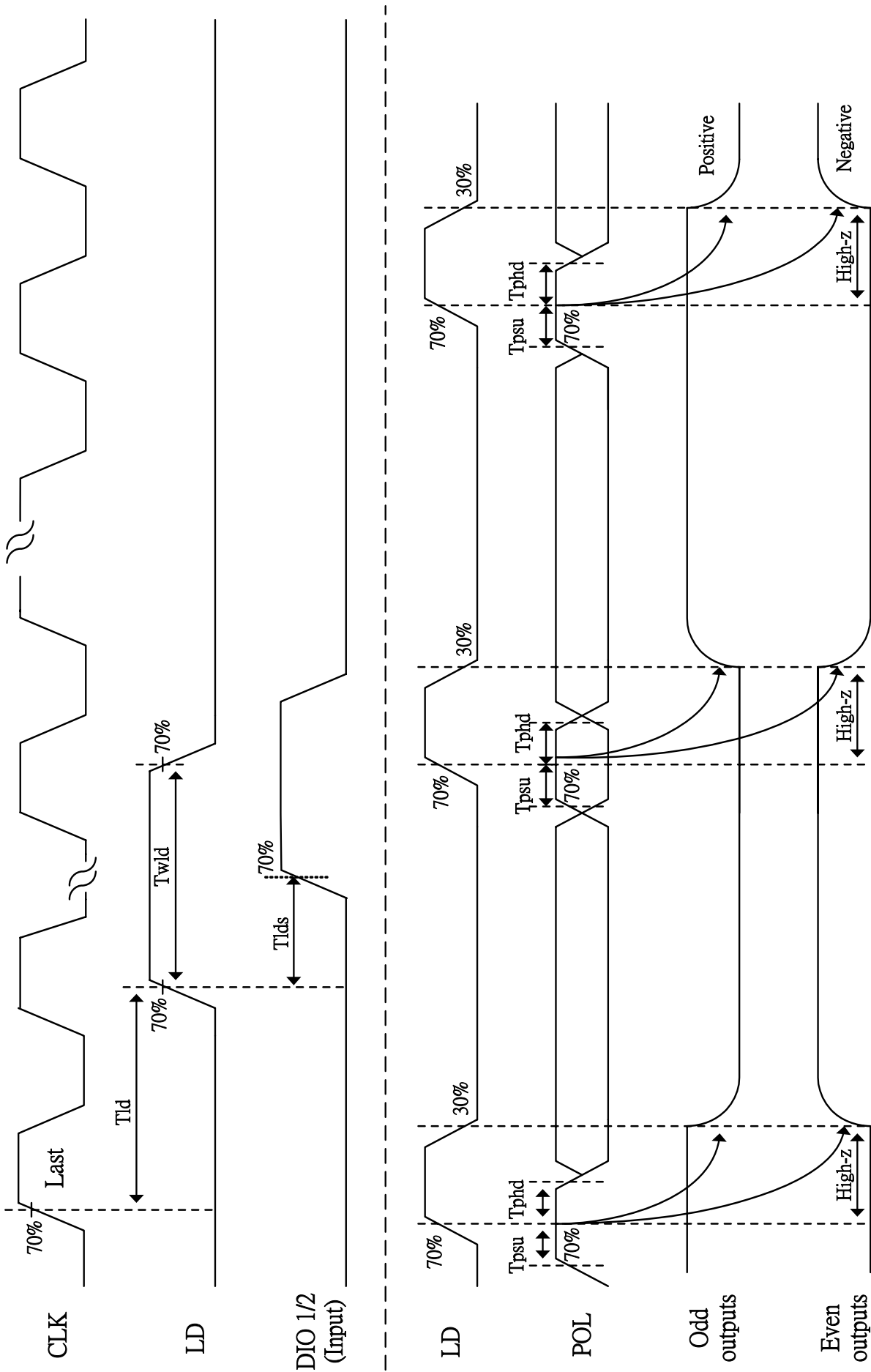


Fig. 11-2 Horizontal timing(2)

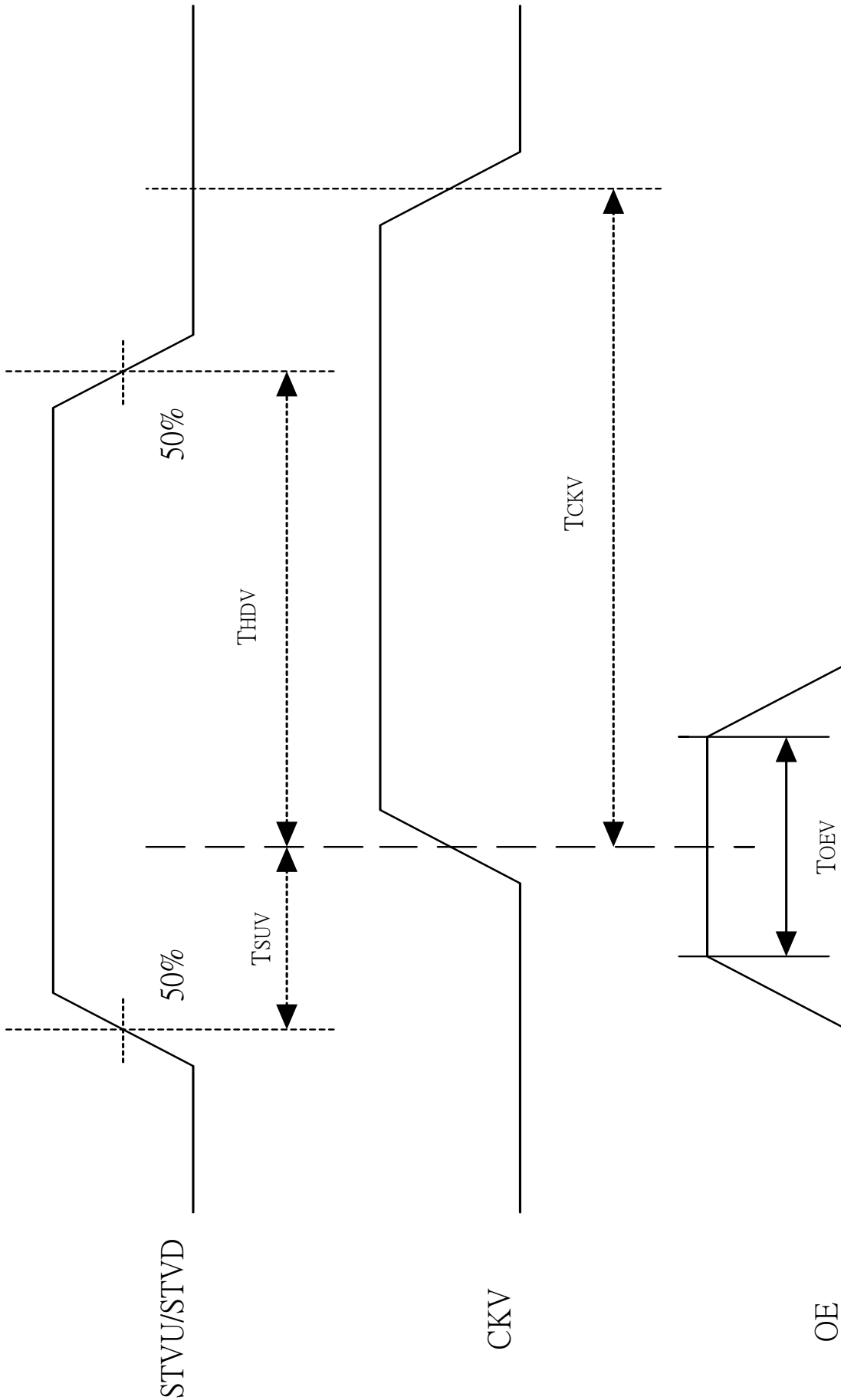


Fig. 11-3 Vertical shift clock timing

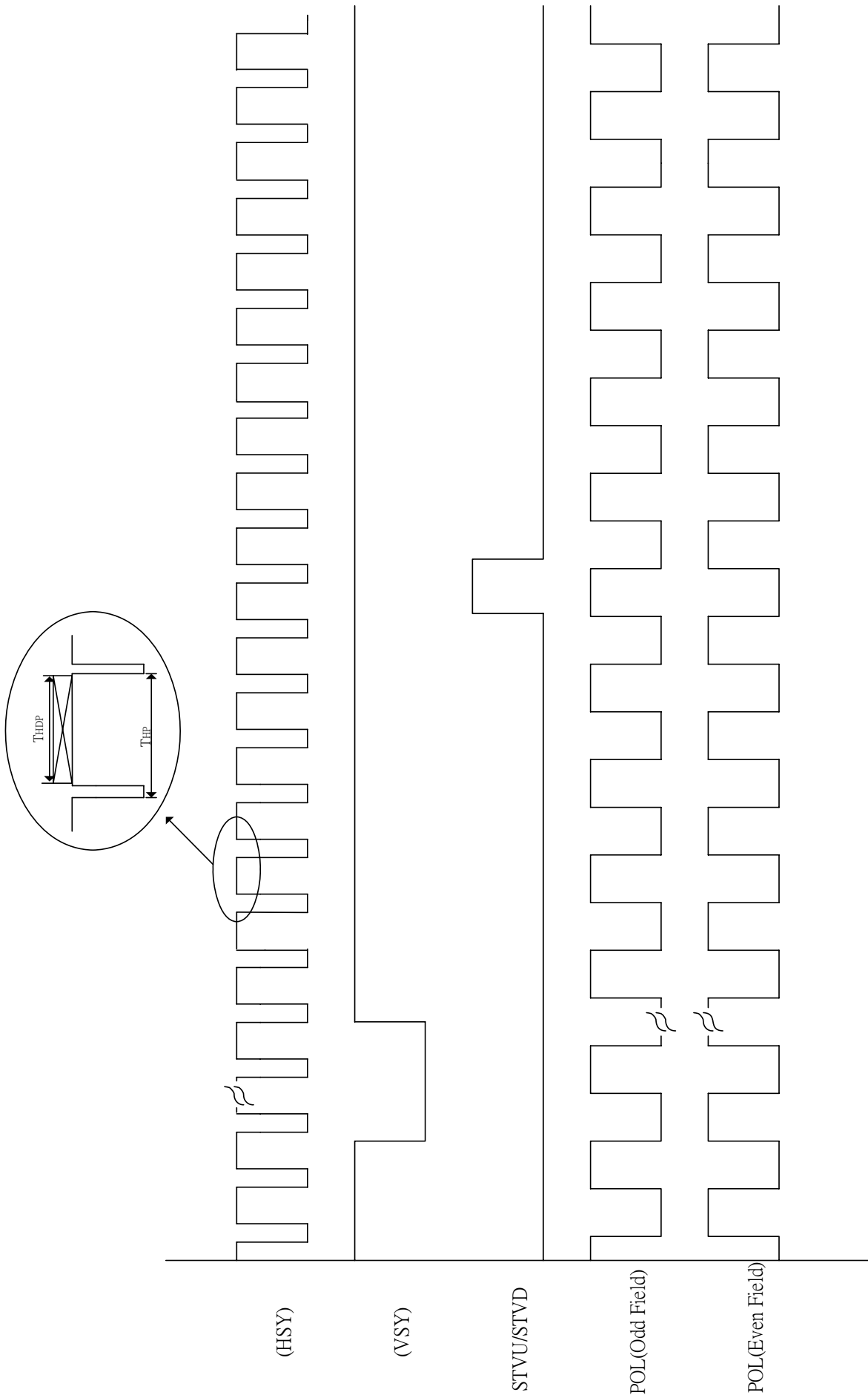


Fig. 11-4 Vertical timing

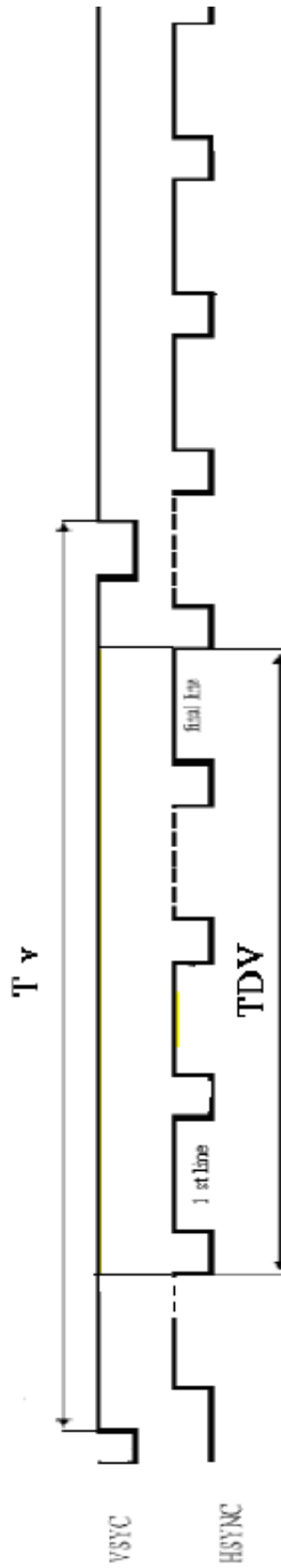
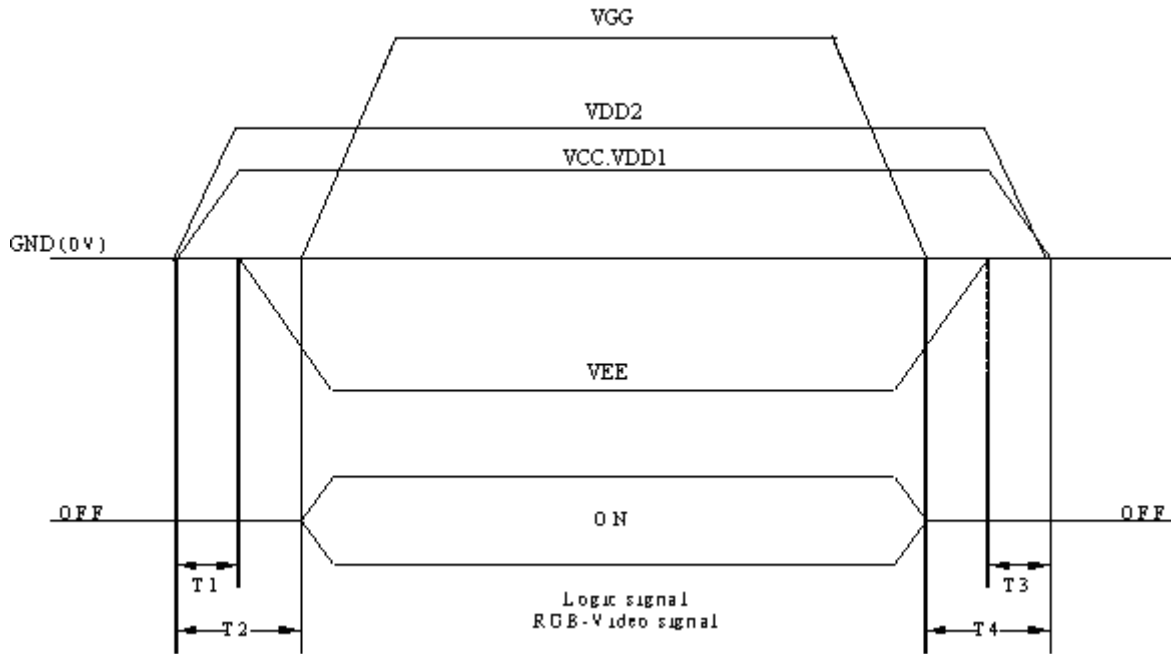


Fig 11-5 VSYNC,H SYNC relationship

12. Power On Sequence



1.  $10\text{ms} \leq T1 < T2$
2.  $0\text{ms} < T3 \leq T4 \leq 10\text{ms}$

13. Optical Characteristics

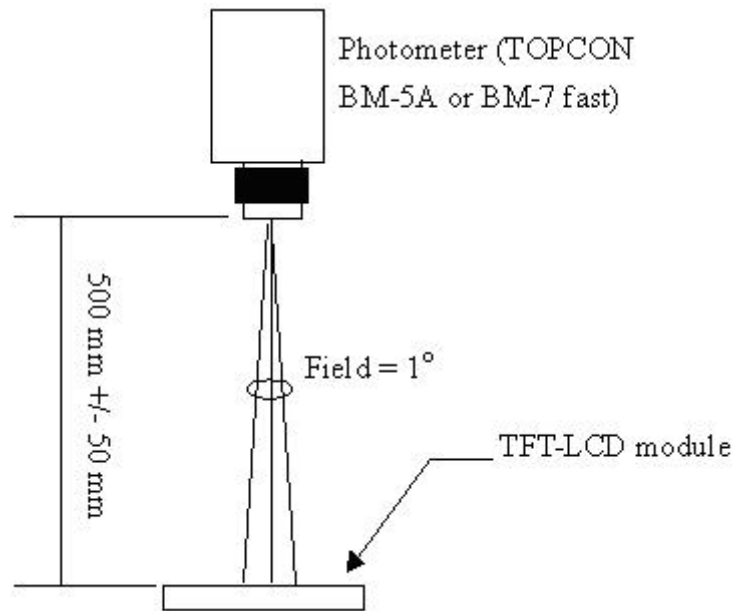
13-1) Specification:

Ta=25°C

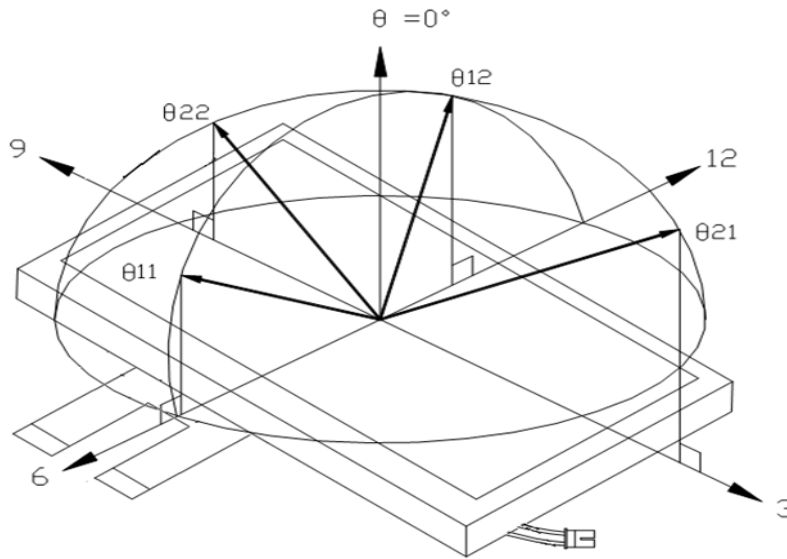
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	$\theta_{22.21}$	65	70	-	deg	Note 13-1
	Vertical	$\theta_{12}$	45	50	-	deg	
		$\theta_{11}$	45	50	-	deg	
Contrast Ratio	CR	At Optimized Viewing Angle	600	750	-	-	Note 13-2
Response time	Rise	$T_r$	-	5	10	ms	Note 13-3
	Fall	$T_f$	-	20	40	ms	
Brightness	L	$\theta=0^\circ/\varphi=0$	400	500	-	cd/m <sup>2</sup>	
LED Life Time		+25°C	20000	--	-	hrs	Note 13-4
Luminance Uniformity	U	-	75	80	-	%	Note 13-5
White Chromaticity	x	-	0.255	0.295	0.335	-	
	y	-	0.280	0.320	0.360	-	
Cross Talk	CTK	$\theta=0^\circ/\varphi=0$	-	-	3.5	%	Note 13-6

## PM090WY2

All the optical measurement shall be executed 30 minutes after backlight being turn-on. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.

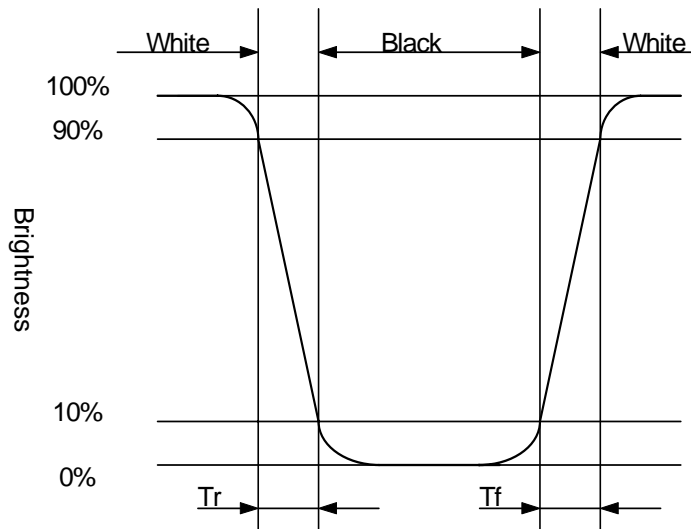


Note 13-1: The definitions of viewing angles are as follow



Note 13-2 :  $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

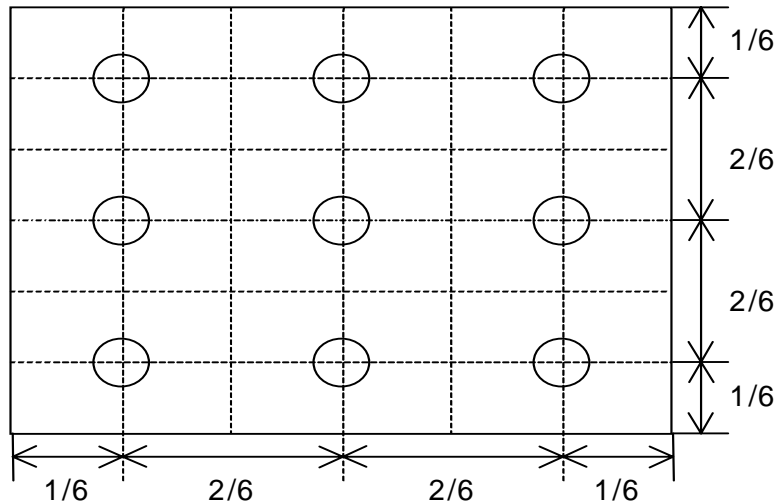
Note 13-3: Definition of Response Time  $T_r$  and  $T_f$



Note 13-4: The “LED Life time “is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25°C and  $I_{LED} = 210mA$

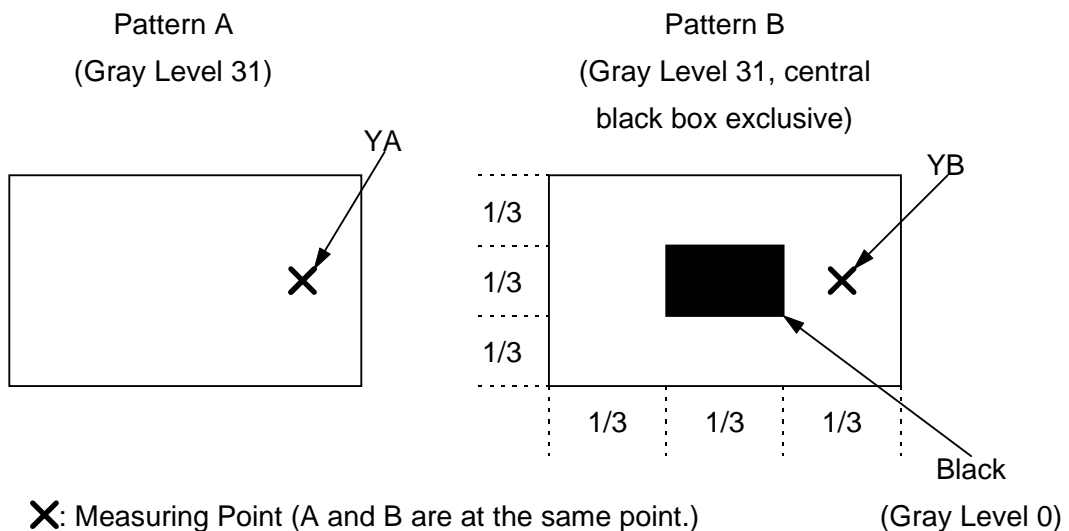
Note 13-5: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$
 Luminance meter: BM-5A or BM-7 fast (TOPCON)  
 Measurement distance: 500 mm +/- 50 mm  
 Ambient illumination: < 1 Lux  
 Measuring direction: Perpendicular to the surface of module  
 The test pattern is white.



Note 13-6: Cross Talk (CTK) =  $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A  
 YB: Brightness of Pattern B  
 Luminance meter: BM 5A or BM-7 fast (TOPCON)  
 Measurement distance: 500 mm +/- 50 mm  
 Ambient illumination: < 1 Lux  
 Measuring direction: Perpendicular to the surface of module





**14. Handling Cautions**

**14-1) Mounting of module**

- a) Please power off the module when you connect the input/output connector.
- b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- c) Protective film (Laminator) is applied on surface to protect it against scratches and dirt's.
- d) Please following the tear off direction as figure 14-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

**14-2) Precautions in mounting**

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

**14-3) Adjusting module**

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

**14-4) Others**

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

**14-5) Polarizer mark**

The polarizer mark is to describe the direction of wide view angle film how to match up with the rubbing direction.

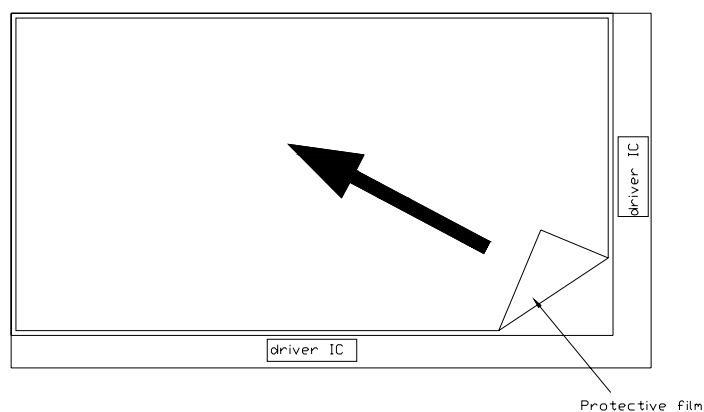


Figure 14-1 the way to peel off protective film

## 15. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +95°C, 240 hrs
2	Low Temperature Storage Test	Ta = -40°C, 240 hrs
3	High Temperature Operation Test	Ta = +85°C, 240 hrs
4	Low Temperature Operation Test	Ta = -30°C, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60°C, 90%RH, 240 hrs (No Condensation)
6	Thermal Shock Test (non-operating)	-30°C → +80°C, 200 Cycles 30min 30min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz Amplitude : 1 mm Sweep time : 11 min Test Period : 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction : ±X, ±Y, ±Z Cycle : 3 times
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time/each terminal

Ta: ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (Including: line defect, no image). All the cosmetic specification is judged before the reliability stress.

16. Packing Diagram

