PRIME VIEW

PD057VX3

Version : 3.0

TECHNICAL SPECIFICATION

MODEL NO. : PD057VX3

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Please contact PVI or its agent for further information.

☐Customer' s Confirmation

Customer _____

Date _____

By _____

☐PVI' s Confirmation

Confirmed By Tommy Chang

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Revision History

Rev.	Issued Date	Revised Contents
1.0	Sep.7, 2007	New
2.0	Aug. 11, 2008	Add Page 29 16.Handling Cautions d) items of 16-1
3.0	May. 04, 2009	Follow ECN200904020 的生效結果 變更 4. Mechanical Drawing of TFT-LCD Module

TECHNICAL SPECIFICATION

CONTENTS

1. Application :

This data sheet applies to a color TFT LCD module, PD057VX3.
PD057VX3 module applies to OA product, car TV (must use Analog to Digital driving board), which requires high quality flat panel display. If you must use in severe reliability environment, please don't extend over PVI's reliability test conditions.

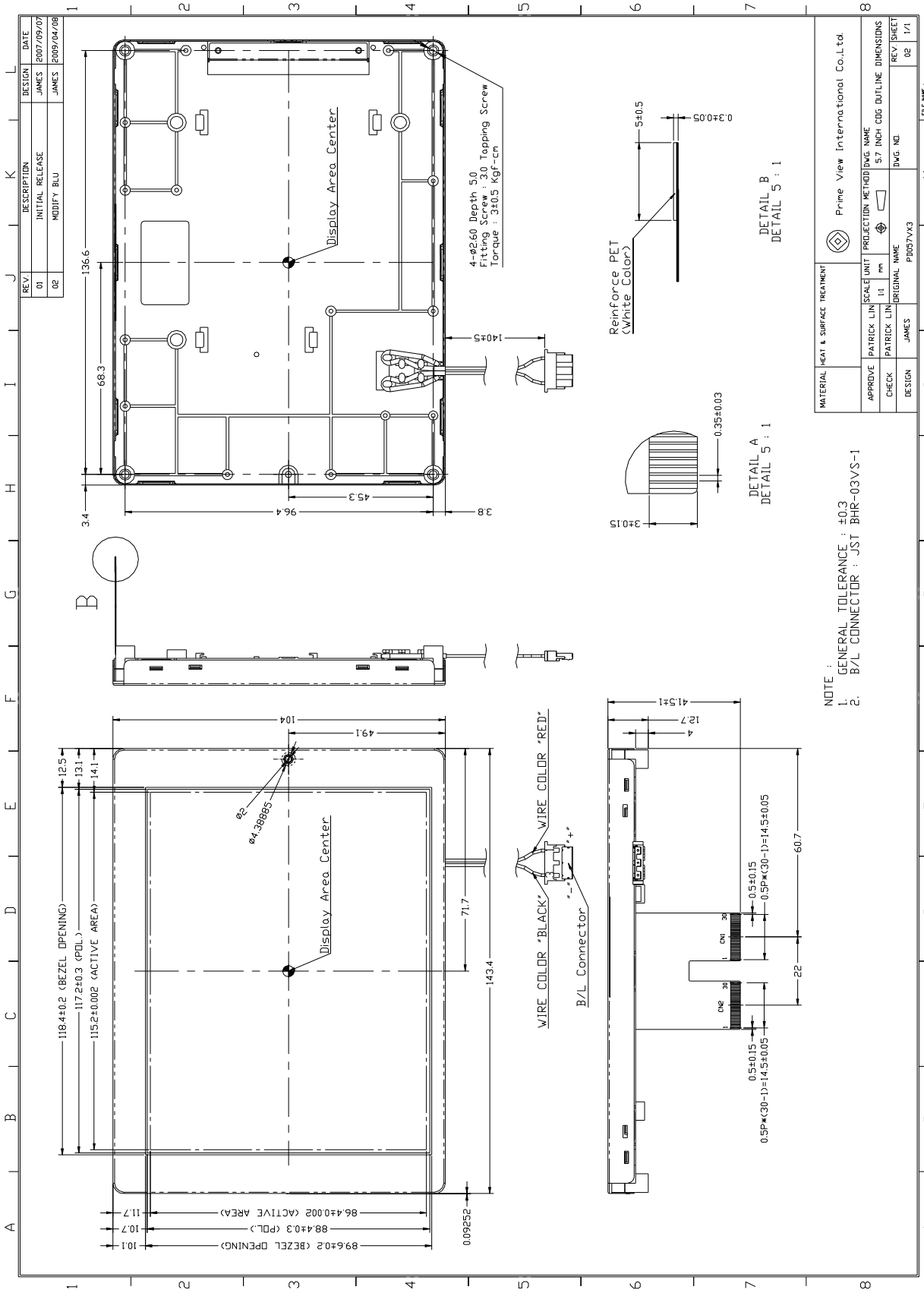
2. Features :

. VGA (640*480 pixels) resolution
. Amorphous silicon TFT LCD panel with LED back-light unit
. Pixel in stripe configuration
. Thin and light weight
. Display Colors : 16.7M colors

3. Mechanical Specifications :

Parameter	Specifications	Unit
Screen Size	5.7 (diagonal)	inch
Display Format	640×(R,G,B)×480	dot
Display Colors	16.7M	
Active Area	115.20 (H)×86.4 (V)	mm
Pixel Pitch	0.18(H)×0.18(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	143.4 (W)×104 (H)×12.7 (D) (typ.)	mm
Weight	160±10	g
Back-light	36-LED	
Surface treatment	Anti-glare + EWV film	
Display mode	Normally white	
Gray scale inversion direction	6 o' clock [ref to Note 15-1]	

4. Mechanical Drawing of TFT-LCD Module：



5. Input / Output Terminals :

5-1) TFT-LCD Panel Driving :

FPC Down Connect, 30 Pins, Pitch: 0.5 mm

CN 1

Pin No.	Symbol	Function	Remark
1	D27(B7)	Blue Data	Note 5-1
2	D26(B6)	Blue Data	
3	D25(B5)	Blue Data	
4	D24(B4)	Blue Data	
5	D23(B3)	Blue Data	
6	D22(B2)	Blue Data	
7	D21(B1)	Blue Data	
8	D20(B0)	Blue Data	
9	GND	Digital ground	
10	D17(G7)	Green Data	Note 5-1
11	D16(G6)	Green Data	
12	D15(G5)	Green Data	
13	D14(G4)	Green Data	
14	D13(G3)	Green Data	
15	D12(G2)	Green Data	
16	D11(G1)	Green Data	
17	D10(G0)	Green Data	
18	GND	Digital ground	
19	D07(R7)	Red Data	Note 5-1
20	D06(R6)	Red Data	
21	D05(R5)	Red Data	
22	D04(R4)	Red Data	
23	D03(R3)	Red Data	
24	D02(R2)	Red Data	
25	D01(R1)	Red Data	
26	D00(R0)	Red Data	
27	GND	Digital ground	
28	VEE	Negative power for gate driver	Note 5-8
29	VCC2	Digital power supply for gate driver	Note 5-9
30	VGG	Positive power for gate driver	Note 5-10

CN2

Pin No.	Symbol	Function	Remark
1	VCOM	Voltage for common electrode	Note 5-7
2	VSET	Externally/Internally gamma voltage setup	Note 5-11
3	VDDA	Analog power supply for source driver	Note 5-2
4	V10	Gamma correction voltage 10	
5	V9	Gamma correction voltage 9	
6	V8	Gamma correction voltage 8	
7	V7	Gamma correction voltage 7	
8	V6	Gamma correction voltage 6	
9	V5	Gamma correction voltage 5	
10	V4	Gamma correction voltage 4	
11	V3	Gamma correction voltage 3	
12	V2	Gamma correction voltage 2	
13	V1	Gamma correction voltage 1	
14	VSSA	Analog ground for source drive	
15	FRP	Select normally white or normally black panel	Note 5-13
16	CS	Charge share function control	Note 5-14
17	STB	Standby mode control	Note 5-15
18	VSSA	Analog ground for source drive	
19	L/R	Left/Right control for source driver	Note 5-12
20	U/D	Up/Down control for gate driver	Note 5-12
21	GND	Digital ground	
22	VCC1	Digital power supply for source driver	Note 5-6
23	RESETB	Hardware global reset	
24	SPDA	Serial port data input/output	
25	SPCK	Serial port clock	
26	SPENA	Serial port data enable signal	
27	DEN	Input data enable control	Note 5-5
28	HS	Horizontal sync input	Note 5-3
29	VS	Vertical sync input	Note 5-4
30	CLK	Clock signal. Latching data at the rising edge	

Note 5-1 : Digital data input. DX0 is LSB and DX7 is MSB.
If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G and B data in turn.

Note 5-2 : VDDA Typ. = 8V

Note 5-3 : Horizontal sync input in digital RGB mode and CCIR601 mode.
(Short to GND if not used)

Note 5-4 : Vertical sync input in digital RGB mode and CCIR601 mode.
(Short to GND if not used)

Note 5-5 : The SYNC(HS+ VS) Mode and DEN mode are supported. If DEN signal is fixed low, SYNC Mode is used. Otherwise, DEN mode is used.

Note 5-6 : V_{CC1} Typ. = 3.3V

Note 5-7 : V_{COM} Typ.= 3.5V

Note 5-8 : V_{EE} Typ. = -7 V

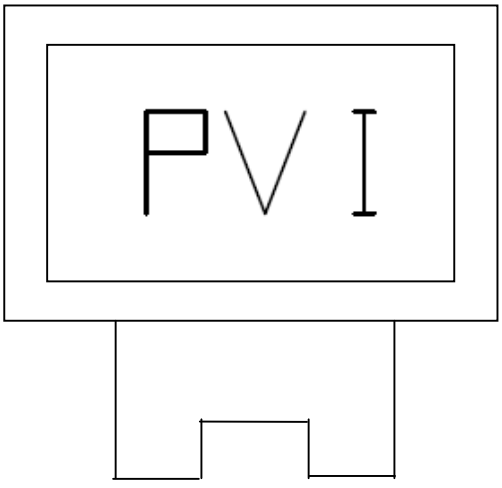
Note 5-9 : V_{CC2} Typ.= 3.3V

Note 5-10 : V_{GG} Typ. =17.6V

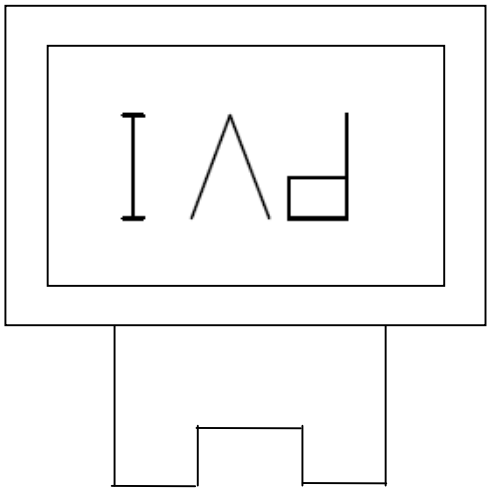
Note 5-11 : If. SET=" H" , the gamma correction voltage generated externally.

Note 5-12 : The definition of L/R , U/D

U/D CN2(PIN 20)=Low
L/R CN2(PIN 19)=High



U/D CN2(PIN 20)=High
L/R CN2(PIN 19)=Low

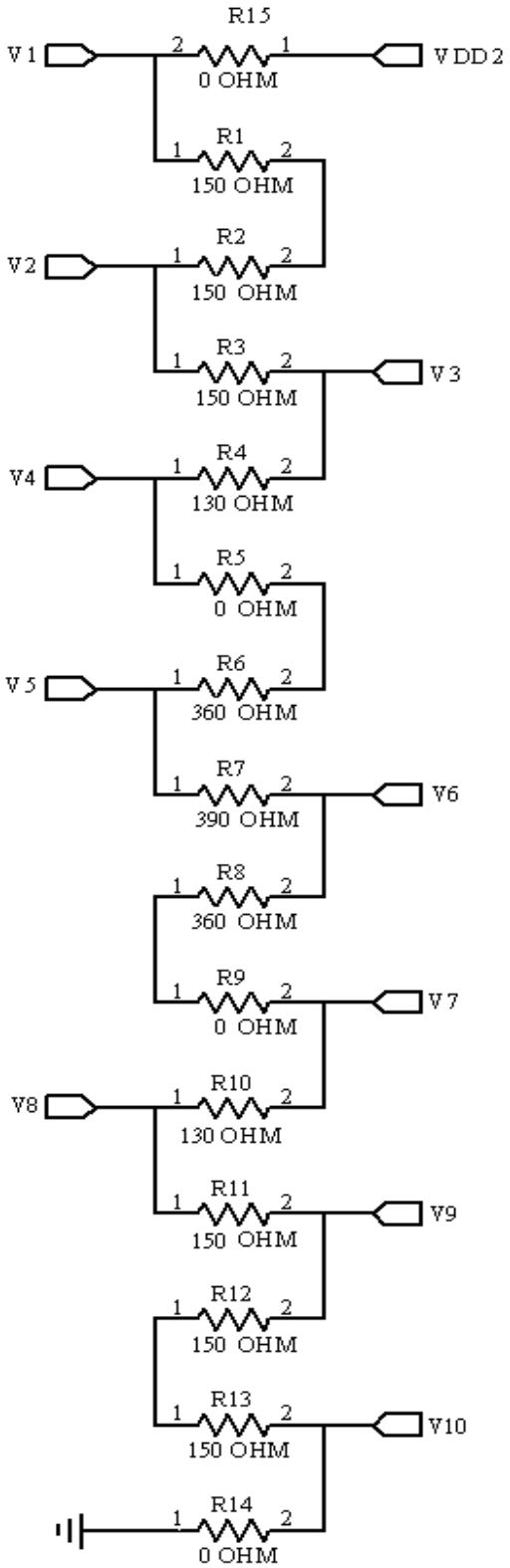


Note 5-13 : Default pull low:
FRP=L, pass the input data for normally white panel.
FRP=H, invert the input data for normally black panel.

Note 5-14 : Default pull high:
CS=L, disable charge share function.
CS=H, enable charge share function.

Note 5-15 : Default pull high:
STB=L, TCON and source drive are off.
STB=H, all the functions are on.

Typical Application Circuit (When VDDA = 8V)



5-2) LED Backlight driving :

Connector type: JST BHR-03VS-1, PIN No 3 pins, pitch=8.0mm

Pin No	Symbol	Description	Remark
1	+	Input terminal (Anode)	Wire color : Red
2	NC	NC	-
3	-	Input terminal (Cathode)	Wire color : Black

6. Absolute Maximum Ratings :

VSSA=GND=0V, Ta=25℃

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	V_{CC2}	-0.3	6.0	V	
	V_{CC1}	-0.3	7.0	V	
	V_{DDA}	-0.3	13.5	V	
	V_{GG}	-0.3	40.0	V	
	V_{GG}-V_{EE}	-0.3	40.0	V	
	V_{EE}	-20	0.3	V	

7. Electrical Characteristics :

7-1) Recommended Operating Conditions :

VSSA=GND=0V, Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	V_{CC1}	2.7	3.3	3.6	V	
	V_{DDA}	-	8	-	V	
Supply Voltage for Gate Driver	V_{GG}	-	17.6	-	V	
	V_{EE}	-	-7	-	V	
	V_{CC2}	2.7	3.3	3.6	V	
VCOM Voltage	V_{COM}	-	3.5	-	V	
Digital Input Voltage	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	
	V_{IL}	0	-	0.3 V_{CC}	V	

7-2) Recommended Driving Condition for LED Back Light :

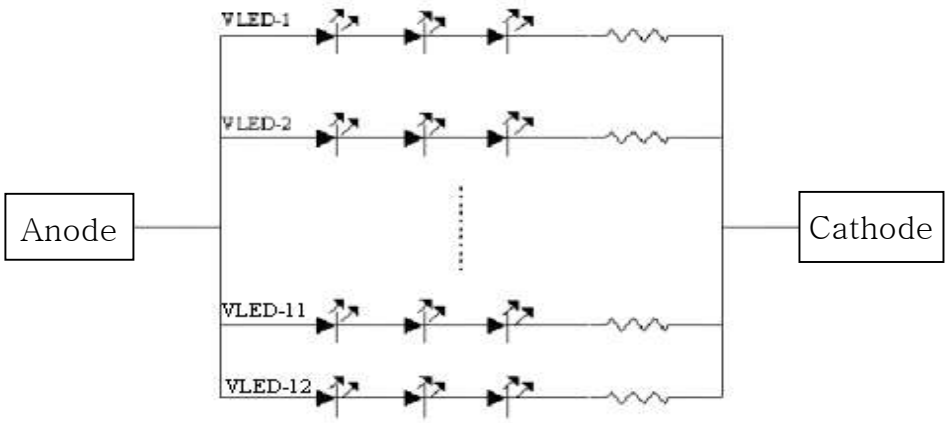
Ta=25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V_{LED}	-	-	(11)	V	Note 7-1
LED current	I_{LED}	-	20	-	mA	Note 7-2
Back Light Power Consumption	P_{LED}	-	-	2640	mW	Note 7-3

Note 7-1 : The I_{LED}=20 mA(Constant current).

Note 7-2 : The LED driving condition is defined for each LED module. (3 LED Series)
The input current= 20 mA*12=240 mA.

Note 7-3 : $P_{LED} = V_{LED-1} * I_{LED-1} + V_{LED-2} * I_{LED-2} \cdots + V_{LED-11} * I_{LED-11} + V_{LED-12} * I_{LED-12}$



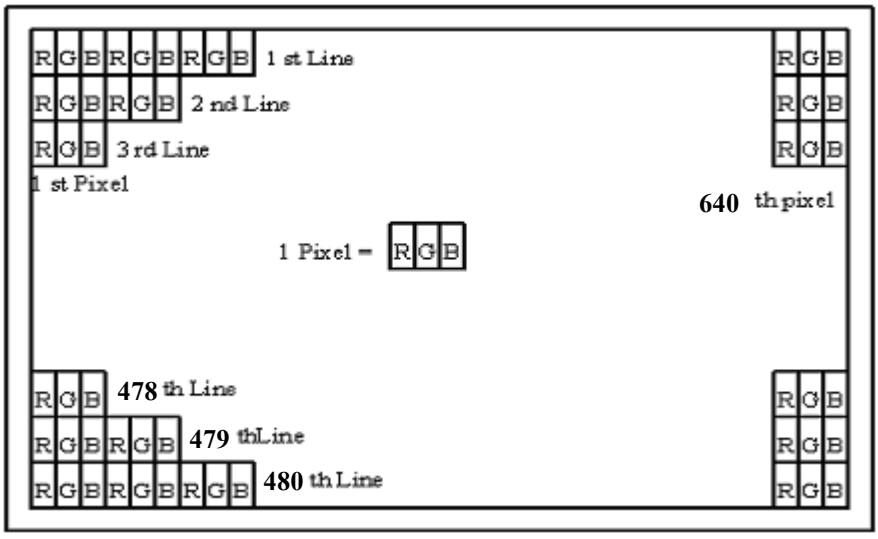
7-3) Power Consumption :

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	IGG	VGG= 17.6V	0.1	0.2	mA	
Supply Current for Gate Driver (Low level)	IEE	VEE= -7V	0.1	0.2	mA	
Supply Current for Source Driver (Digital)	ICC1	VCC1= 3.3V	0.92	2.76	mA	
Supply Current for Source Driver (Analog)	IDDA	VDDA= 8V	4.76	14.28	mA	
Supply Current for Gate Driver (Digital)	ICC2	VCC2= 3.3V	0.003	0.006	mA	
LCD Panel Power Consumption	-	-	0.484	0.606	W	Note 7-4
Total Power Consumption	-	-	-	3.25	W	

Note 7-4: The power consumption of backlight is not included.

8. Pixel Arrangement :

The LCD module pixel arrangement is stripe configuration.

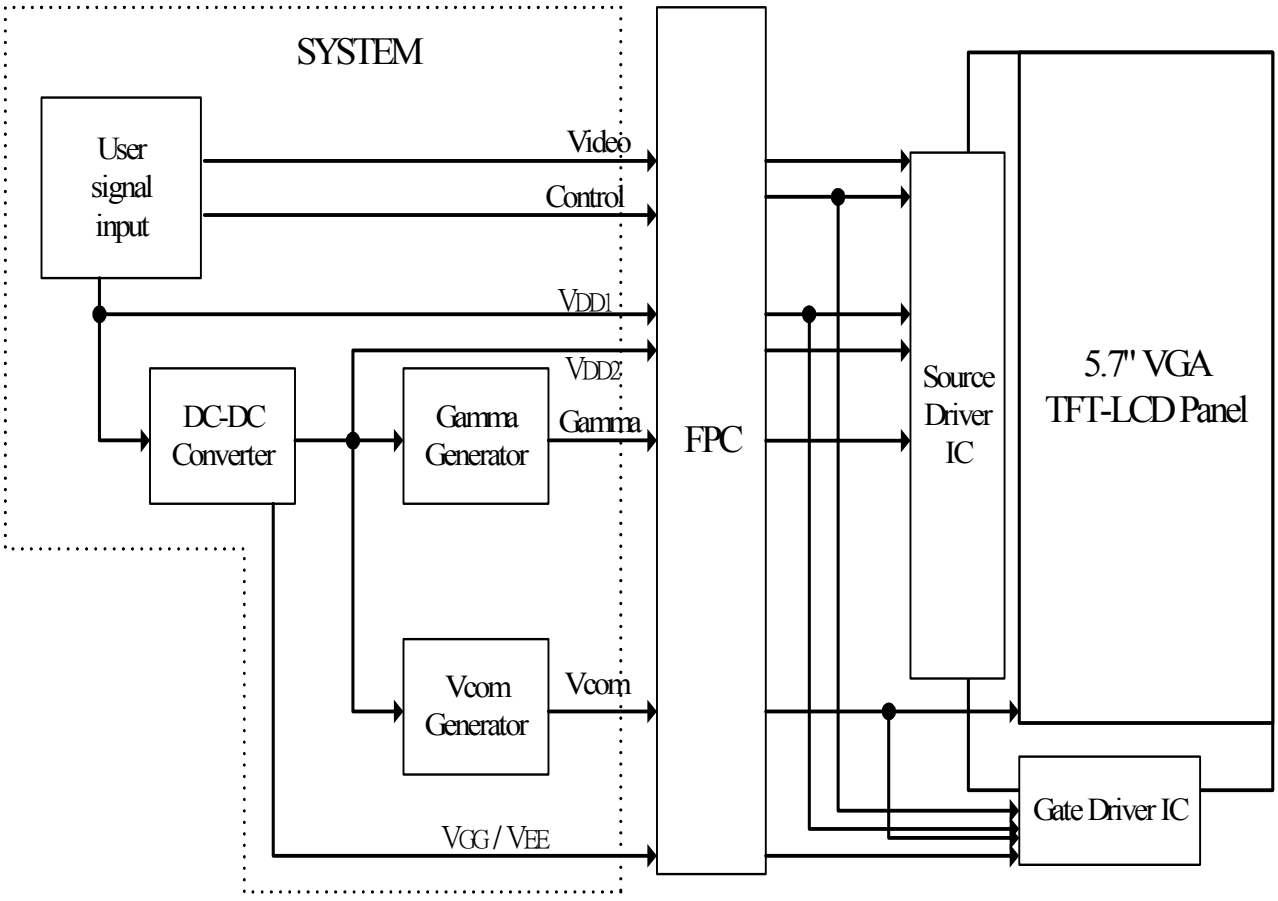


9. Display Color and Gray Scale Reference：

Color		Input Color Data																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magent	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighte																								
	Red	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighte																								
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighte																								
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

10. Block Diagram :

TFT-module Block Diagram :



11. Operation description :

11-1) SPI Register Description :

Register Name	Test RW	Address A3	A2	A1	A0	Data D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	▯	▯	▯	▯	▯	PSC	STB	RESETB
						▯	▯	▯	▯	▯	0	0	1
R1	0	0	0	0	1	▯	▯	▯	RESL1	RESL0	IF2	IF1	IF0
						▯	▯	▯	1	0	0	0	1
R2	0	0	0	1	0	▯	▯	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
						▯	▯	0	0	0	0	0	0
R3	0	0	0	1	1	▯	▯	STVP3	STVP2	STVP1	STVP0	FRAD1	FRAD0
						▯	▯	0	0	0	0	0	0
R4	0	0	1	0	0	CS	FRP	FRC	LPF	VS_POL	HS_POL	NPC_SET	NPC_IN
						1	0	1	1	0	0	0	1
R5	0	0	1	0	1	AUTO_DP	DISP_ON	A_TIME1	A_TIME0	B_TIME2	B_TIME1	B_TIME0	▯
						1	0	0	1	0	1	0	▯

▯ RW must always keep low.

- **Register R0**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	reserved	PSC	STB	RESETB
Default	-	-	-	-	-	0	0	1

Table 11.1 Register R0 setting

PSC: Operating mode setting by input pin or SPI register.
PSC="H", set STB, FRP, CS, IF[2:0],RESL[1:0] by SPI register.
PSC="L", set STB, FRP, CS, IF[2:0], RESL[1:0] by input pin.

STB: Standby mode setting.
STB="L", TCON and source driver are off
STB="H", all the functions are on.

RESETB: Global reset.
RESETB="L", global reset the whole chip.
RESETB="H", Normal operation.

- **Register R1**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	RESL1	RESL0	IF2	IF1	IF0
Default	–	–	–	1	0	0	0	1

Table 11.2 Register R1 setting

RESL [1:0]: Display resolution selection.

RESL1	RESL0	Resolution
0	0	**reserved**
0	1	reserved
1	0	**1920 x RGB x 480**
1	1	reserved

Table 11.3 Display resolution selection

IF [2:0]: Data input mode selection.

IF2	IF1	IF0	Data input format	Operating freq
0	0	0	**reserved**	**reserved**
0	0	1	24-bit parallel RGB	25.175MHz (Max)
0	1	0	**reserved**	**reserved**
0	1	1	**reserved**	**reserved**
1	0	0	**reserved**	**reserved**
1	0	1	**reserved**	**reserved**
1	1	0	**reserved**	**reserved**
1	1	1	**reserved**	**reserved**

Table 11.4 Data input mode selection

- **Register R2**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
Default	—	—	0	0	0	0	0	0

Table 11.5 Register R2 setting

STHD [5:0]: adjust start pulse position by dot

STHD5	STHD4	STHD3	STHD2	STHD1	STHD0	STH position adjust	Unit
0	0	0	0	0	0	0	T_{CPH}
0	0	0	0	0	1	+1	T_{CPH}
0	0	0	0	1	0	+2	T_{CPH}
0	0	0	0	1	1	+3	T_{CPH}
0	0	0	1	0	0	+4	T_{CPH}
0	0	0	1	0	1	+5	T_{CPH}
0	0	0	1	1	0	+6	T_{CPH}
0	0	0	1	1	1	+7	T_{CPH}
				⋮			
0	1	1	0	0	0	+24	T_{CPH}
0	1	1	0	0	1	+25	T_{CPH}
0	1	1	0	1	0	+26	T_{CPH}
0	1	1	0	1	1	+27	T_{CPH}
0	1	1	1	0	0	+28	T_{CPH}
0	1	1	1	0	1	+29	T_{CPH}
0	1	1	1	1	0	+30	T_{CPH}
0	1	1	1	1	1	+31	T_{CPH}
1	0	0	0	0	0	-1	T_{CPH}
1	0	0	0	0	1	-2	T_{CPH}
1	0	0	0	1	0	-3	T_{CPH}
1	0	0	0	1	1	-4	T_{CPH}
1	0	0	1	0	0	-5	T_{CPH}
1	0	0	1	0	1	-6	T_{CPH}
1	0	0	1	1	0	-7	T_{CPH}
1	0	0	1	1	1	-8	T_{CPH}
				⋮			
1	1	1	0	0	0	-25	T_{CPH}
1	1	1	0	0	1	-26	T_{CPH}
1	1	1	0	1	0	-27	T_{CPH}
1	1	1	0	1	1	-28	T_{CPH}
1	1	1	1	0	0	-29	T_{CPH}
1	1	1	1	0	1	-30	T_{CPH}
1	1	1	1	1	0	-31	T_{CPH}
1	1	1	1	1	1	-32	T_{CPH}

Table 11.6 Adjust start pulse position by dot

- **Register R3**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	STVP3	STVP2	STVP1	STVP0	FRAD1	FRAD0
Default	–	–	0	0	0	0	0	0

Table 11.7 Register R3 setting

STVP [3:0]: adjust first line position by line

STVP3	STVP2	STVP1	STVP0	STV position adjust	Unit
0	0	0	0	0	T_H
0	0	0	1	+1	T_H
0	0	1	0	+2	T_H
0	0	1	1	+3	T_H
0	1	0	0	+4	T_H
0	1	0	1	+5	T_H
0	1	1	0	+6	T_H
0	1	1	1	+7	T_H
1	0	0	0	-1	T_H
1	0	0	1	-2	T_H
1	0	1	0	-3	T_H
1	0	1	1	-4	T_H
1	1	0	0	-5	T_H
1	1	0	1	-6	T_H
1	1	1	0	-7	T_H
1	1	1	1	-8	T_H

Table 11.8 Adiust first line position by line

FRAD [1:0]: Odd frame or Even frame advance control

FRAD1	FRAD0	Advance Frame	Notes
0	0	**reserved**	
0	1	**reserved**	
1	0	Even frame	Odd frame Tstv = STVP setting + 1H
1	1	Reserve	Reserve

Table 11.9 Odd frame or Even frame advance control

- **Register R4**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CS	FRP	FRC	LPF	VS_POL	HS_POL	NPC_SET	NPC_IN
Default	1	0	1	1	0	0	0	1

Table 11.10 Register R4 setting

CS: Charge share function control.
CS=L, disable charge share function.
CS=H, enable charge share function.

FRP: Select normally white or normally black panel.
FRP=L, pass the input data for normally white panel.
FRP=H, inverse the input data for normally black panel.

FRC: Dithering ON/OFF control.
FRC=L, Dithering function disable.
FRC=H, Dithering function enable

LPF: **Reserved**

VS_POL: VS polarity setting.
VS_POL=L, negative polarity.
VS_POL=H, positive polarity.

HS_POL: HS polarity setting.
HS_POL=L, negative polarity.
HS_POL=H, positive polarity.

NPC_SET: Set the NTSC/PAL auto detection or define by NPC_IN.
NPC_SET=L, auto detection.
NPC_SET=H, define by NPC_IN.

NPC_IN: Define the NTSC/PAL mode by SPI.
NPC_IN=L, PAL.
NPC_IN=H, NTSC.

- **Register R5**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	AUTO_DP	DISP_ON	A_TIME1	A_TIME0	B_TIME2	B_TIME1	B_TIME0	reserved
Default	1	0	0	1	0	1	0	—

Table 11.11 Register R5 setting

AUTO_DP: When power on, select blank image display time decided by A_TIME (bit 5, 4) or DISP_ON (bit 6).
AUTO_DP ="L", Blank image display time decided by DISP ON (bit 6).
AUTO_DP ="H", Blank image display time decided by A TIME (bit 5, 4).

DISP_ON: When AUTO_DP (bit 7) = "L", and DISP_ON = "H", blank image display off, then display normal image.

A_TIME [1:0]: When AUTO_DP(bit 7) = "H". the blank image display time is decided by A_TIME
00: blank image display time is 8 VS time
01: blank image display time is 16 VS time
10: blank image display time is 32 VS time
11: blank image display time is 64 VS time

B_TIME [2:0]: When into STB mode. the blank image display time is decided by B_TIME.
000: blank image display time is 3 VS time.
001: blank image display time is 4 VS time.
010: blank image display time is 5 VS time.
011: blank image display time is 6 VS time.
100: blank image display time is 7 VS time.
101: blank image display time is 8 VS time.
110: blank image display time is 9 VS time.
111: blank image display time is 10 VS time.

11-2) Power ON Control :

To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: VCC1, GND → VDDA, VSSA → V1 to V10
Power OFF: V1 to V10 → VDDA, VSSA → VCC1, GND

Source drive has a power ON sequence control function. There are two kinds of the mode. One is auto mode, and another is manual mode.

Auto Mode: When power is ON, blank data is outputted for 16-frames (default value) first, from the falling edge of the following VS signal. The blank data would be gray level 255 for normally white panel.
It can be defined in register R5 A_TIME1(bit 5) and A TIME0 (bit 4) when AUTO_DP(bit 7) = "H"

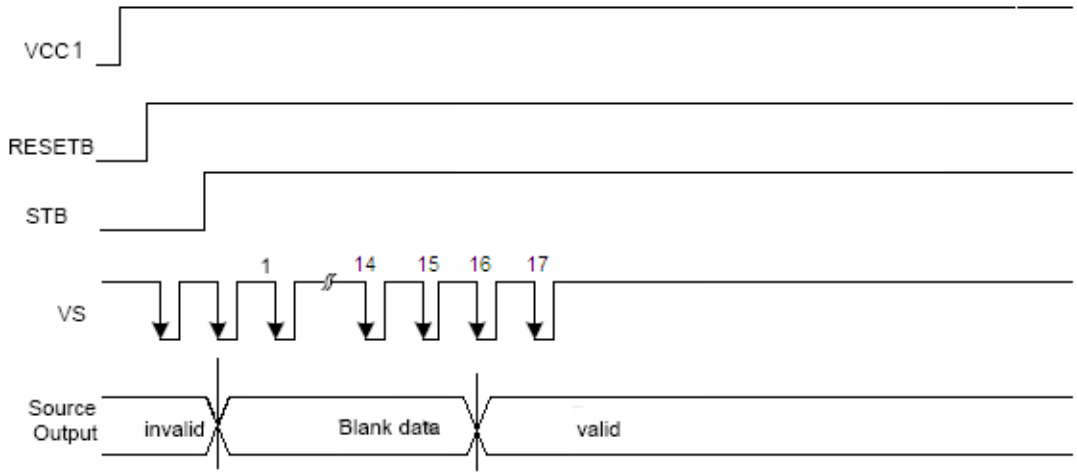


Figure 11-1 Power on control for Auto Mode

Manual Mode: When power is ON , you should set the register R5 AUTO_DP(bit 7) = "L" to stay at the manual mode. Blank data is outputted until the DISP_ON(bit 6) = H then display the normal image.

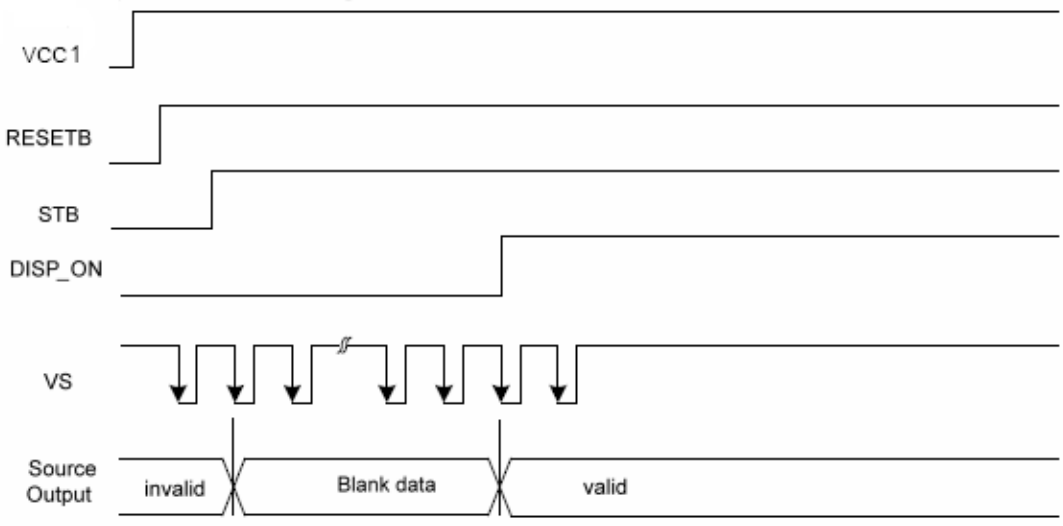


Figure 11-2 Power on control for Manual Mode

11-3) Standbys ON/OFF Control :

Source drive has a standby ON/OFF sequence control function. When STB pin is "L", blank data is outputted for 5-frames (default value) first, from the falling edge of the following VSYNC signal. The blank data would be gray level 255 for normally white panel. It can be defined in register R5 B_TIME[2:0] to adjust the frame number of the blank data.

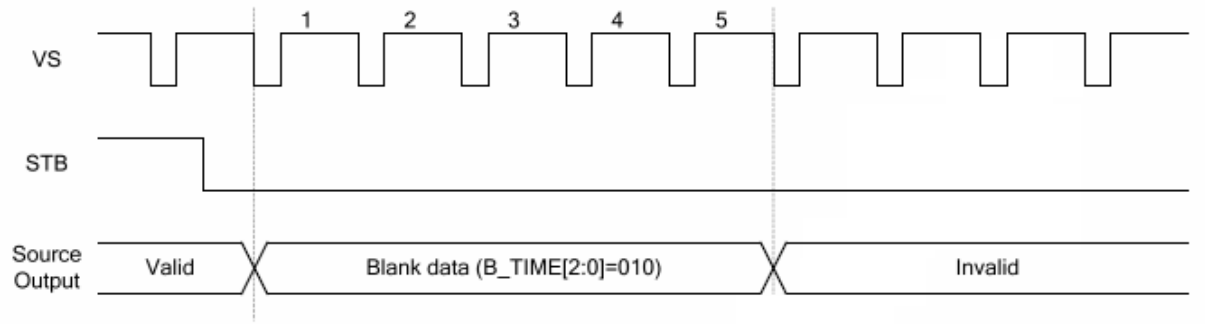


Figure 11-3 Standby ON/OFF Control

11-4) Reset when power on :

Source drive is internally initialized by the global reset signal. RESETB. The reset input must be held for at least 1ms after power is stable.

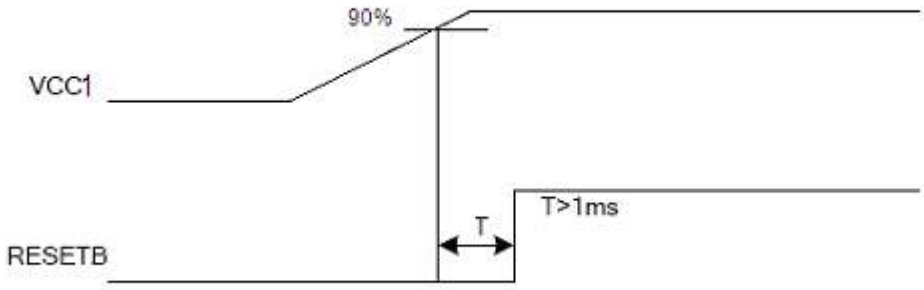


Figure 11-4 RESETB control after power stable

12. AC Characteristics :

12-1) SPI timing characteristics :

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPCK period	T_{CK}	60	-	-	ns
SPCK high width	T_{CKH}	30	-	-	ns
SPCK low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CE}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns

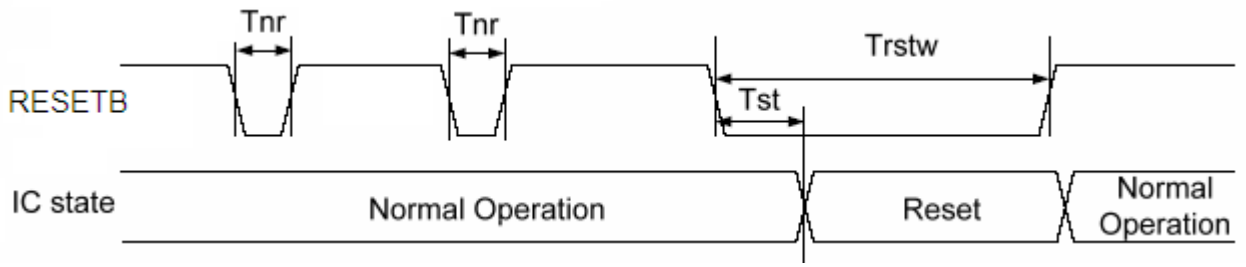
12-2) Digital Parallel RGB interface :

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK Frequency	F_{CPH}	-	25.175	-	MHz
CLK period	T_{CPH}	-	39.7	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	800	-	T_{CPH}
HS pulse width	T_{WH}	5	30	-	T_{CPH}
HS-first horizontal data line	T_{HS}	112	144	175	T_{CPH}
DEN pulse width	T_{EP}	-	640	-	T_{CPH}
VS pulse width	T_{WV}	1	3	5	T_H
VS-DEN time	T_{STV}	-	35	-	T_H
VS period	T_V	-	525	-	T_H

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	100	-	T_{CPH}
CKV pulse width	T_{CKV}	-	96	-	T_{CPH}
HS-CKV time	T_1	-	52	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HA-POL time	T_3	-	72	-	T_{CPH}
STV setup time	T_{SUV}	-	46	-	T_{CPH}
STV pulse time	T_{WSTV}	-	1	-	T_H

12-3) Hardware reset timing :

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
RESETB low pulse width		10	-	-	μs
Negative noise pulse width	T_{nr}	-	-	2	μs
Reset start time	T_{st}	2	-	-	μs



13. Waveform :

Timing Controller Timing Chart :

13-1) SPI timing :

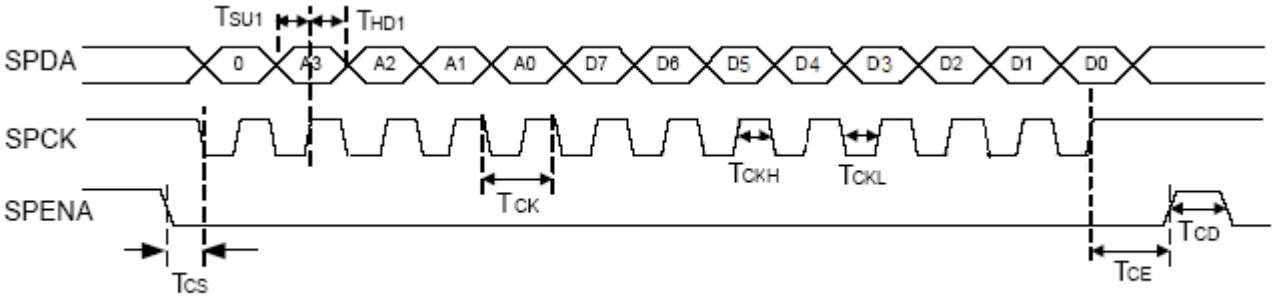


Figure 13-1 SPI timing

13-2) Clock and Data input waveforms :

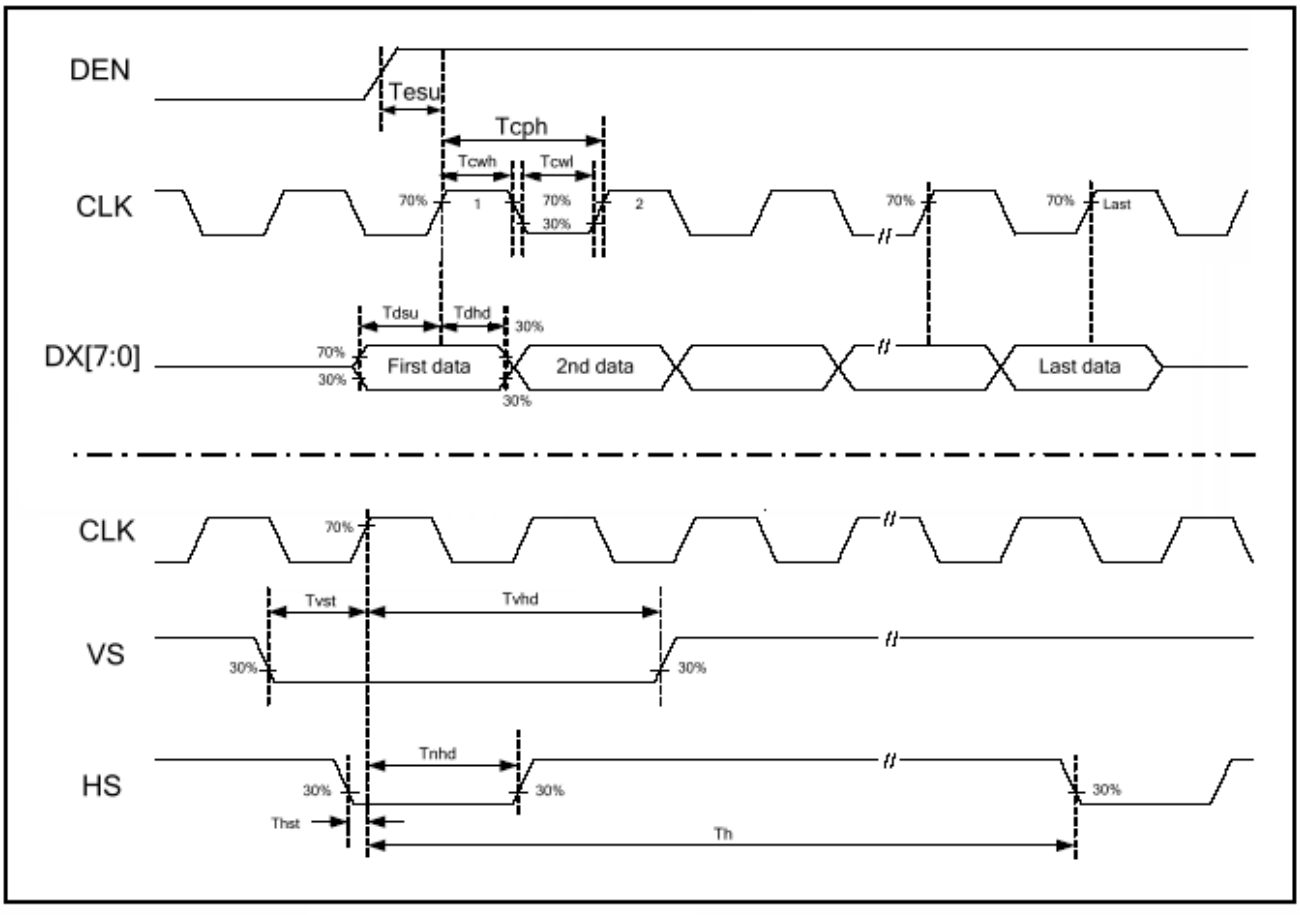


Figure 13-2 Clock and Data input waveforms.

13-3) Data input format for RGB Mode :

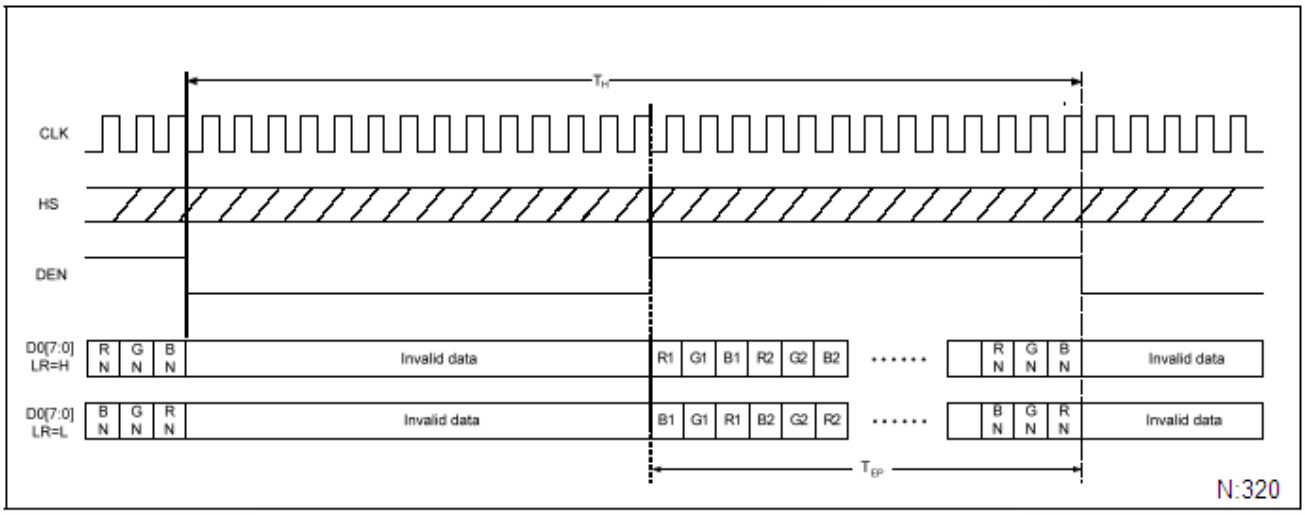


Figure 13-3 Parallel RGB Horizontal Data Format

13-6) The HS & VS timing of the ODD/EVEN field :

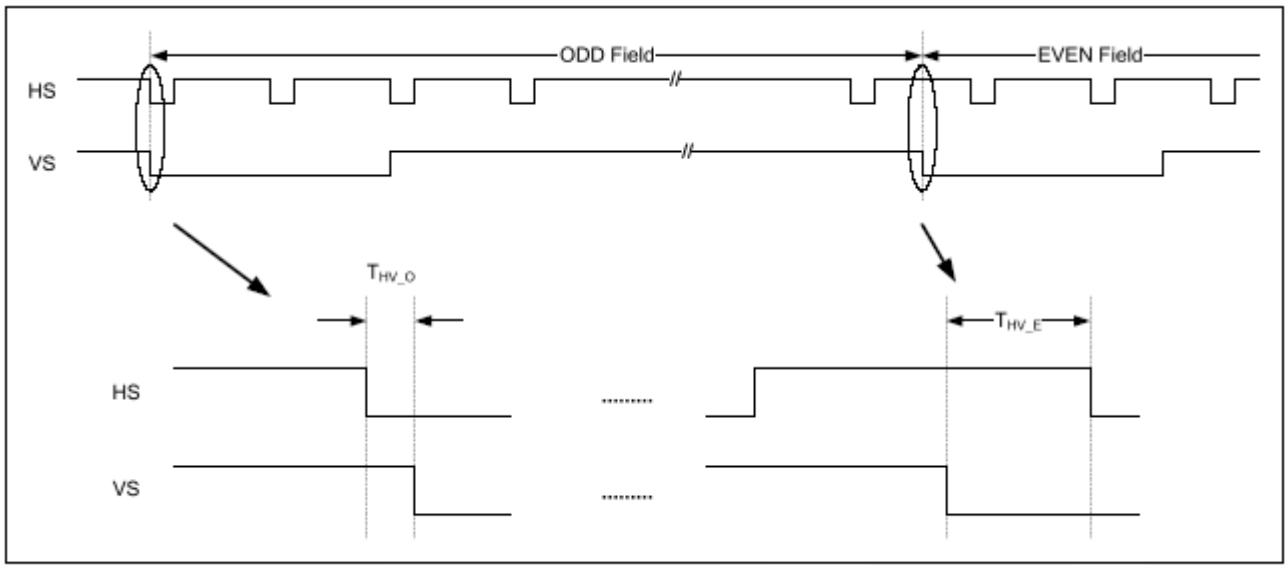
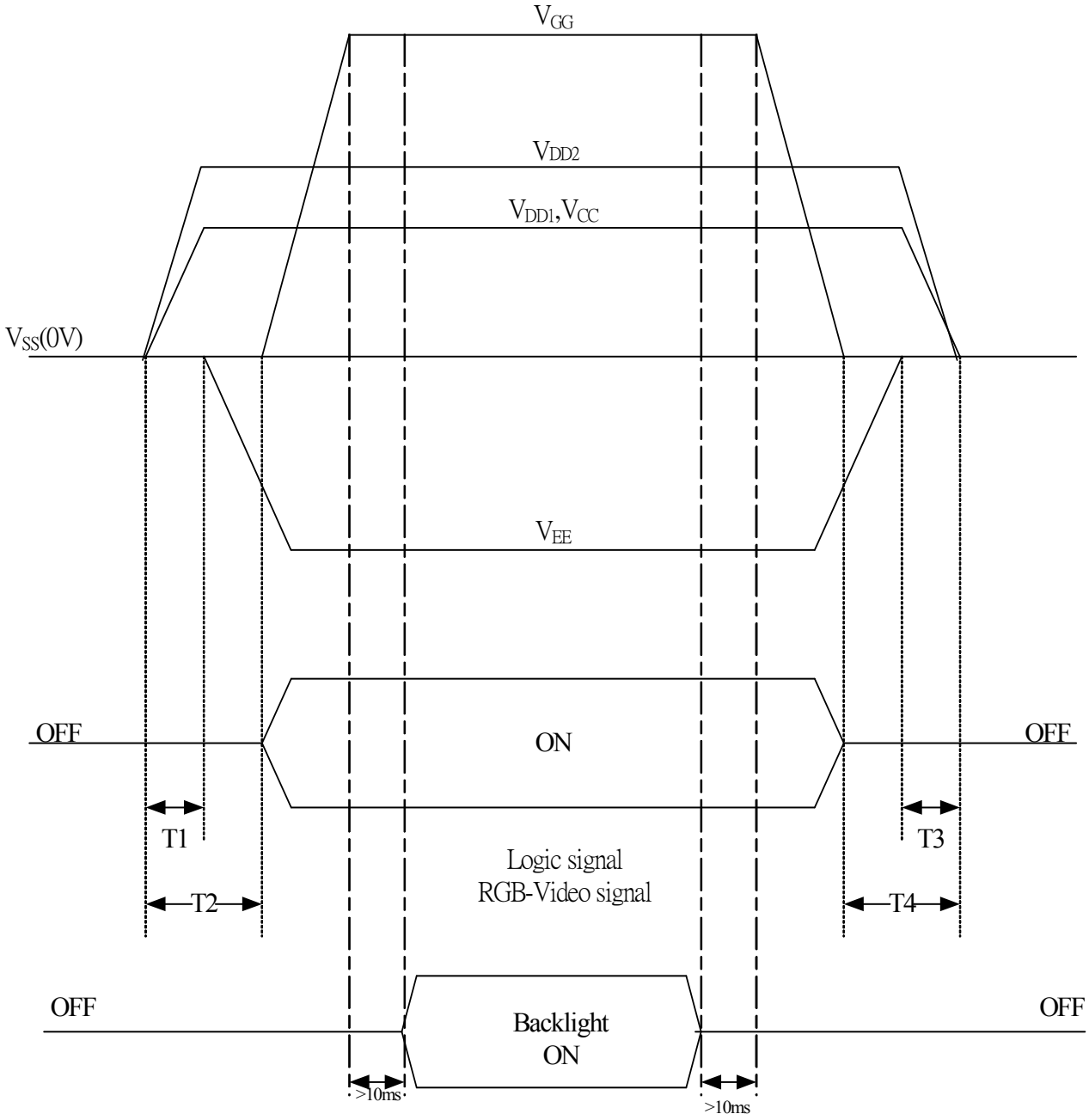


Figure 13-15 Define the HSYNC to VSYNC timing for RGB mode

14. Power On Sequence：

The Power on Sequence only effect by VCC1, VGG, VCC2, VSSA and VEE, the others do not care.



1) 10ms≦T1<T2

2) 0ms<T3≦T4≦10ms

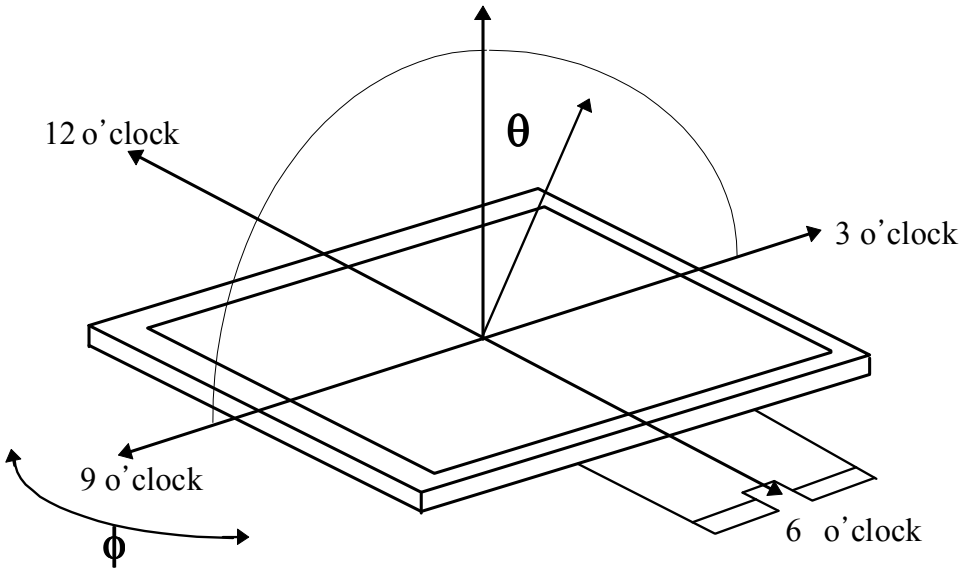
15. Optical Characteristics :

15-1) Specification: :

Ta=25℃

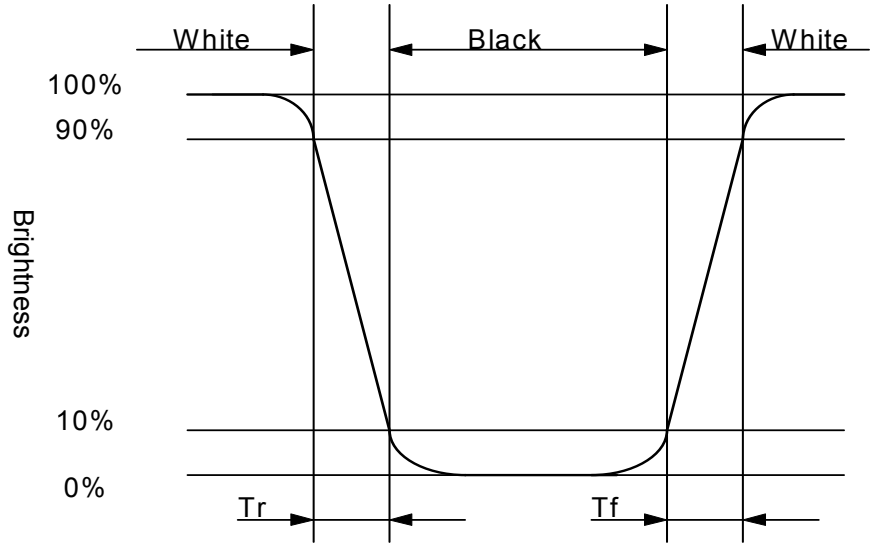
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	Θ	CR≧10	75	80	-	deg	Note 15-1
	Vertical	Θ (to 6 o' clock)		65	70	-	deg	
		Θ (to 12 o' clock)		45	50	-	deg	
Contrast Ratio		CR	At optimized viewing angle	400	600	-	-	Note 15-2
Response time	Rise	Tr	Θ =0°	-	15	30	ms	Note 15-3
	Fall	Tf		-	25	50	ms	
Brightness		-	Θ =0°/ϕ =0	450	500	-	cd/m²	
Luminance Uniformity		U%		80	85	-	%	
White Chromaticity		x		0.26	0.30	0.34	-	
		y		0.29	0.33	0.37	-	
Cross Talk		-	Θ =0°	-	-	3.5	%	Note 15-4
LED Life Time		-		20000	-	-	hr	Note 15-5

Note 15-1: The definitions of viewing angles are as follow :



Note 15-2: The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 15-3: Definition of Response Time Tr and Tf :



Note 15-4 : Cross Talk (CTK) $= \frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A

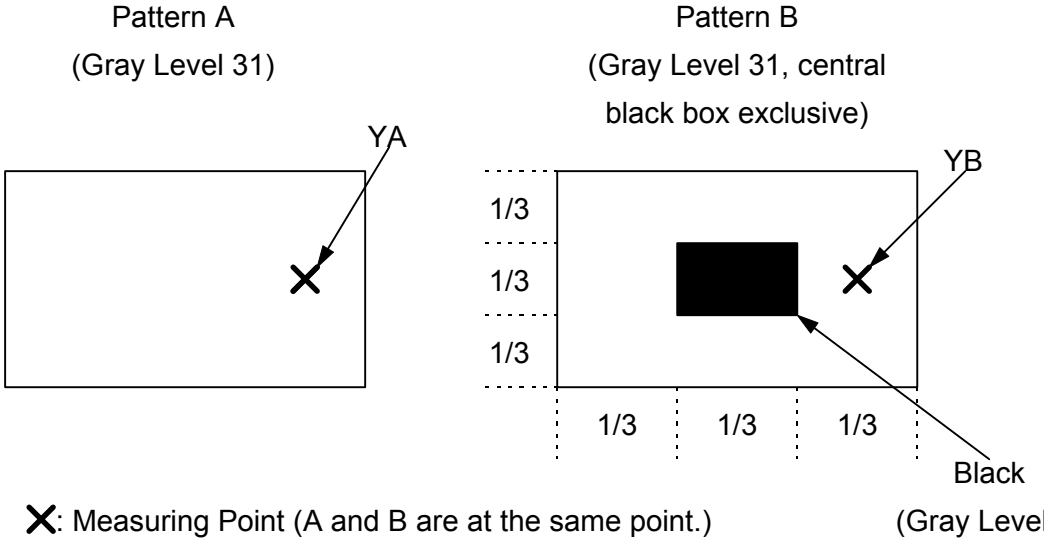
YB: Brightness of Pattern B

Luminance meter : BM 5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module



Note 15-5 : The " LED Life time " is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25℃ and I_{LED} =20mA

16. Handling Cautions :

16-1) Mounting of module :

a) Please power off the module when you connect the input/output connector.

b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

c) Protective film (Laminator) is applied on surface to protect it against scratches and dirt.

d) Please following the tear off direction as figure 16-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

16-2) Precautions in mounting :

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

16-3) Adjusting module :

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

16-4) Others :

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal is stuck on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

f) Please adjust the voltage of common electrode as material of attachment by 1 module.

16-5) Polarizer mark :

The polarizer mark is to describe the direction of wide view angle film how to match up with the rubbing direction.

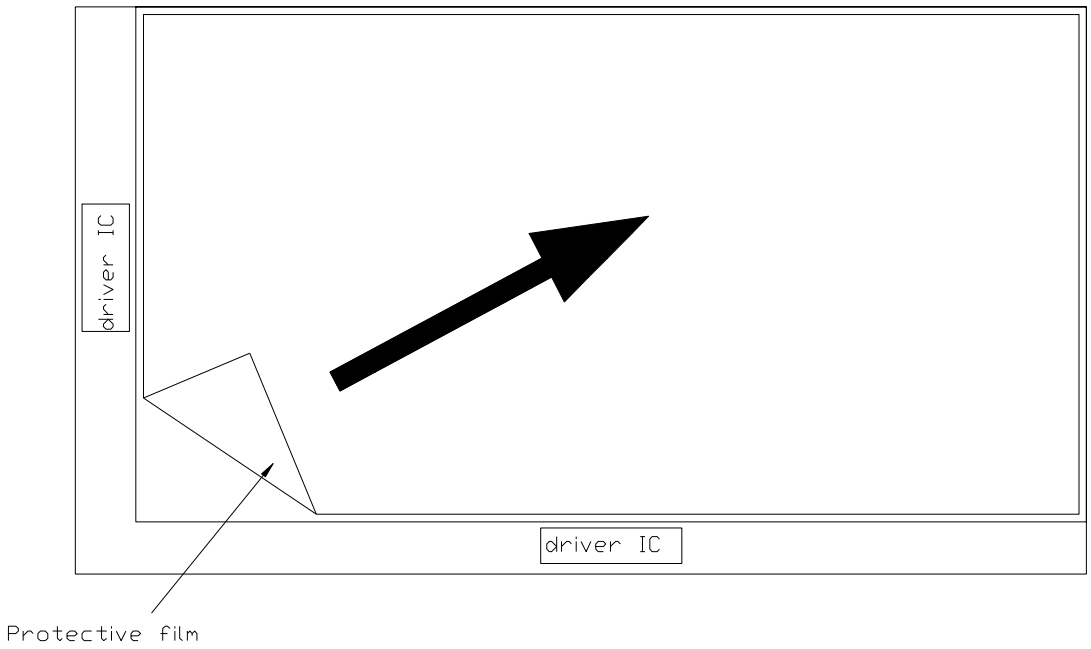


Figure 16-1 the way to peel off protective film

17. Reliability Test :

No	Test Item	Test Condition	Remark
1	High Temperature Storage Test	Ta = +80℃, 240 hrs	
2	Low Temperature Storage Test	Ta = -40℃, 240 hrs	
3	High Temperature Operation Test	Ta = +70℃, 240 hrs	
4	Low Temperature Operation Test	Ta = -30℃, 240 hrs	
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs (No Condensation)	
6	Thermal Cycling Test (non-operating)	-20℃(+70℃, 200 Cycles 30 min 30 min	
7	Vibration Test (non-operating)	Frequency: 10 ~ 57 HZ /Vibration Width:0.075mm 58-500 Hz / Gravity: 9.8m/s2 Sweep time: 11 minutes Test period: 3 hrs for each direction of X, Y, Z	
8	Shock Test (non-operating)	Gravity: 490m/s2 * 6ms Direction: ±X, ±Y, ±Z 3 times for each direction	
9	Electrostatic Discharge Test (non-operating)	150pF, 330Ω Air : ±15KV ; Contact : ±8KV 10 times/point, 9 points/panel face	

Ta: ambient temperature

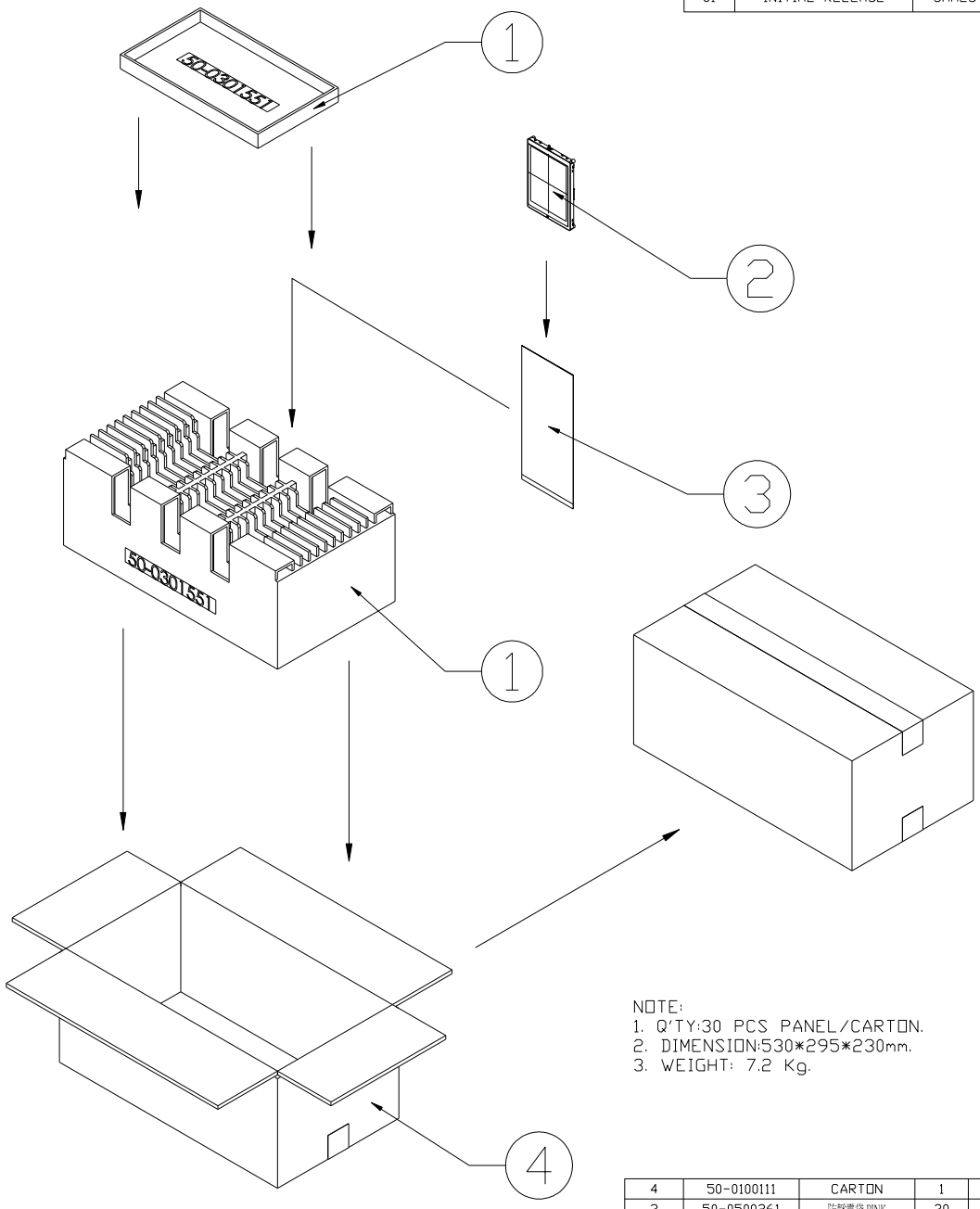
Note: The protective film must be removed before temperature test

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (Including : line defect, no image) All the cosmetic specification is judged before the reliability stress.

18. Packing Diagram：

REV.	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	JAMES	2007/09/07



NOTE:
1. Q'TY:30 PCS PANEL/CARTON.
2. DIMENSION:530*295*230mm.
3. WEIGHT: 7.2 Kg.

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
4	50-0100111	CARTON	1	
3	50-0500261	防靜電袋 PINK	30	抗靜電
2		5.7" Module	30	
1	50-0301551	瓦楞隔板緩衝材	1	上蓋+底座

MTL.SPEC.	UNSPECIFIED TOL. ANGLE ROUGHNESS	REMARK	元太科技股份有限公司 Prime View Internation Co.,ltd.		
APPROVE	FRANK SHIN	SCALE	UNIT	SHEET 1 OF 1	DWG.TITLE 5.7" Module Packing Draw
CHECK	FRANK SHIN	MTL.NO. PD057VX3		DWG.NO.	REV. 01 / A4 SIZE
DESIGN	JAMES				