



<p>TECHNICAL SPECIFICATION</p> <p>MODEL NO. : PD050VXB</p>
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The content of this information is subject to be changed without notice.

Please contact EIH or its agent for further information.

Customer's Confirmation

Customer _____

Date _____

By _____

EIH's Confirmation

Dep	FAE	Panel Design	Electronic Design	Mechanical Design	Product Verification	Prepared by
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Revision History

Rev.	Issued Date	Revised Contents
0.1	March 16,2011	New



TECHNICAL SPECIFICATION

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1.Application

This data sheet applies to a color TFT LCD module, PD050VXB.

This module applies to OA product, computer peripheral, industrial meter, image communication and multi-media. If you must use in severe reliability environment, please don't extend over EIH's reliability test conditions.

If you use PD050VXB, Elnk Holding Inc advises your systems use EIH's timing controller IC (PVI-2003A) which will generate proper timing signals to control it.

2. Features

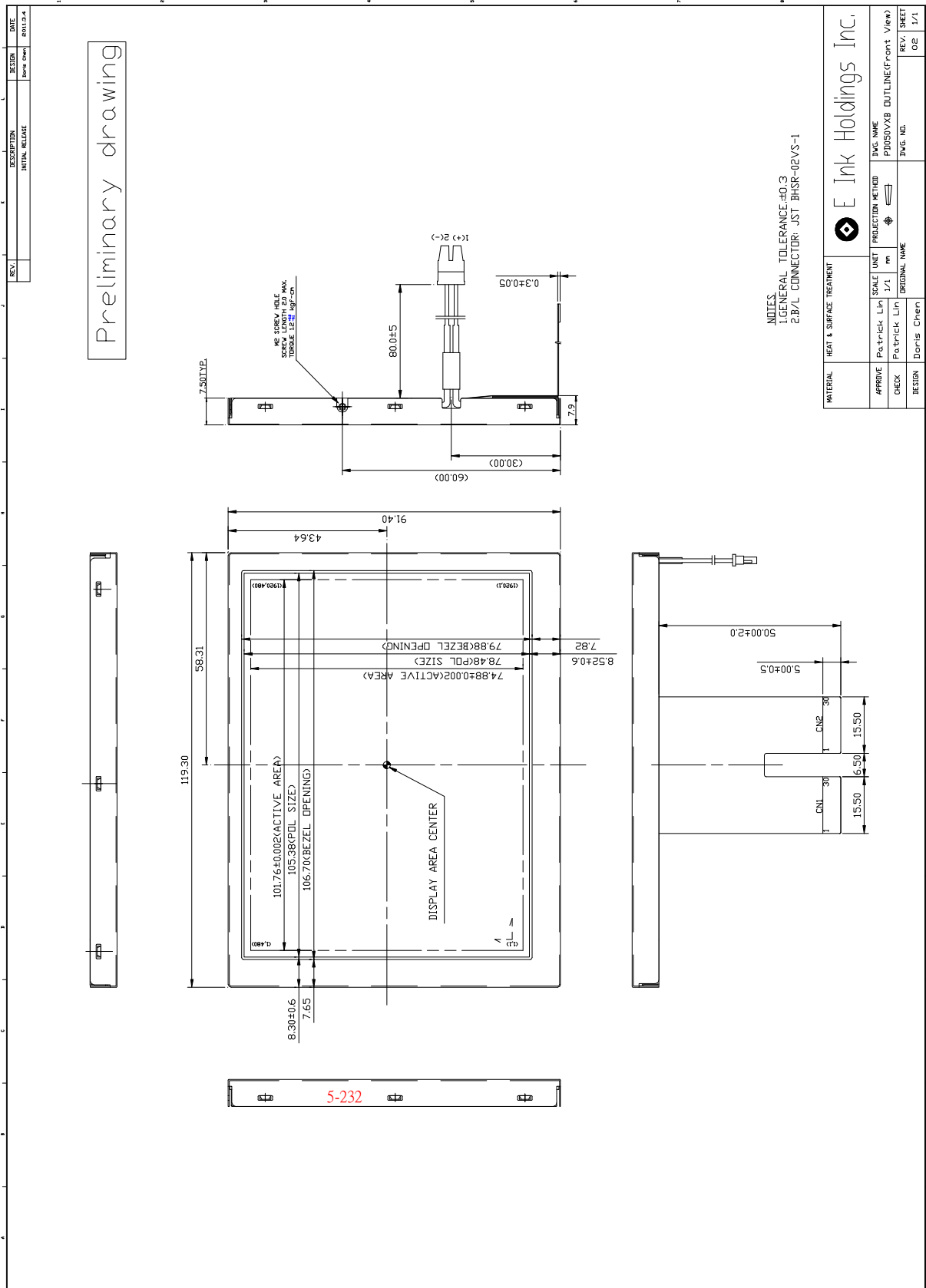
- . VGA (640*480 pixels) resolution
- . Amorphous silicon TFT LCD panel with back-light unit
- . Pixel in stripe configuration
- . Thin and light weight
- . Display Colors : 262,144 colors
- . Portrait mode
- . TTL transmission interface

3.Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	5.0(diagonal)	inch
Display Format	640(H)×(R, G, B)×480(V)	dot
Display Colors	262,144	
Active Area	74.88 (H)×101.76(V)	mm
Pixel Pitch	0.156(H)×0.159(V)	mm
Pixel Configuration	Stripe	
Surface Treatment	AG+EWV	
Outline Dimension	91.4(H)×119.3 (V)×7.9(D)	mm
Weight	TBD	g
Back-light	LED	
Display mode	Normally white	
Gray scale inversion direction	3 o'clock [ref. to Note 13-1]	



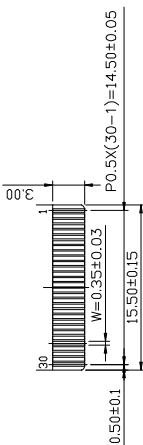
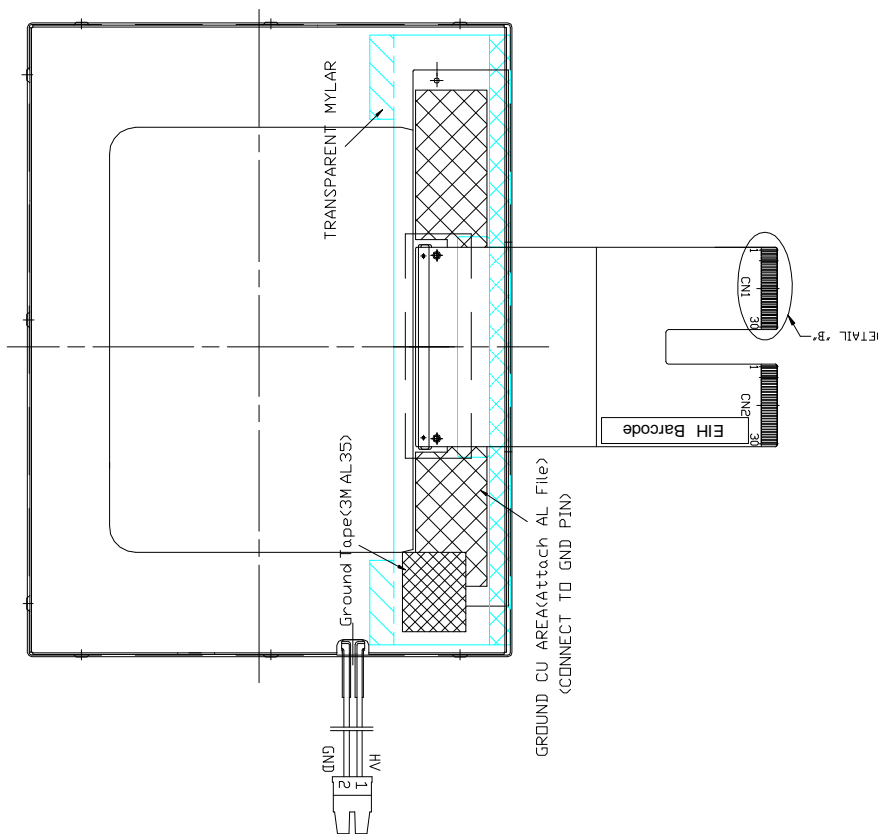
4.Mechanical Drawing of TFT-LCD Module





REV.	DESCRIPTION	DESIGN	DATE
	INITIAL RELEASE	Spoke Chen	2011.9.4

Preliminary drawing



DETAIL 'B'
(S: 2/1,2PLS)

NOTES:
1. GENERAL TOLERANCE: ±0.3
2. B/L CONNECTOR: JST BHSR-02VS-1

MATERIAL		HEAT & SURFACE TREATMENT		E Ink Holdings Inc.	
APPROVE	Patrick Lin	SCALE UNIT	1/1	PROJECTION METHOD	PD050VXB OUTLINE (Back View)
CHECK	Patrick Lin	INCH	mm	DESIGN	Doris Chen
DESIGN	Doris Chen	ORIGINAL NAME		DESIGN NO.	
				REV. SHEET	02 1/1

**5. Input / Output Terminals****5-1) TFT-LCD Panel Driving****CN 1**

LCD Module Connector

30 Pins , Pitch : 0.5 mm

Pin No.	Symbol	I/O	Function	Remark
1	DIO1	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-6
2	VSS1	I	Ground	
3	VDD1	I	Power Supply for Source	
4	CLK	I	Horizontal Shift Clock	
5	VSS1	I	Ground	
6	R/L	I	Right/Left selection	Note 5-6
7	R0	I	Red Data (LSB)	
8	R1	I	Red Data	
9	R2	I	Red Data	
10	R3	I	Red Data	
11	R4	I	Red Data	
12	R5	I	Red Data (MSB)	
13	VSS1	I	Ground	
14	G0	I	Green Data (LSB)	
15	G1	I	Green Data	
16	G2	I	Green Data	
17	G3	I	Green Data	
18	G4	I	Green Data	
19	G5	I	Green Data (MSB)	
20	VSS1	I	Ground	
21	B0	I	Blue Data (LSB)	
22	B1	I	Blue Data	
23	B2	I	Blue Data	
24	B3	I	Blue Data	
25	B4	I	Blue Data	
26	B5	I	Blue Data (MSB)	
27	LD	I	Load output signal	Note 5-7
28	REV	I	Data invert control	Note 5-8
29	POL	I	Polarity selection	Note 5-9
30	DIO2	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-6



CN 2

Pin No.	Symbol	I/O	Function	Remark
1	VSS2	I	Ground	
2	V1	I	Gamma Voltage 1	Note 5-10
3	V2	I	Gamma Voltage 2	Note 5-10
4	V3	I	Gamma Voltage 3	Note 5-10
5	V4	I	Gamma Voltage 4	Note 5-10
6	V5	I	Gamma Voltage 5	Note 5-10
7	V6	I	Gamma Voltage 6	Note 5-10
8	V7	I	Gamma Voltage 7	Note 5-10
9	VSS2	I	Ground	
10	V8	I	Gamma Voltage 8	Note 5-10
11	V9	I	Gamma Voltage 9	Note 5-10
12	V10	I	Gamma Voltage 10	Note 5-10
13	V11	I	Gamma Voltage 11	Note 5-10
14	V12	I	Gamma Voltage 12	Note 5-10
15	V13	I	Gamma Voltage 13	Note 5-10
16	V14	I	Gamma Voltage 14	Note 5-10
17	VSS2	I	Ground	
18	VDD2	I	Voltage for analog circuit	Note 5-10
19	VCOM	I	Common Voltage	
20	XON	I	NC	
21	OE	I	Output Enable	Note 5-5
22	U/D	I	Up/Down selection	Note 5-3
23	CKV	I	Vertical Shift Clock	Note 5-4
24	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note 5-3
25	STVD	I/O	Vertical Shift Pulse Signal Input or Output	Note 5-3
26	VGG	I	Gate On Voltage	Note 5-2
27	GND	I	Ground	
28	VCC	I	Voltage for logic circuit	
29	GND	I	Ground	
30	VEE	I	Gate Off Voltage	Note 5-1



Note 5-1: Gate off voltage, $V_{EE}=-5.5V$

Note 5-2: Gate on voltage, $V_{GG}=+15.4V$

Note 5-3: Select up or down shift

U/D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down

Note 5-4: Gate driver shift clock

Note 5-5: When OE is connected to high “1”, the driver outputs are disabled (Gate output = V_{EE}). Under this condition, the operation of registers will not be affected.

Note 5-6: Select left or right shift

R/L	DIO1	DIO2	Shift
1	Input	Hi-Z	Left to right
0	Hi-Z	Input	Right to left

Note 5-7: Latch the polarity of outputs and switch the new data to outputs. At the rising edge (LD), latch the “POL” signal to control the polarity of the outputs.

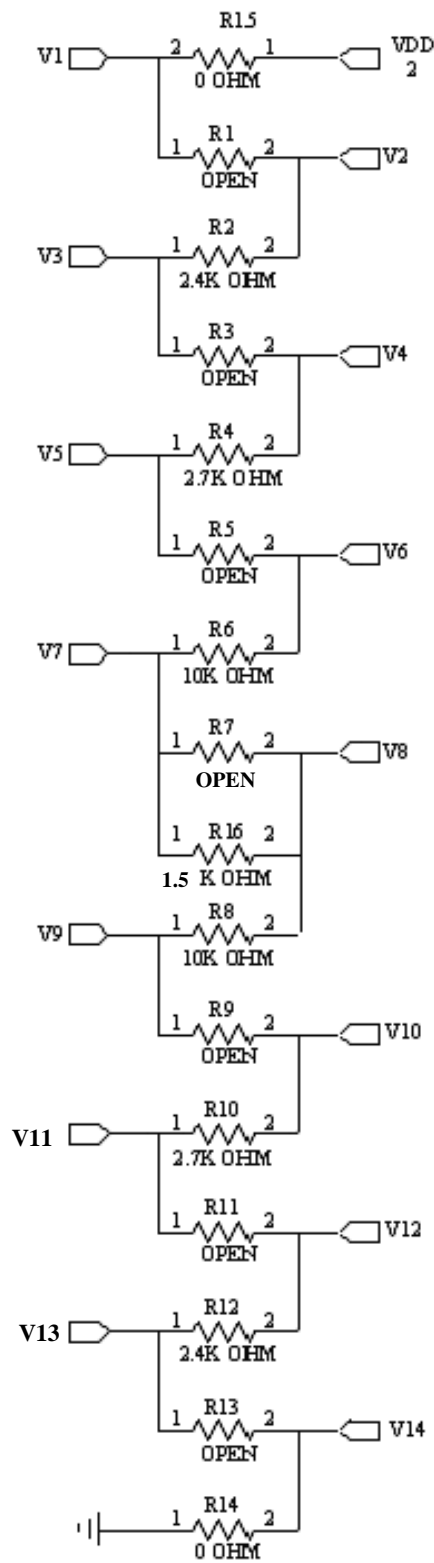
Note 5-8: Control whether the Data R0~G5 are inverted or not. (EIH suggests connecting to GND)
When “REV=1”, these data will be inverted.
EX: “00”→”3F”, “07”→”38”, “15”→”2A”

Note 5-9: Polarity selector for dot-inversion control. Available at the rising edge of LD.
When POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14;
When POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7.



Note 5-10: $V_{DD2} = +7.7V$

Typical Application Circuit (When $V_1 = +7.7V$)



**5-2) Backlight driving**

Pin No	Symbol	Description	Remark
1	+	Input terminal(Anode)	Red
2	NC	No connect	-
3	-	Input terminal(Cathode)	Black

6.Absolute Maximum Ratings:

$$V_{SS1}=V_{SS2}=GND=0V, T_a=25^{\circ}C$$

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	V_{DD1}	-0.5	5.0	V	
	V_{CC}	-0.3	6.0	V	
	V_{DD2}	-0.5	12.0	V	
	V_{GG}	-0.3	40.0	V	
	$V_{GG}-V_{EE}$	-0.3	40.0	V	
	V_{EE}	-20	0.3	V	
Storage Temperature	T_{st}	-30	80	$^{\circ}C$	
Operation Temperature	T_{op}	-20	70	$^{\circ}C$	

7.Electrical Characteristics**7-1) Recommended Operating Conditions:**

$$V_{SS1}=V_{SS2}=GND=0V, T_a=25^{\circ}C$$

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	V_{DD1}	2.3	3.3	3.6	V	
	V_{DD2}	6.5	7.7	13.5	V	
Supply Voltage for Gate Driver	V_{GG}	14.4	15.4	16.4	V	
	V_{EE}	-6.0	-5.5	-5.0	V	
	V_{CC}	2.3	3.3	5.5	V	
V_{com} Voltage	V_{com}	-	2.6	-	V	
Digital Input Voltage	V_{IH}	$0.7 V_{CC}$	-	V_{CC}	V	
	V_{IL}	0	-	$0.3 V_{CC}$	V	



7-2) Recommended Driving Condition for Back Light

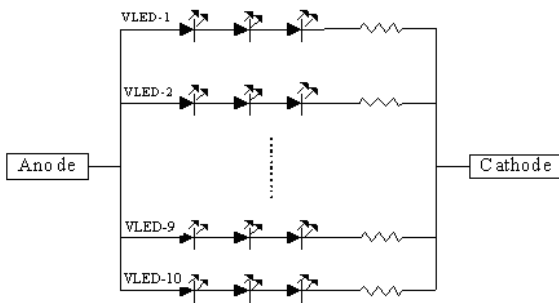
Ta = 25°C

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V _{LED}	-	-	11.5	V	Note 7-1
Supply current of LED backlight	I _{LED}	-	(20)	-	mA	Note 7-2
Backlight Power Consumption	P _{LED}	-	(2.2)	(2.3)	W	Note 7-1 /Note 7-3

Note 7-1 : I_{LED} = 20mA, Constant Current.

Note 7-2: The LED driving condition is defined for each LED module. (3 LED Serial)
Input current = 20 mA *10=200mA

Note 7-3: P_{LED} = (V_{LED} * I_{LED})



7-3) Power Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	I _{GG}	V _{GG} =+15.4V	(0.1)	(0.3)	mA	
Supply Current for Gate Driver (Low level)	I _{EE}	V _{EE} =-5.5V	(0.1)	(0.3)	mA	
Supply Current for Source Driver (Digital)	I _{DD1}	V _{DD1} =+3.3V	(4.7)	(9.4)	mA	
Supply Current for Source Driver (Analog)	I _{DD2}	V _{DD2} =+7.7V	(17.0)	(34.0)	mA	
Supply Current for Gate Driver (Digital)	I _{CC}	V _{CC} =+3.3V	(0.1)	(0.3)	mA	
LCD Panel Power Consumption		-	(148.8)	(300.0)	mW	Note 7-4
Back Light Lamp Power Consumption		-	(2.2)	(2.3)	W	Note 7-5

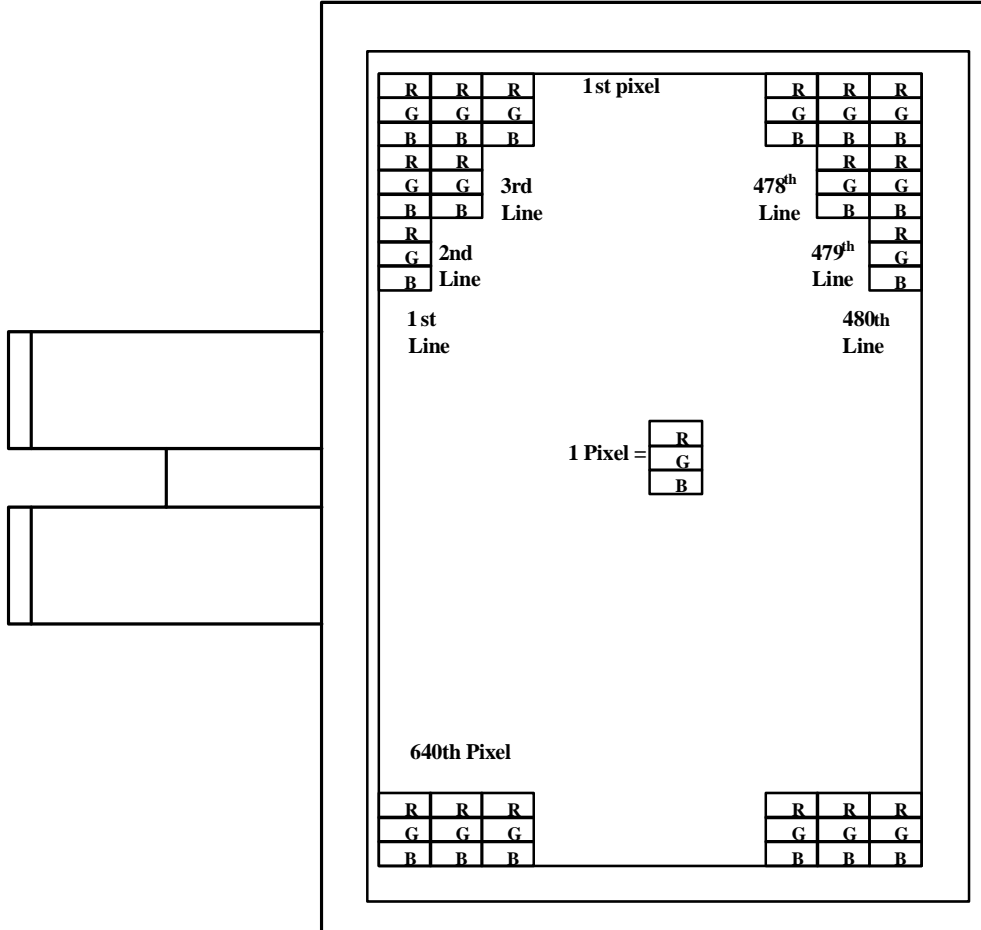
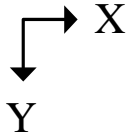
Note 7-4: The power consumption for back light is not included.

Note 7-5: Back light lamp power consumption is calculated by I_L×V_L.



8. Pixel Arrangement

The LCD module pixel arrangement is the stripe.





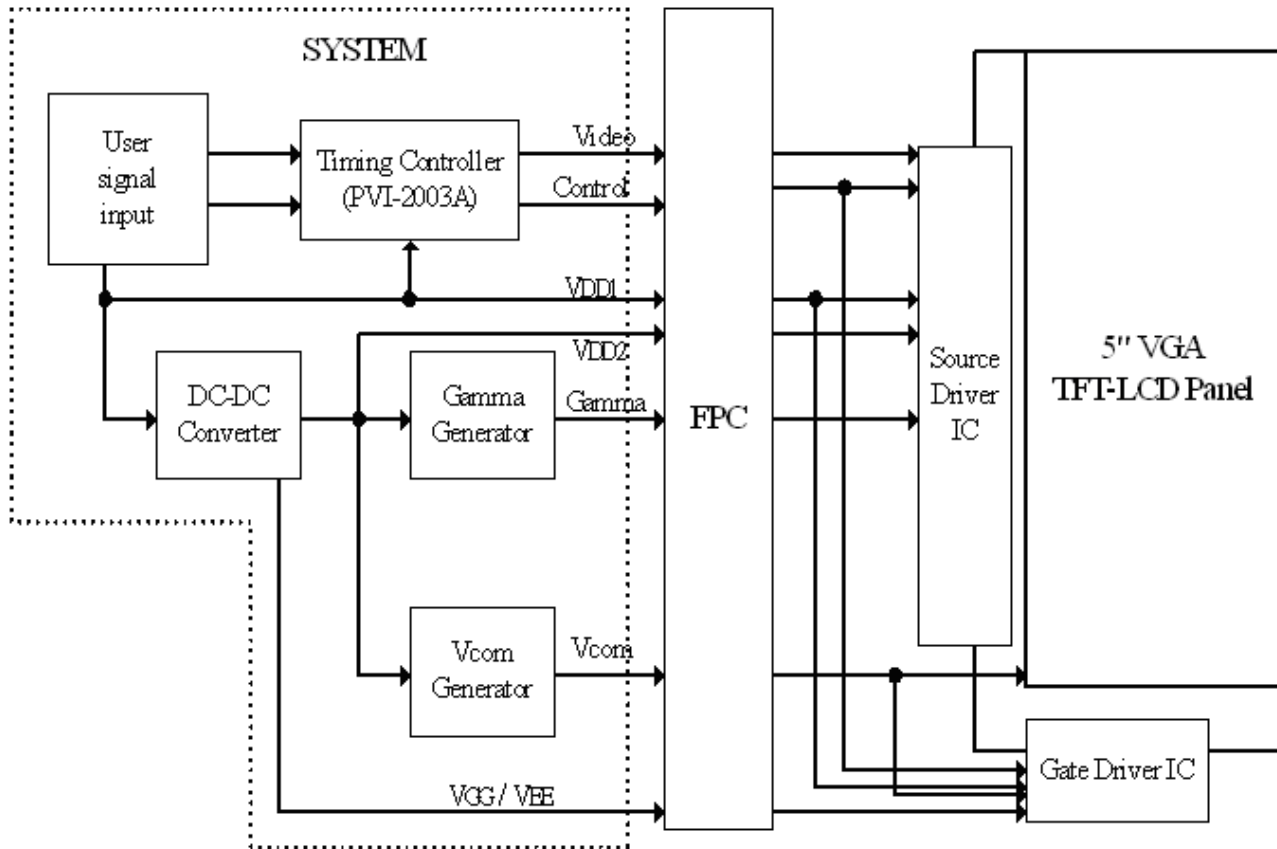
9.Display Color and Gray Scale Reference

Color		Input Color Data																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	



10. Block Diagram

10-1) TFT-module Block Diagram



If you use PD050VXB you can apply PVI-2003A(Timing controller) which will generate timing signals to support PD050VXB.

**11. Interface Timing****11.1) Timing Parameters**AC Electrical Characteristics ($V_{CC}=V_{DD1}=3.3V$, $V_{DD2}=7.7V$, $GND=V_{SS1}=V_{SS2}=0V$, $T_a=25^{\circ}C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency	Fclk	-	25	40	MHz
CLK Pulse Width	Tcw	25	40	-	ns
Data Set-up Time	Tsu	4	-	-	ns
Data Hold Time	Thd	2	-	-	ns
Propagation Delay of DIO2/1	Tphl	6	10	15	ns
Time That The Last Data to LD	Tld	1	-	-	Tcw
Pulse width of LD	Twld	2	-	-	Tcw
Time That LD to DIO1/2	Tlds	5	-	-	Tcw
POL Set-up Time	Tpsu	6	-	-	ns
POL Hold Time	Tphd	6	-	-	ns
OE Pulse Width	T _{OE} V	1	-	-	μs
CKV Pulse Width	T _{CKV}	500	-	-	ns
STV Set-up Time	T _{SUV}	400	-	-	ns
STV Hold Time	T _{HDV}	400	-	-	ns
Horizontal Display Period	T _{HDP}	-	640	-	Tcw
Horizontal Period Timing Range	T _{HP}	-	800	-	Tcw
Horizontal Lines Per Field	T _V	520	525	640	T _{HP}
Vertical Display Timing Range	T _{DV}	-	480	-	T _{HP}



11.2) Timing Diagram

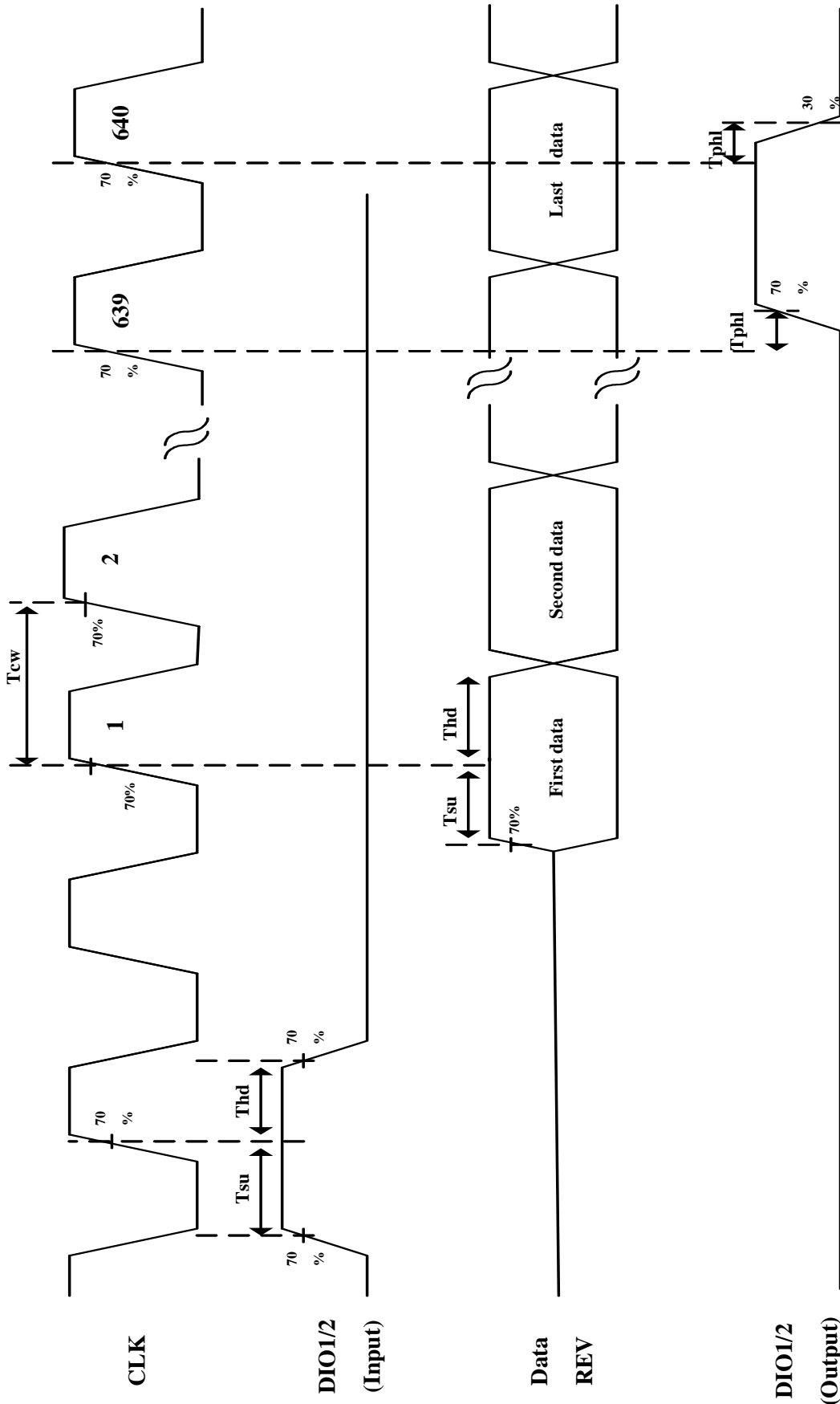


Fig. 11-1 Horizontal timing (1)

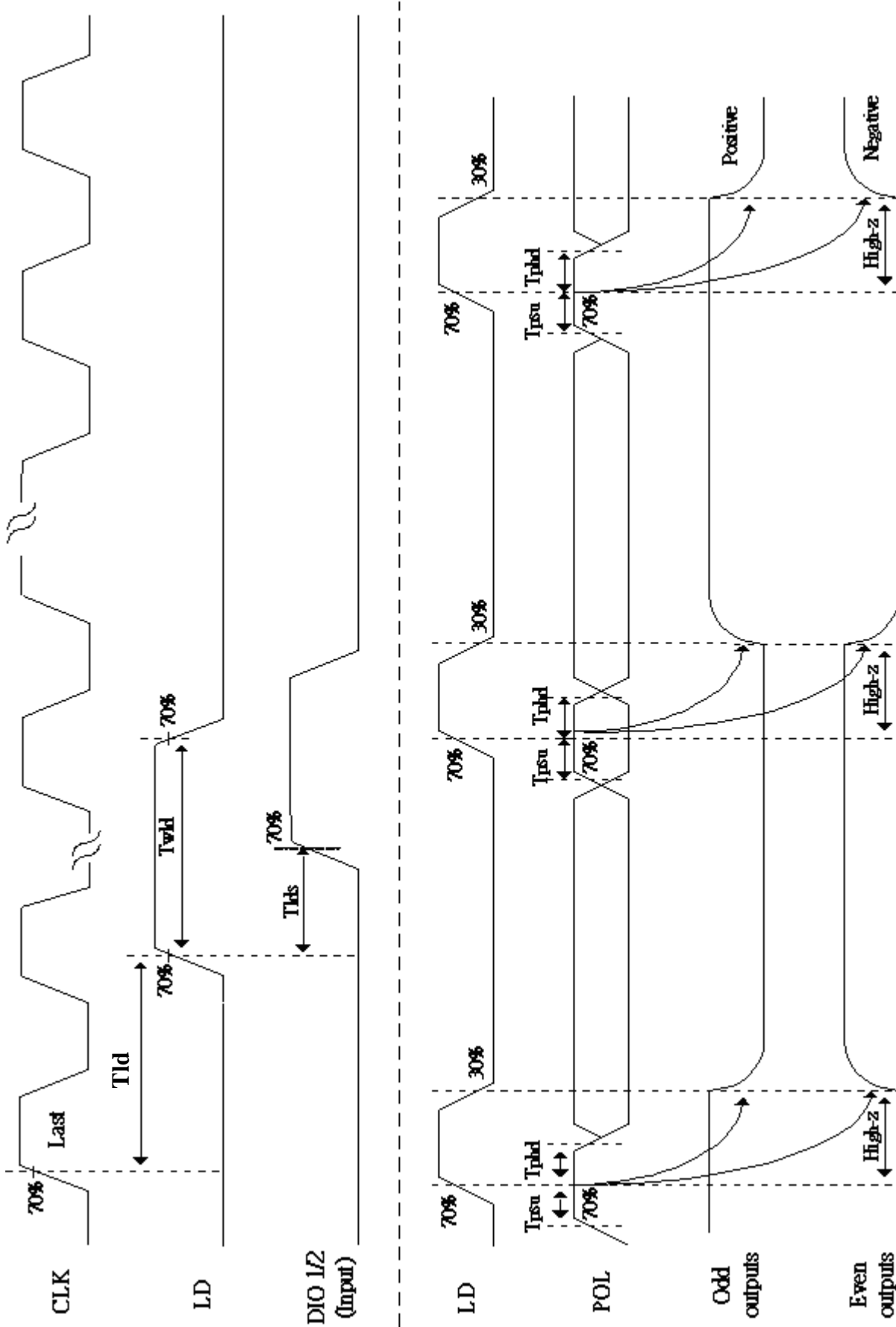


Fig. 11-2 Horizontal timing(2)

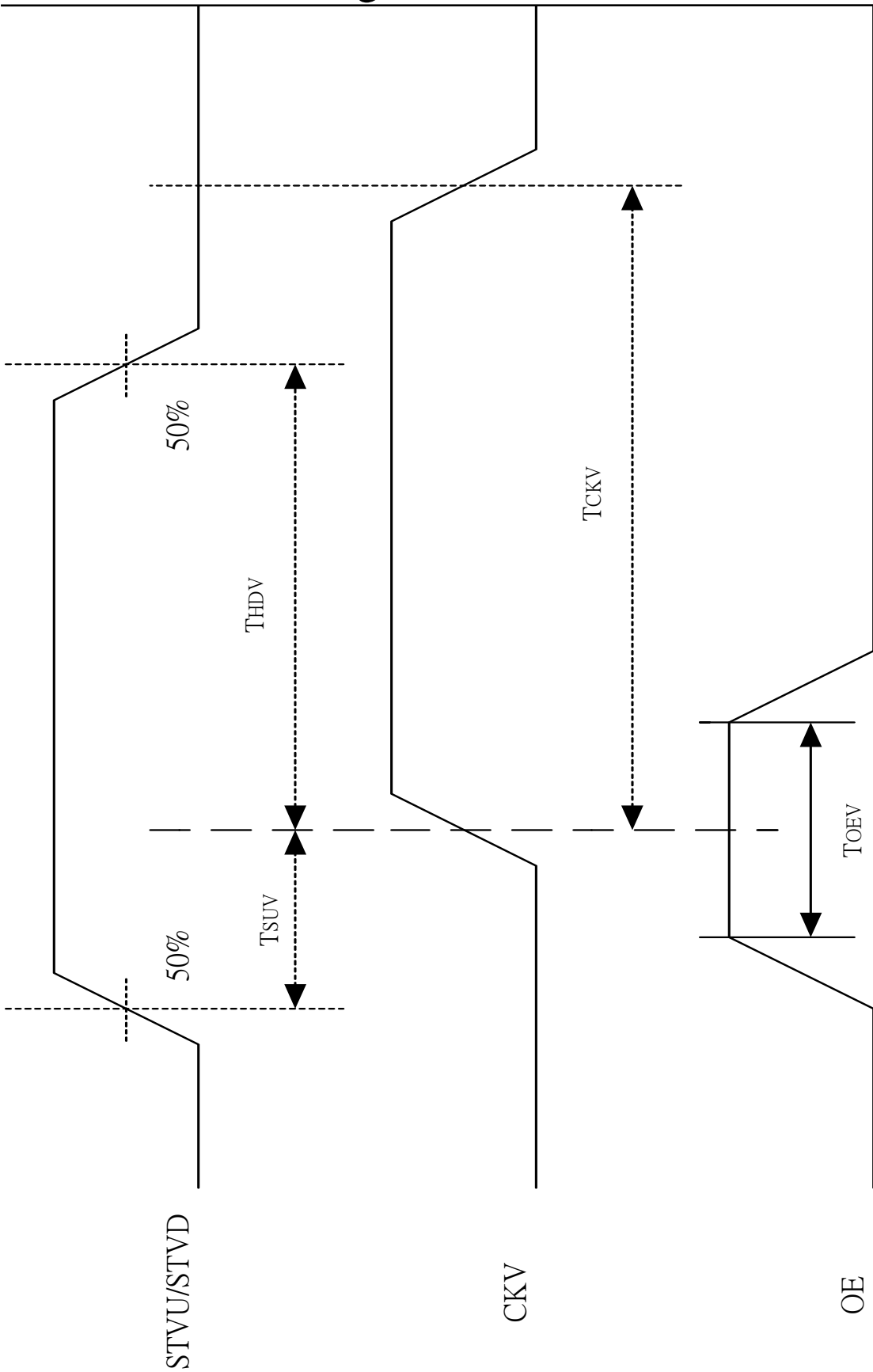


Fig. 11-3 Vertical shift clock timing

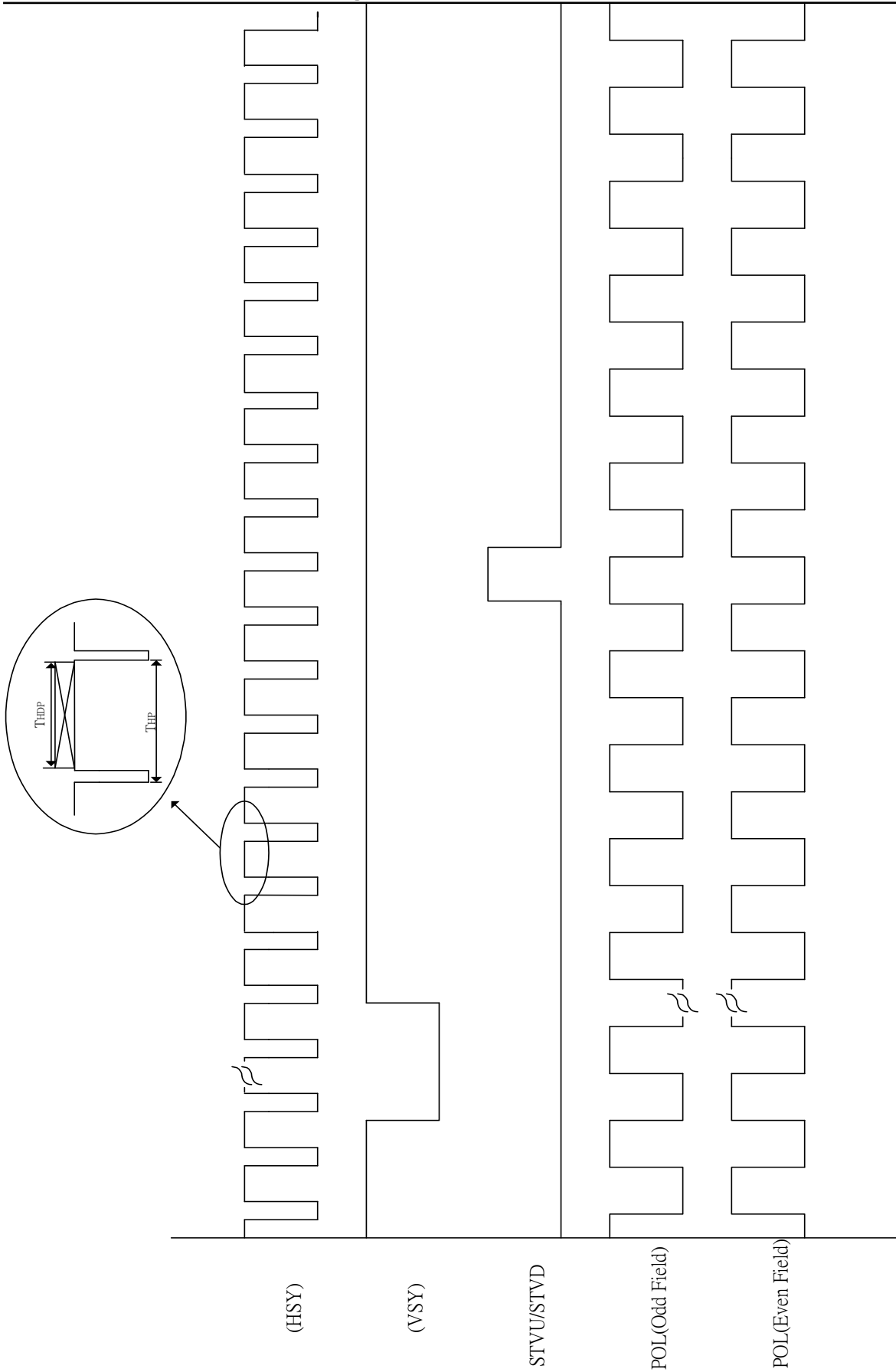
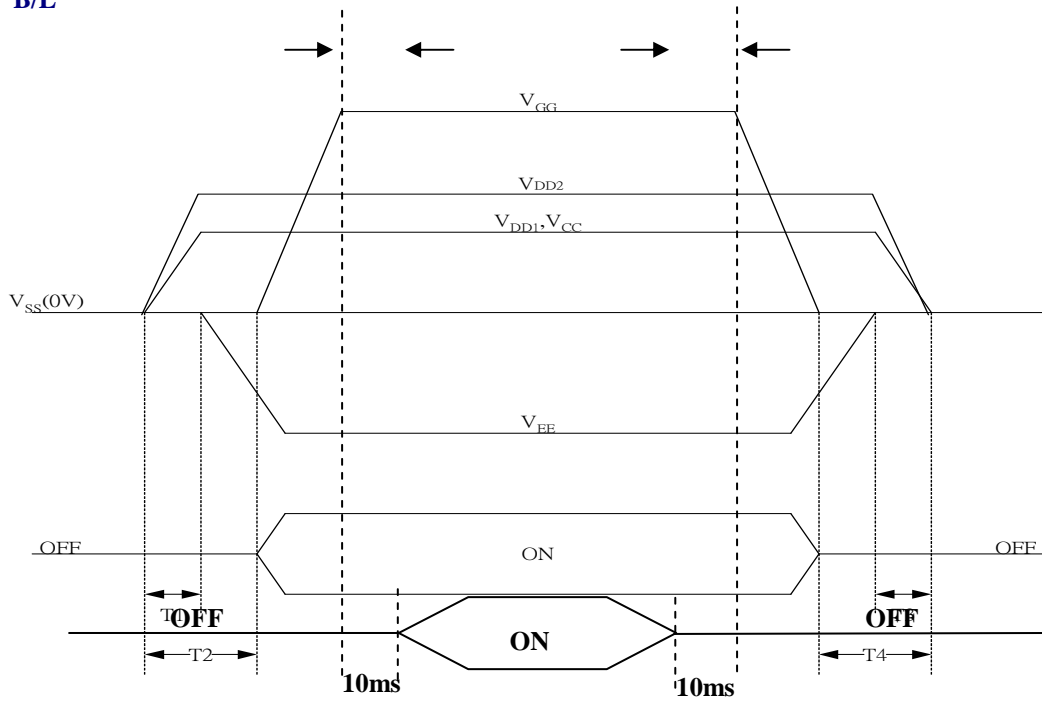


Fig. 11-4 Vertical timing



12. Power On Sequence

B/L



1. $10ms \leq T_1 < T_2$

2. $0ms < T_3 \leq T_4 \leq 10ms$

13. Optical Characteristics

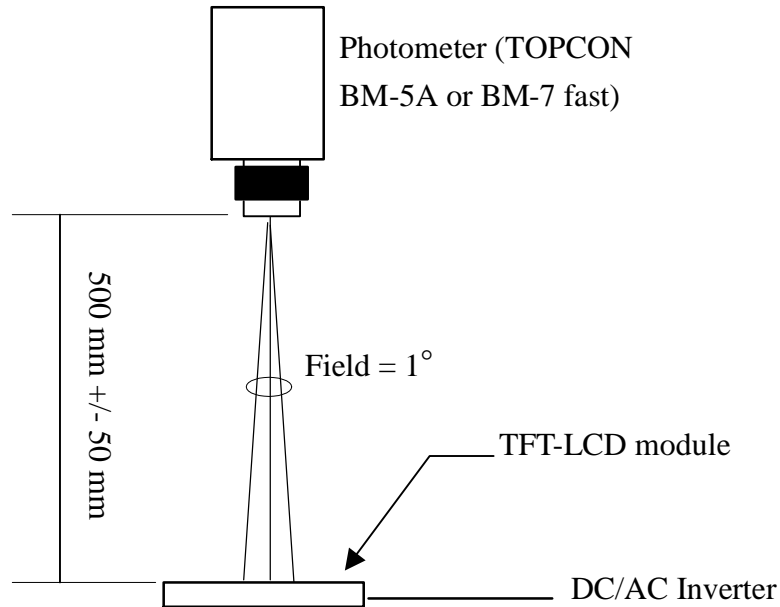
13-1) Specification:

Ta=25°C

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Vertical	θ 11,12	(70)	(75)		deg	Note 13-1
	Horizontal	θ 22 (3 o'clock)	(65)	(70)	-	deg	
		θ 21 (9 o'clock)	(45)	(50)	-	deg	
Contrast Ratio	CR		(200)	(4000)	-	-	Note 13-2
Response time	Rise	Tr	-	15	30	ms	Note 13-3
	Fall	Tf	-	25	50	ms	
Brightness	L	$\theta = 0^\circ / \varphi = 0$	(700)	(850)	-	cd/m ²	
Luminance Uniformity	U		70	75	-	%	Note 13-4
Lamp Life Time			20000	-	-	hrs	Note 13-6
White Chromaticity	x		TBD	TBD	TBD	-	
	y		TBD	TBD	TBD	-	
Cross Talk		$\theta = 0^\circ$	-	-	3.5	%	Note 13-5



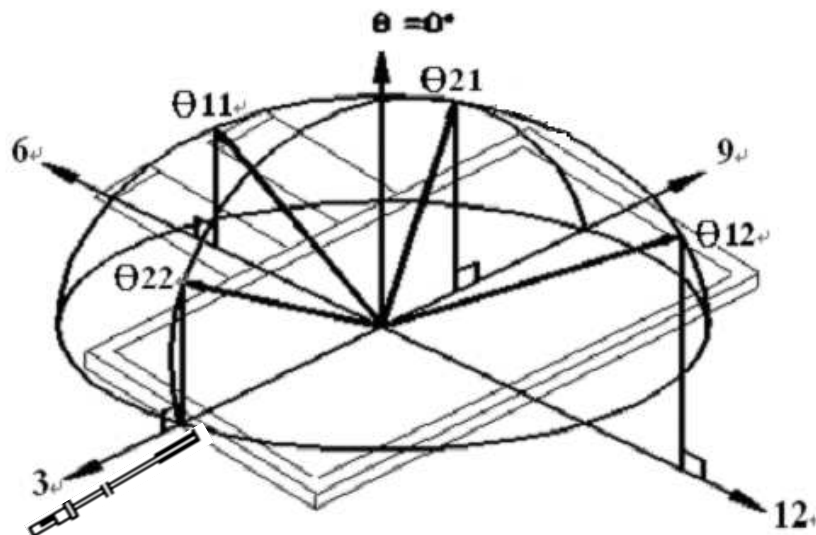
All the optical measurement shall be executed 30 minutes after backlight being turn-on. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.



Optical characteristics measuring configuration

Topcon BM-5A or BM-7 fast luminance meter 1° field of view is used in the testing (after 30 minutes' operation).

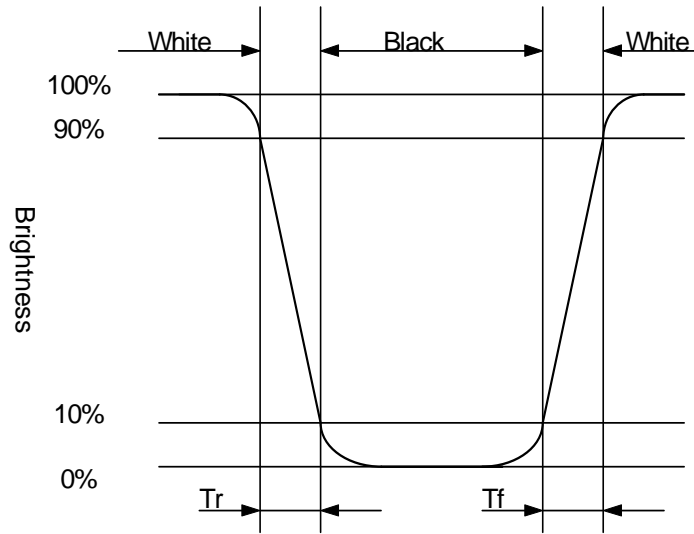
Note 13-1: The definitions of viewing angles are as follow





Note 13-2: The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 13-3: Definition of Response Time T_r and T_f :



Note 13-4: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

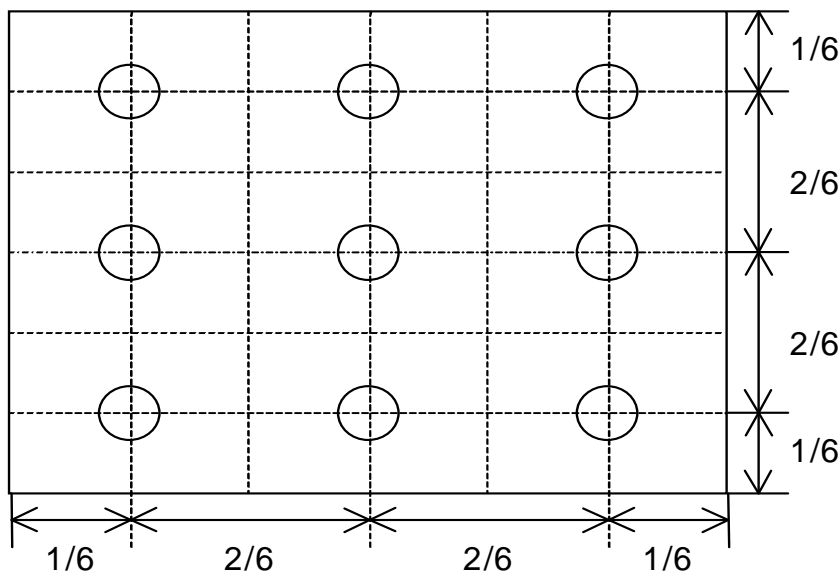
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).



$$\text{Note 13-5: Cross Talk (CTK)} = \frac{|Y_A - Y_B|}{Y_A} \times 100\%$$



YA: Brightness of Pattern A

YB: Brightness of Pattern B

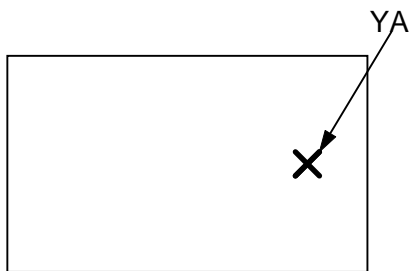
Luminance meter : BM 5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

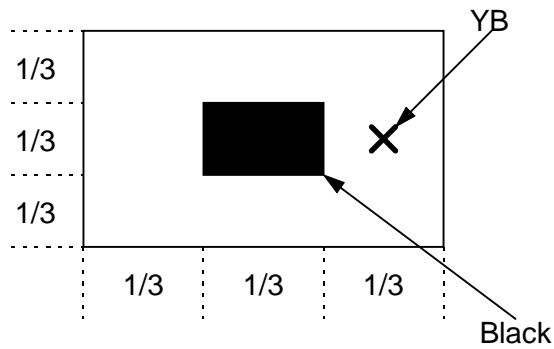
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

Pattern A
(Gray Level 31)



Pattern B
(Gray Level 31, central
black box exclusive)



X: Measuring Point (A and B are at the same point.)

(Gray Level 0)

Note 13-6: The “LED Life time “ is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25°C and I_{LED} =200mA



14. Handling Cautions

14-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- c) Protective film (Laminator) is applied on surface to protect it against scratches and dirt.
- d) Please following the tear off direction as figure14-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

14-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

14-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

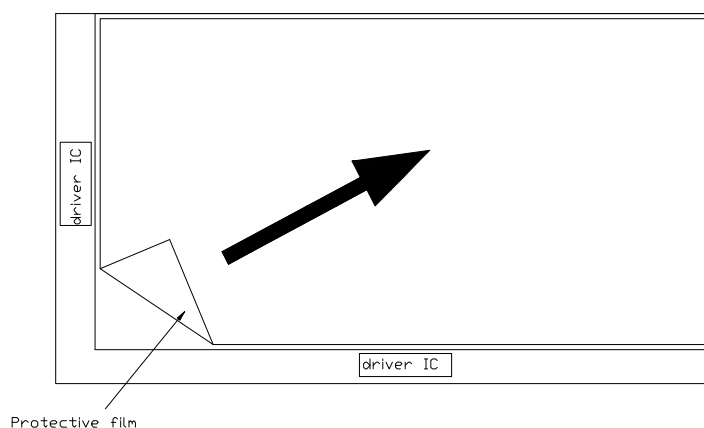


Figure 14-1 the way to peel off protective film

**15. Reliability Test**

No	Test Item	Test Condition	Remark
1	High Temperature Storage Test	Ta = +80°C, 240 hrs	
2	Low Temperature Storage Test	Ta = -30°C, 240hrs	
3	High Temperature Operation Test	Ta = +70°C, 240 hrs	
4	Low Temperature Operation Test	Ta = -20°C, 240hrs	
5	High Temperature & High Humidity Operation Test	Ta = +60°C, 90%RH, 240 hrs (No Condensation)	
6	Thermal Cycling Test (non-operating)	-30°C → +80°C, 100 Cycles 30min 30min	
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz, Amplitude : 1 mm Sweep time: 11 min Test Period: 6 Cycles for each direction of X, Y, Z	
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times	
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal	

Ta : ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (Including : line defect, no image) All the cosmetic specification is judged before the reliability stress.



16. Packing Diagram

TBD