

Version: 3.0

TECHNICAL SPECIFICATION
MODEL NO : PD035QX2

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Revision History

Rev.	Issued Date	Revised Contents
0.1	Nov 19, 2007	Preliminary
0.2	Apr 17, 2008	Add Page 22~43 Serial Interface/Command Table/ Command Description/ Gamma Adjustment Function
1.0	June 23, 2008	New
2.0	Mar 26, 2010	Modify Page22 Table 11.1 R/S & R/W setting
3.0	July.19.2010	Modify Page 7 6.Absolute Maximum Ratings:

***TECHNICAL SPECIFICATION
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1.Application

This data sheet applies to a color TFT LCD module, PD035QX2. The module applies to OA product, GPS, which require high quality flat panel display. If you must use in high reliability environment can't over reliability test condition.

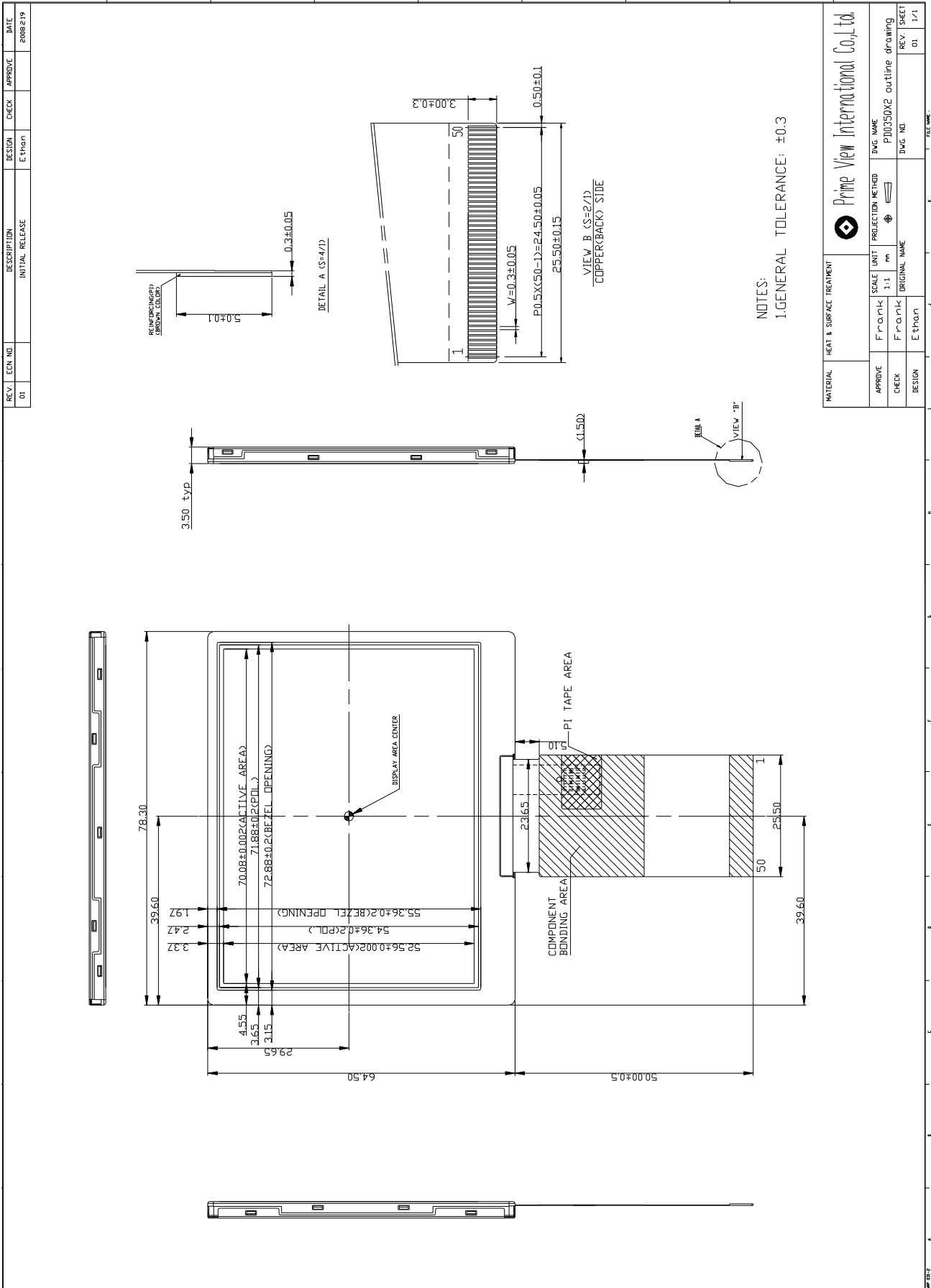
2. Features

- . Amorphous silicon TFT LCD panel with LED backlight unit
- . Pixel in stripe configuration
- . Thin and lightweight
- . Support digital 8-bits serial/24-bits parallel RGB and CCIR601/656 input mode.
- . Low current sleep mode and 8-color display mode for power saving.
- . Programmable gamma correction curve.
- . Non-Volatile Memory (OTP) for VCOM calibration
- . Programmable common electrode voltage amplitude and level.

3.Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.5(diagonal)	inch
Display Format	320×(R, G, B)×240	dot
Display Colors	262K	
Active Area	70.08(H)×52.56(V)	mm
Pixel Pitch	0.219(H)×0.219(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	78.3(H)×64.5(V)×3.5(D)	mm
Weight	36.2±4	g
Back-light	9-LEDs	
Surface treatment	Anti-glare + EWV	
Display mode	Normally white	
Gray scale inversion direction	6 o'clock [Note 16-1]	

4.Mechanical Drawing of TFT-LCD Module



REV.	ECN NO.	DESCRIPTION	DESIGN	CHECK	APPROVE	DATE
01		INITIAL RELEASE	E.than			2008.9.19

MATERIAL		HEAT & SURFACE TREATMENT		PRIME VIEW INTERNATIONAL CO., LTD.	
APPROVE	FRONT	SCALE UNIT	PROJECTION METHOD	DWG. NAME	DWG. NO.
CHECK	FRONT	1:1	1st	PD035QX2 outline drawing	
DESIGN	DESIGN	E.than	E.than		
				REV. SHEET	DI. 1/1

5.Input / Output Terminals

5-1) TFT-LCD Panel Driving

Pin No.	Symbol	Function	Remark
1	LED+	Supply voltage for LED Backlight	
2	LED- 1	Cathode of LED Backlight	
3	LED- 2	Cathode of LED Backlight	
4	LED- 3	Cathode of LED Backlight	
5	VSS	System Ground	
6	RESB	System Reset	Note 5-1
7	CSB	SPI enable	Note 5-2
8	SCK	SPI clock	
9	SDI	SPI data input	
10	BB0	Blue Data (LSB)	
11	BB1	Blue Data	
12	BB2	Blue Data	
13	BB3	Blue Data	
14	BB4	Blue Data	
15	BB5	Blue Data	
16	BB6	Blue Data	
17	BB7	Blue Data (MSB)	
18	VSS	System Ground	
19	GG0	Green Data (LSB)	
20	GG1	Green Data	
21	GG2	Green Data	
22	GG3	Green Data	
23	GG4	Green Data	
24	GG5	Green Data	
25	GG6	Green Data	
26	GG7	Green Data (MSB)	
27	VSS	System Ground	
28	RR0	Red Data (LSB)	
29	RR1	Red Data	
30	RR2	Red Data	
31	RR3	Red Data	
32	RR4	Red Data	
33	RR5	Red Data	
34	RR6	Red Data	
35	RR7	Red Data (MSB)	
36	VSS	System Ground	
37	DEN	Data enable	Note 5-3
38	HSYNC	Line synchronization signal	Note 5-4
39	VSYNC	Frame synchronization signal	
40	VSS	System Ground	
41	DOTCLK	Clock in	
42	VSS	System Ground	
43	SHUT	Sleep mode work on HI	Note 5-5
44	TB	HI : G0~G239 Low : G239~G0	Note 5-6
45	RL	HI : First RGB data at S0~S2 Low : First RGB data at S959~S957	Note 5-7
46	VSS	System Ground	
47	VDD	Power supply for Logic Circuit	Note 5-8
48	VSSA	Grounding for analog circuit	
49	VDDA	Voltage supply pin for analog circuit	Note 5-9
50	VSSA	Grounding for analog circuit	

Note 5-1: Low active, connect to VDD when not used

Note 5-2: Refer to Serial Interface block. Leave it OPEN when not used.

Note 5-3: Connect to VDD or floating if not used

Note 5-4: Fixed to VDD or floating if not used

Note 5-5: Connect to VDD for sleep mode, VSS for normal operation mode

Note 5-6: Connect to VDD for scan from G0 to G239 (normal scan), VSS for G239 to G0 (reverse scan)

Note 5-7: Connect to VDD for display first RGB data at S0-S2, VSS for S959-S957

Note 5-8: VDD (Typ.) = +3.3V

Note 5-9: VDDA (Typ.) = +3.3V. Requires a noise free path for providing accurate LCD driving voltage

6. Absolute Maximum Ratings:

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

Item	Symbol	Value	Unit
Supply voltage (Analog)	VDDA	VSS- 0.3 to 3.6	V
Supply voltage (Logic)	VDD	-0.3 ~ +3.6	V
Storage Temperature	Tst	-40 ~ +95	°C
Operation Temperature	Top	-30 ~ +85	°C

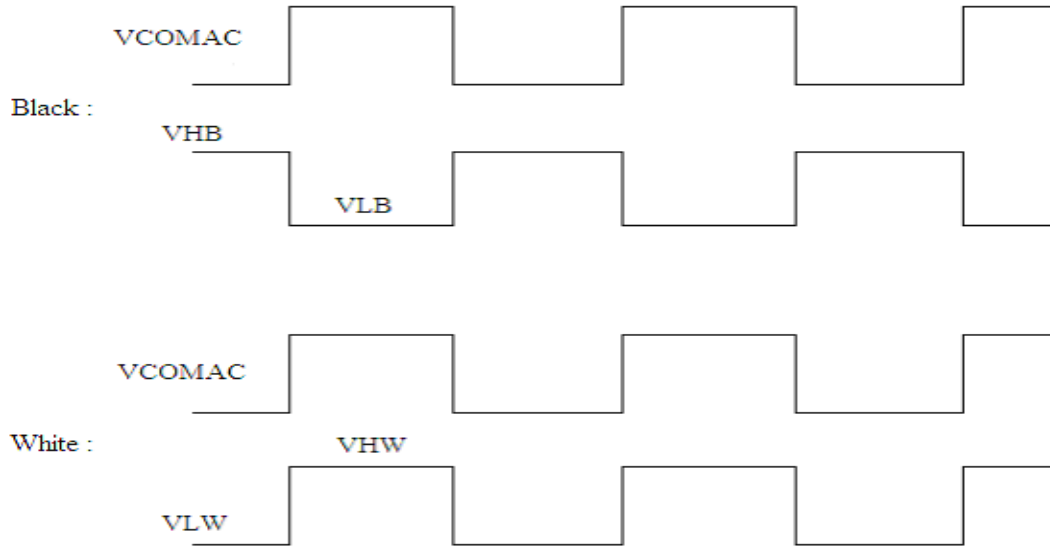
7. Electrical Characteristics

7-1) Recommended Operating Conditions:

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage (Analog)	VDDA	3.0	3.3	3.6	V	
Supply voltage (Logic)	VDD	3.0	3.3	3.6	V	
V _{COM}	VCOMAC	-	6	-	V _{P-P}	AC Component of V _{COM}
	VCOMDC	0.6	1.6	2.6	V	DC Component of V _{COM} Note 7-1
Black of Video Low Voltage	VLB	-	0.56	-	V	Note 7-2
Black of Video High Voltage	VHB	-	4.4	-	V	
White of Video Low Voltage	VLW	-	0.56	-	V	
White of Video High Voltage	VHW	-	4.4	-	V	

Note7-1 : VCOM must be adjusted optimize display quality, crosstalk, contrast ration and etc.

Note7-2 :



7-2) Recommended Driving Condition for Back Light

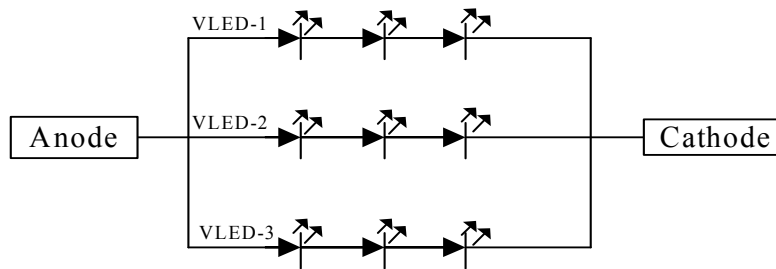
Ta = 25°C

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V _{LED}	-	-	(10.8)	V	Note 7-3
Supply current of LED backlight	I _{LED}	-	20	-	mA	Note 7-4
Backlight Power Consumption	P _{LED}	-	-	648	mW	Note 7-3/7-5

Note 7-3 : I_{LED}= 20mA, constant current

Note 7-4 : The LED driving condition is defined for each LED module. (3 LED Serial)
 Input current = 20mA * 3 = 60mA

Note 7-5 : P_{LED} = V_{LED-1} * I_{LED-1} + V_{LED-2} * I_{LED-2} + V_{LED-3} * I_{LED-3}

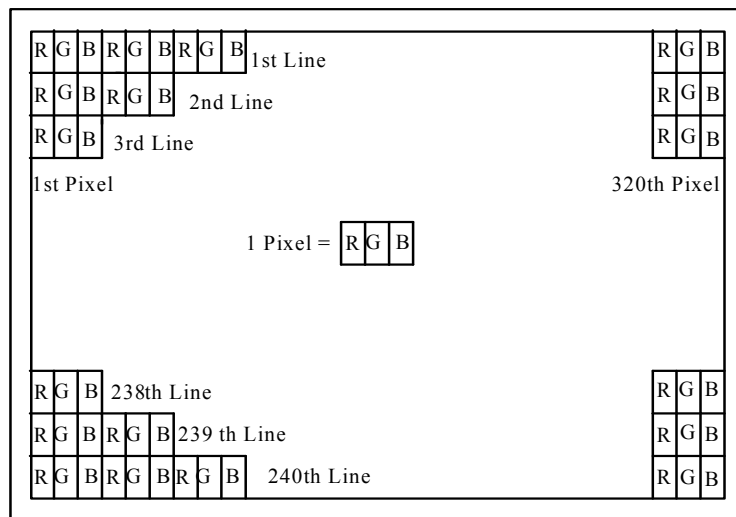


7-3) Power Consumption

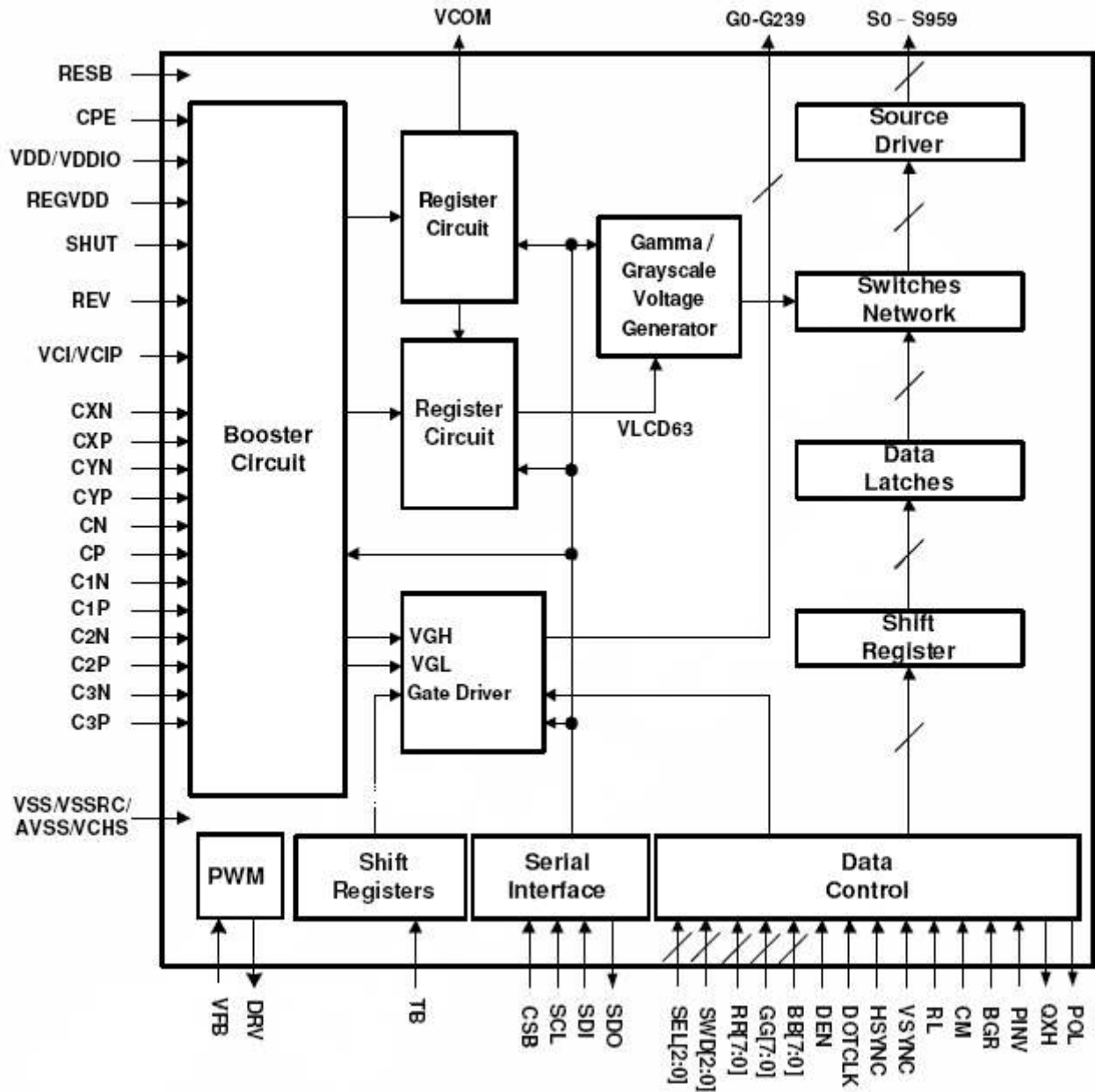
Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply voltage (Logic)	I _{DD}	V _{DD} = 3.3V	0.1	0.3	mA	
Supply voltage (Analog)	I _{DDA}	V _{DDA} = 3.3V	12.2	36.6	mA	
Panel Power Consumption	-	-	40.6	121.8	mW	
Back Light Power Consumption			-	648	mW	
Total Power Consumption			-	769.8	mW	Note 7-6

Note 7-6: Back light power consumption is calculated by I_L×V_L.

8. Pixel Arrangement



9. Block Diagram



10. AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 3.3V, T_A = 25°C)

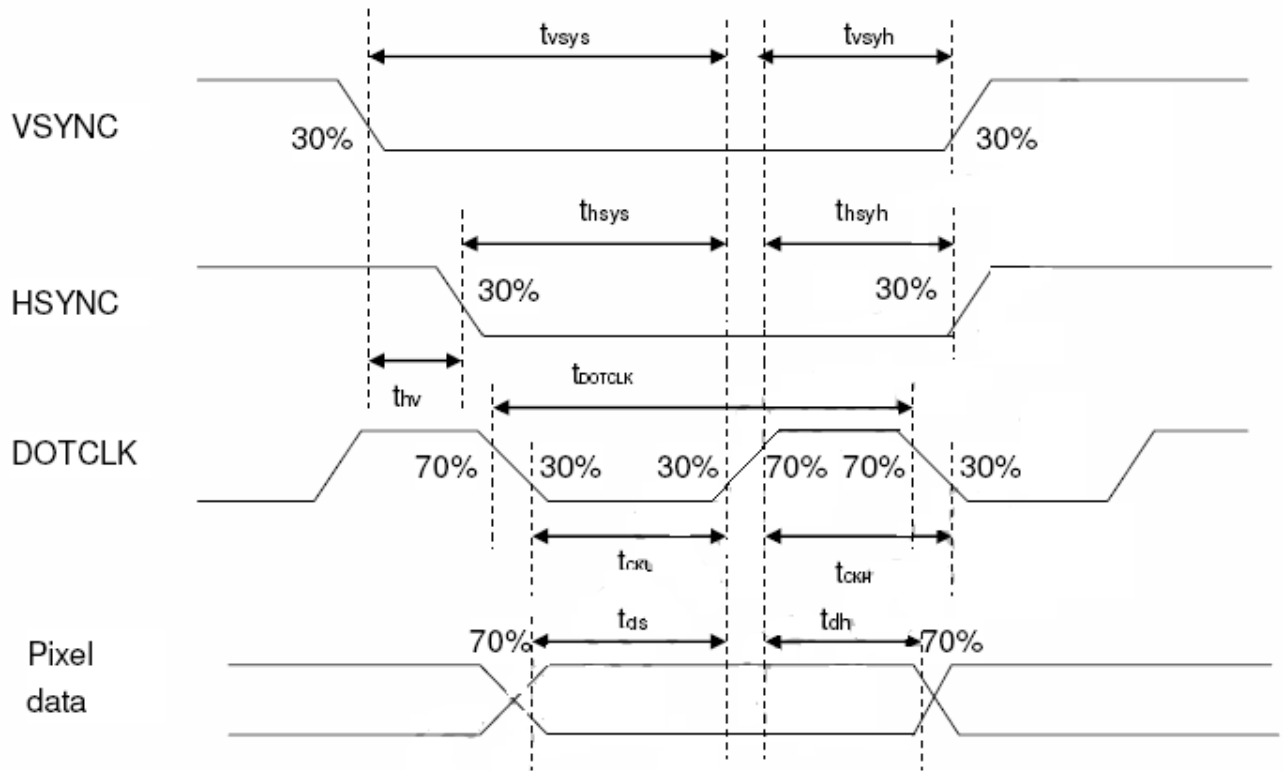


Figure 10.1 Pixel Timing

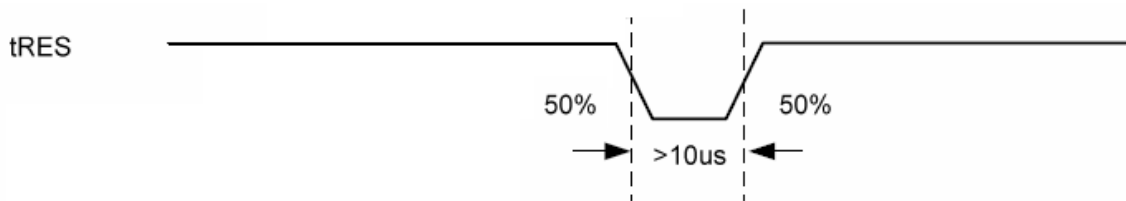
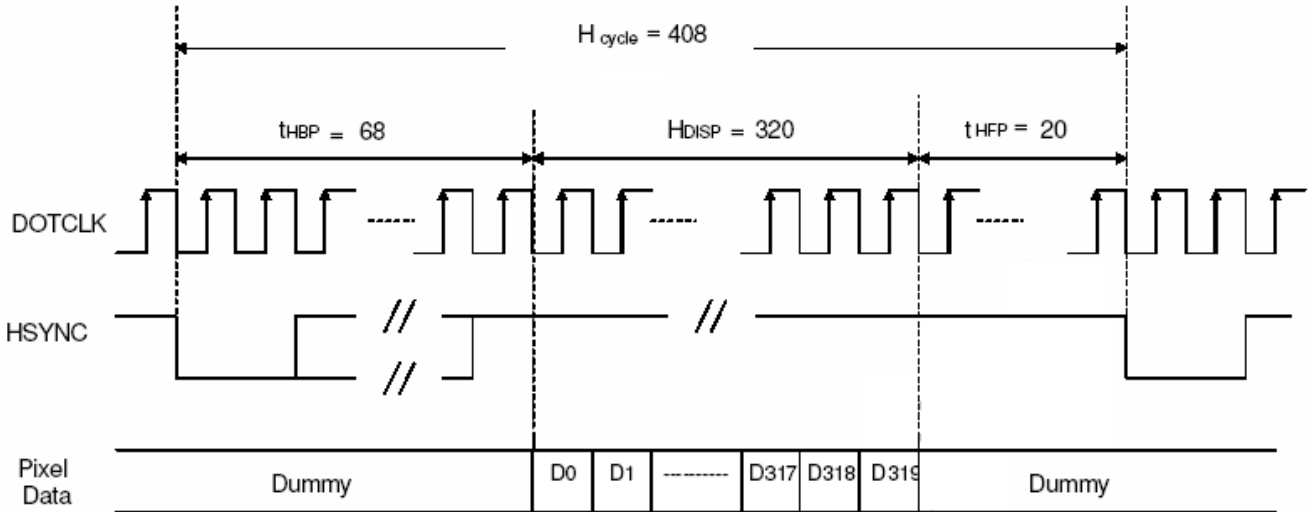


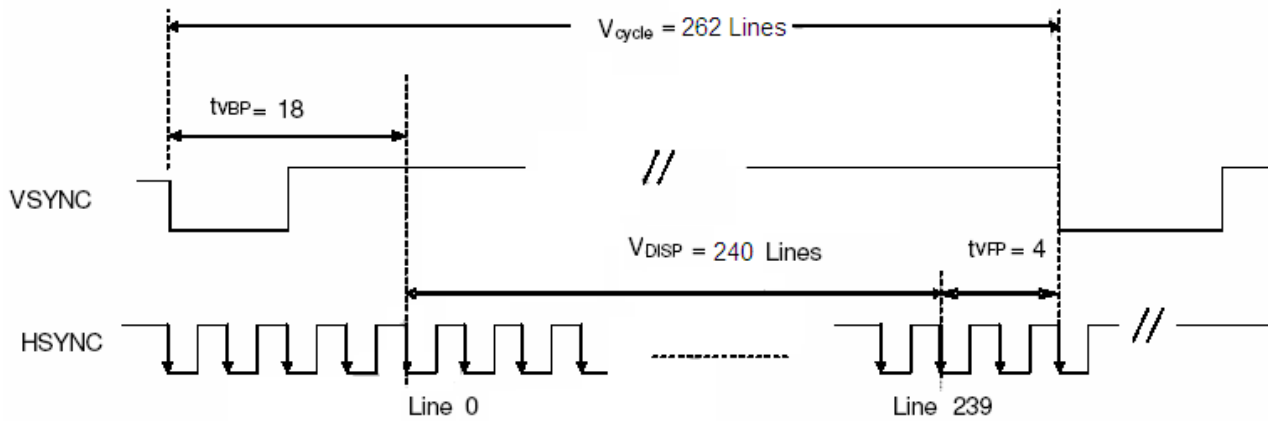
Figure 10.2 tRES Timing

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Vertical Sync Setup Time	tvsys	20	10	-	-	-	-	ns
Vertical Sync Hold Time	tvsyh	20	10	-	-	-	-	ns
Horizontal Sync Setup Time	thsys	20	10	-	-	-	-	ns
Horizontal Sync Hold Time	thsyh	20	10	-	-	-	-	ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-	-	-	-	ns
DOTCLK High Period	tCKH	50	15	-	-	-	-	ns
Data Setup Time	tds	12	8	-	-	-	-	ns
Data hold Time	tdh	12	8	-	-	-	-	ns
Reset pulse width	tRES	10		-		-		us

Table 10.1 Pixel & tRES Timing



a) Horizontal Data Transaction Timing



b) Vertical Data Transaction Timing

Figure 10.3 Data Transaction Timing in Parallel RGB (24 bit) Interface (SYNC Mode)

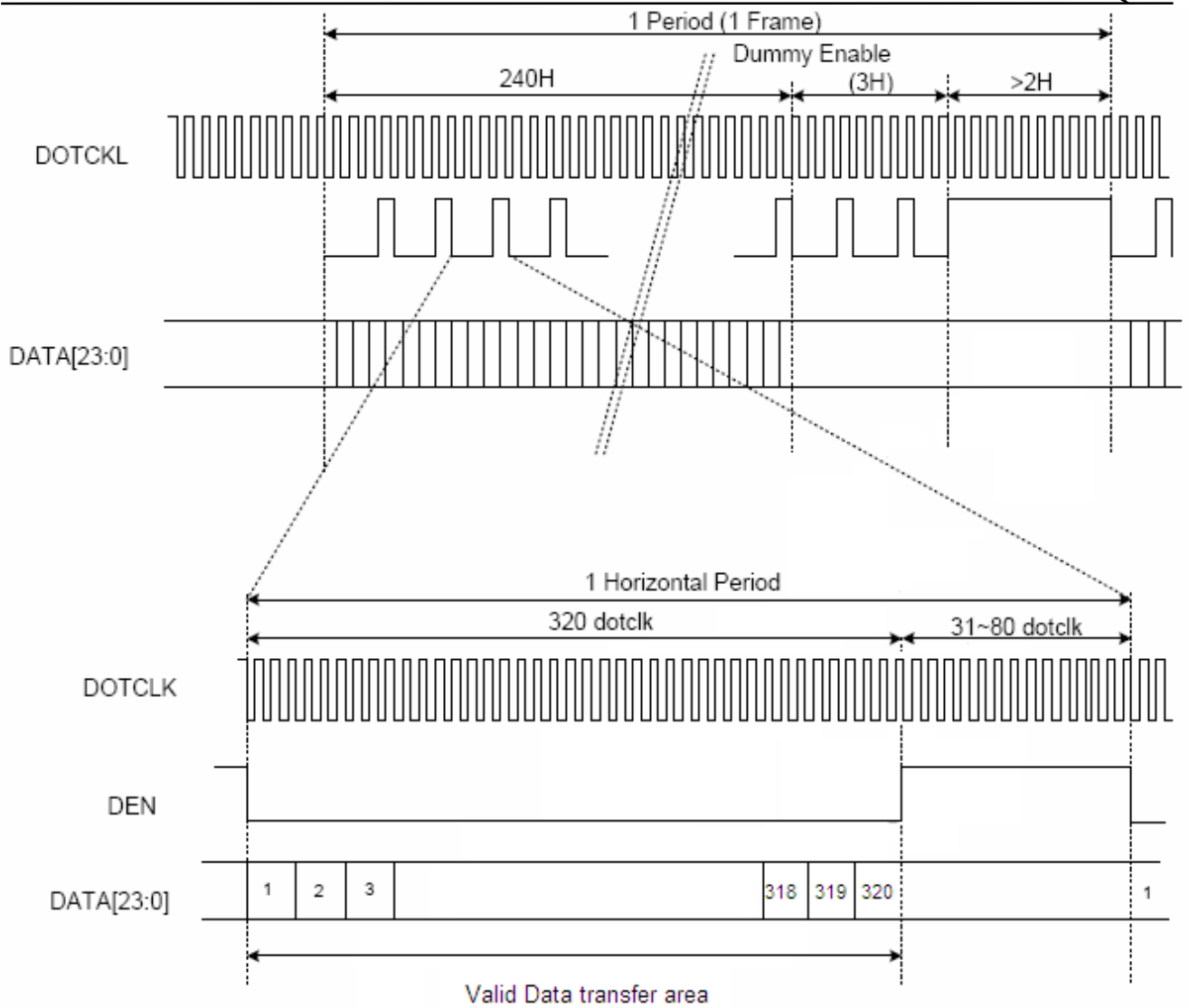
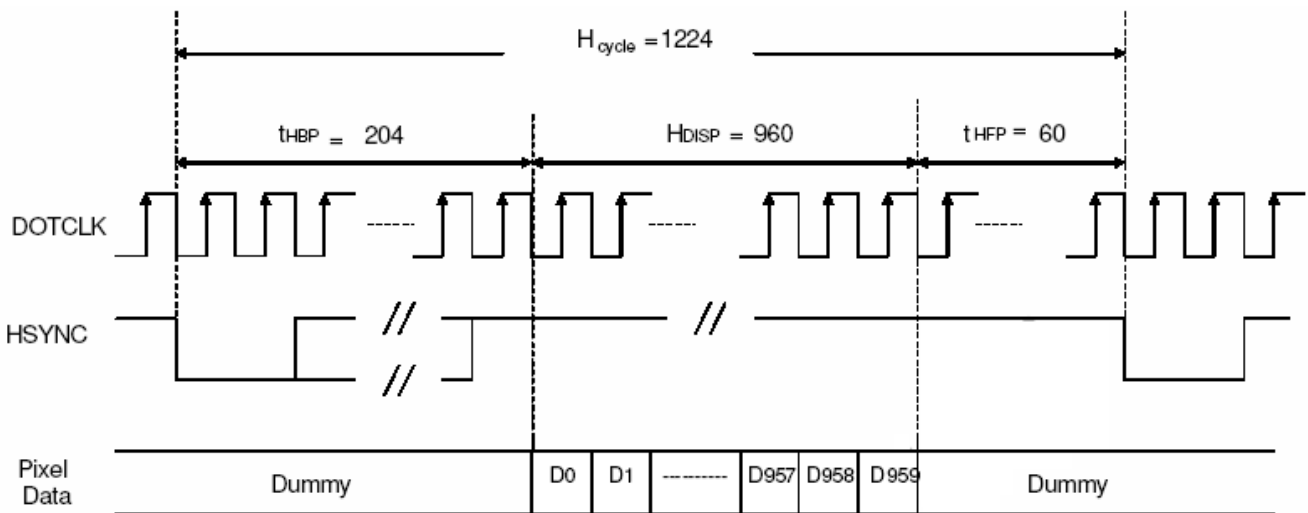


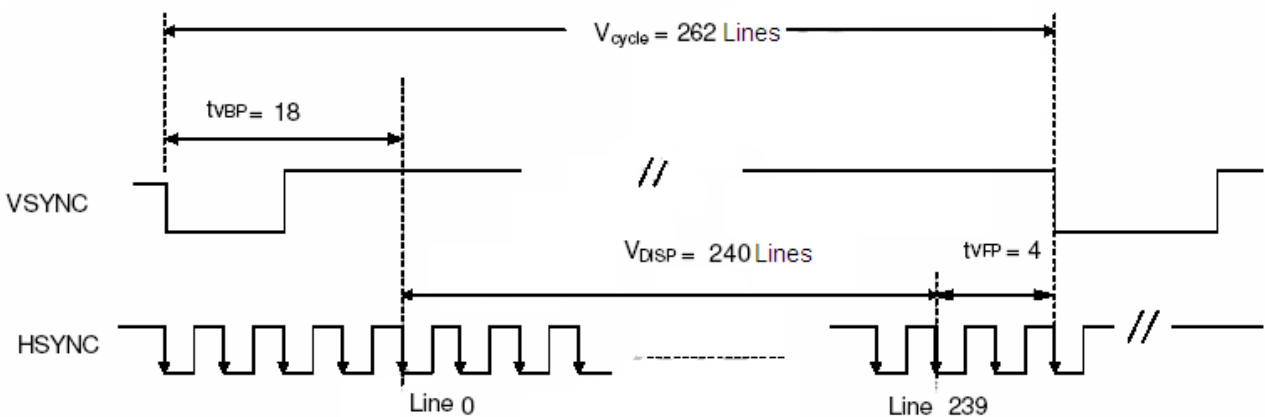
Figure 10. 4 Data Transaction Timing in Parallel RGB (24 bit) Interface (DE Mode)

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	tDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)	fH	-		15.72		22.35		KHz
Vertical Frequency (Refresh)	fV	-		60		90		Hz
Horizontal Back Porch	tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Front Porch	tHFP	-	-	20	60	-	-	tDOTCLK
Horizontal Data Start Point	tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Blanking Period	tHBP + tHFP	-	-	88	264	-	-	tDOTCLK
Horizontal Display Area	HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle	Hcycle	-	-	408	1224	450	1350	tDOTCLK
Vertical Back Porch	tVBP	-		18		-		Lines
Vertical Front Porch	tVFP	-		4		-		Lines
Vertical Data Start Point	tVBP	-		18		-		Lines
Vertical Blanking Period	tVBP + tVFP	-		22		-		Lines
VS pulse width	tWV	-		4		-		Lines
Vertical Display Area	NTSC	-		240		-		Lines
	PAL	-		280(PALM=0) 288(PALM=1)		-		
Vertical Cycle	NTSC	-		262		350		Lines
	PAL	-		313		350		

Table 10. 2 Data Transaction Timing in Normal Operating Mode



a) Horizontal Data Transaction Timing



b) Vertical Data Transaction Timing

Figure 10.5 Data Transaction Timing in Serial RGB (8 bit) Interface (SYNC Mode)

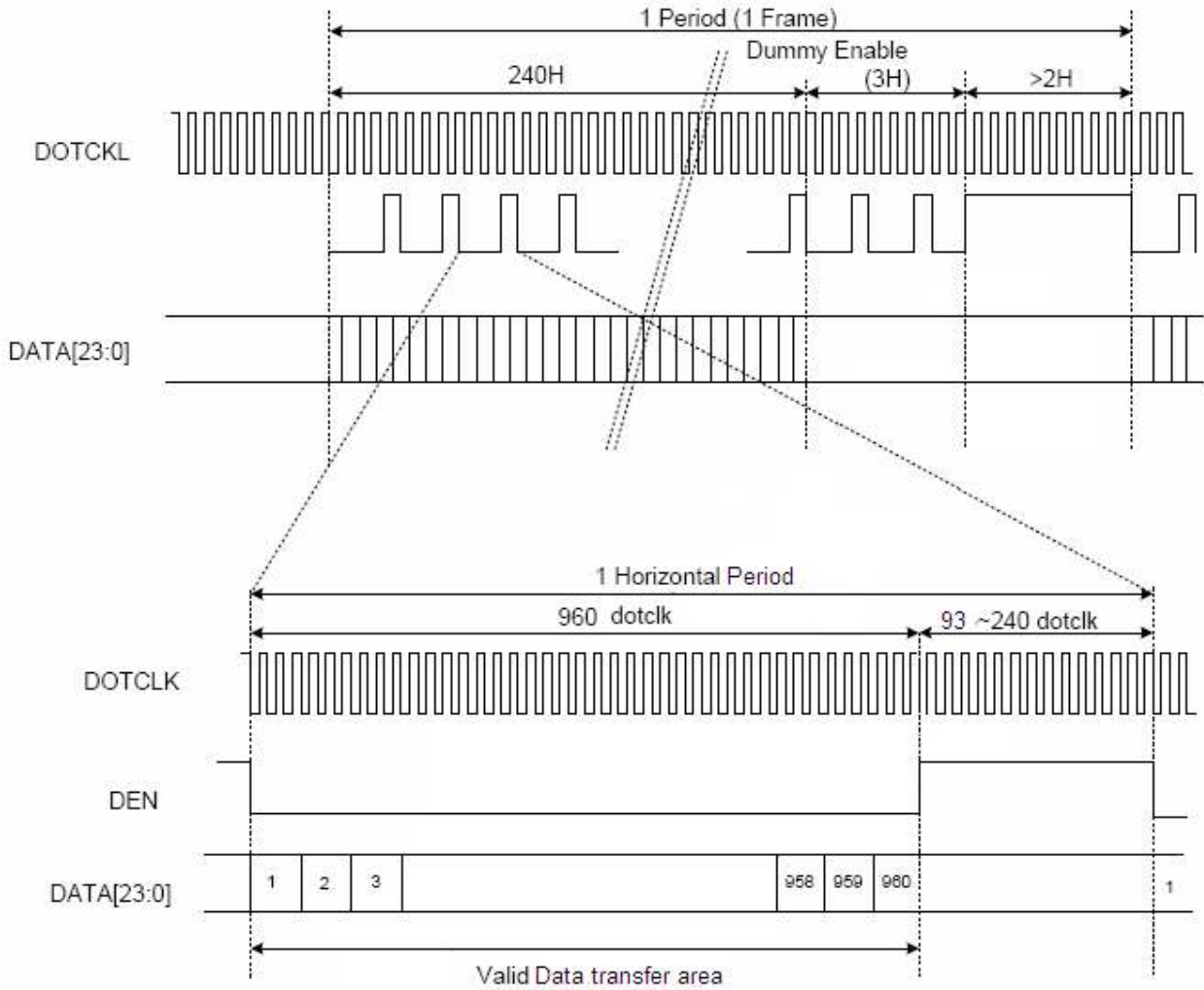
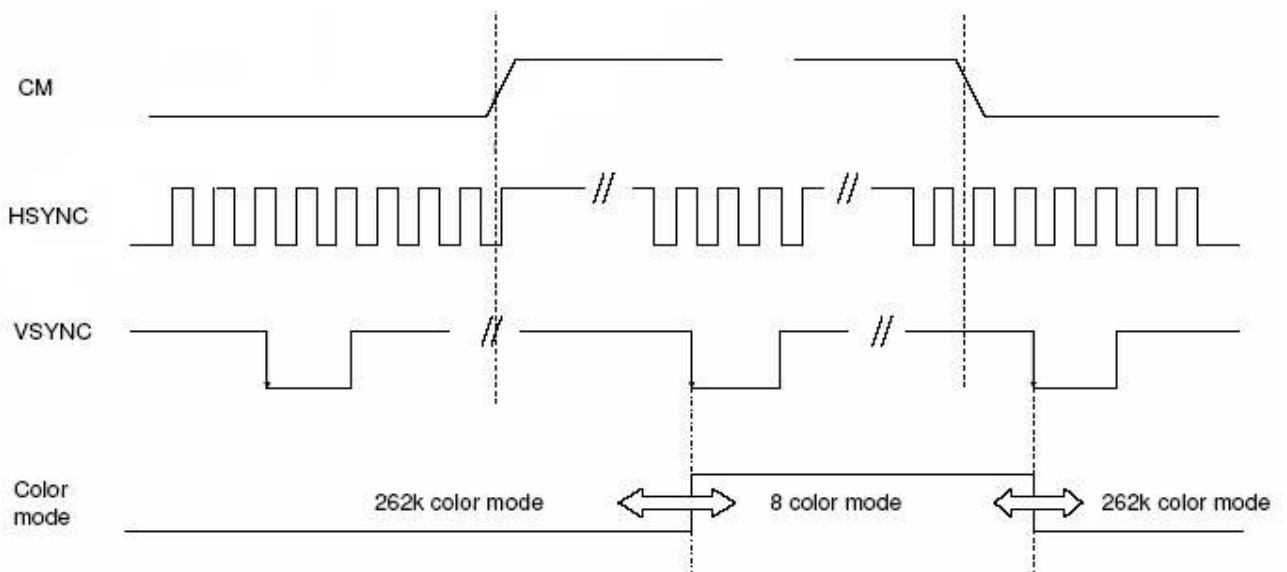


Figure 10. 6 Data Transaction Timing in Serial RGB (8 bit) Interface (DE Mode)



Note: The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.

Figure 10. 7 Color Mode Conversion Timing

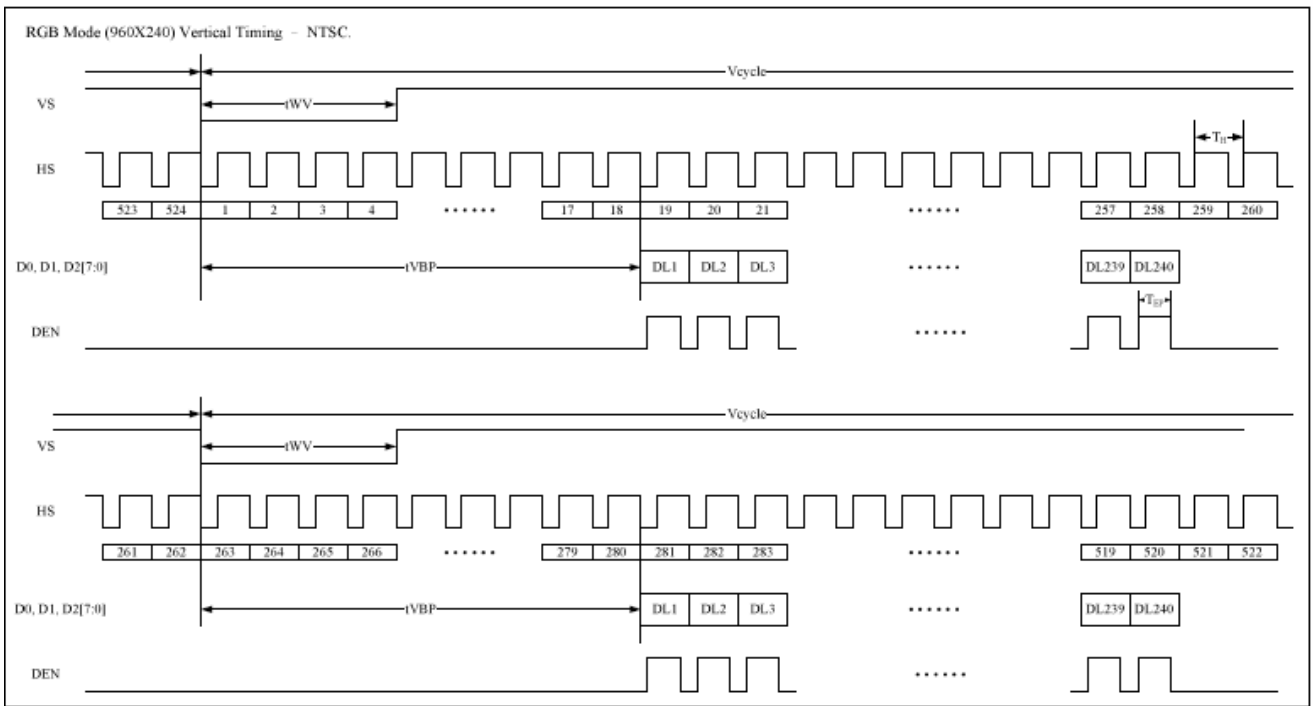


Figure 10. 8 Digital RGB NTSC mode Vertical Data Format for 262T_H

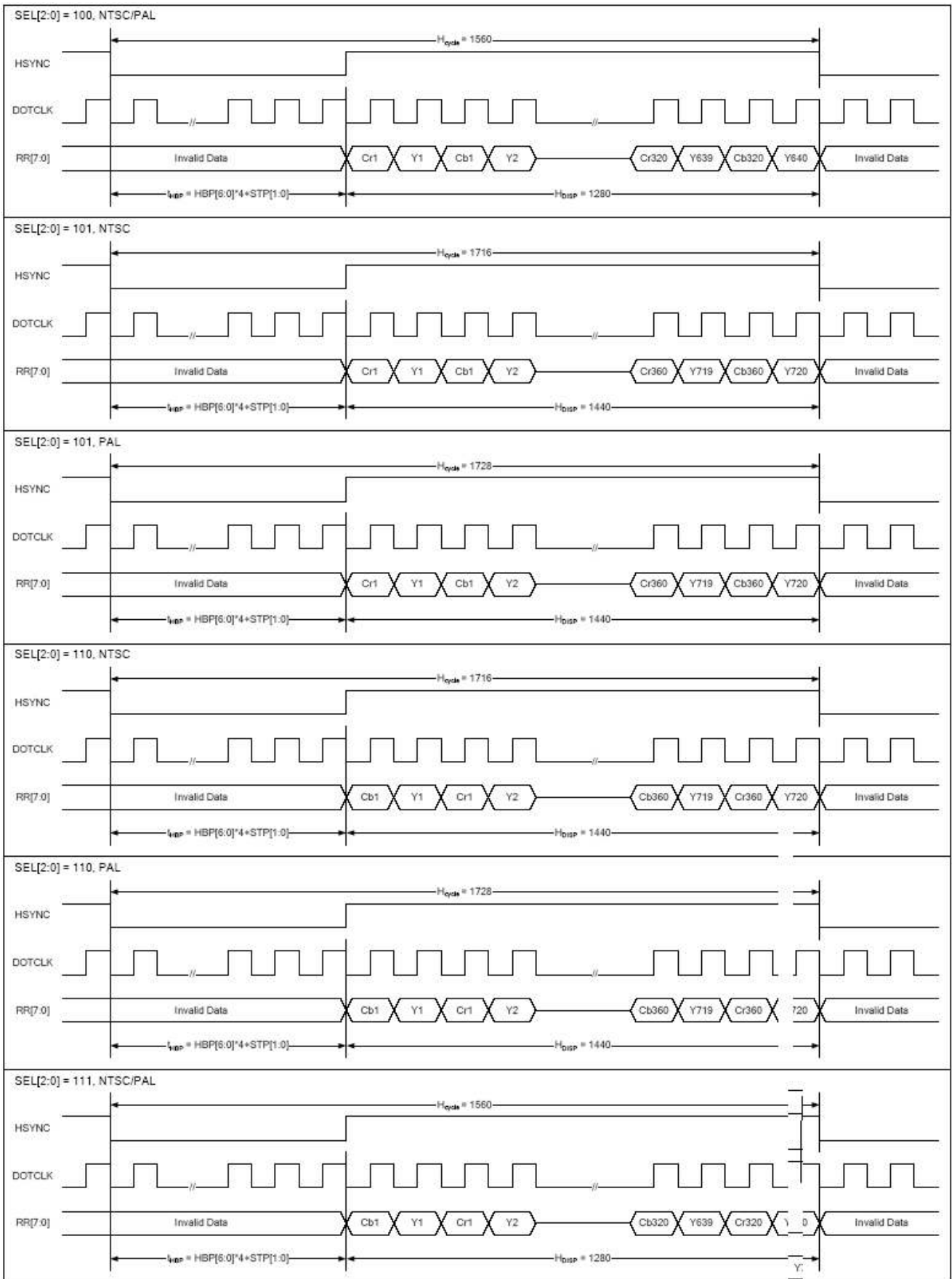


Figure 10. 9 CCIR601 Horizontal Timing

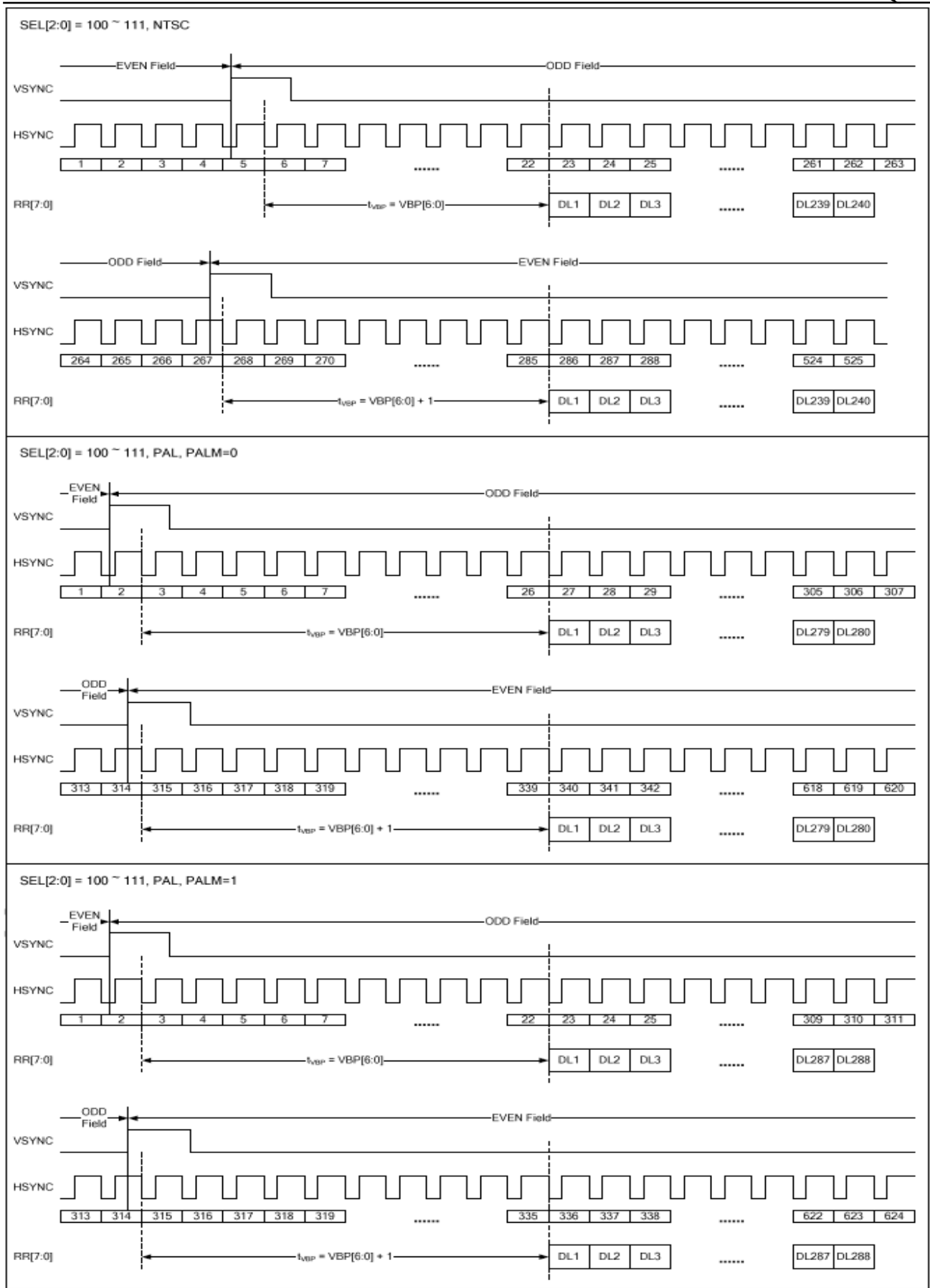


Figure 10. 10 CCIR601 Vertical Timing

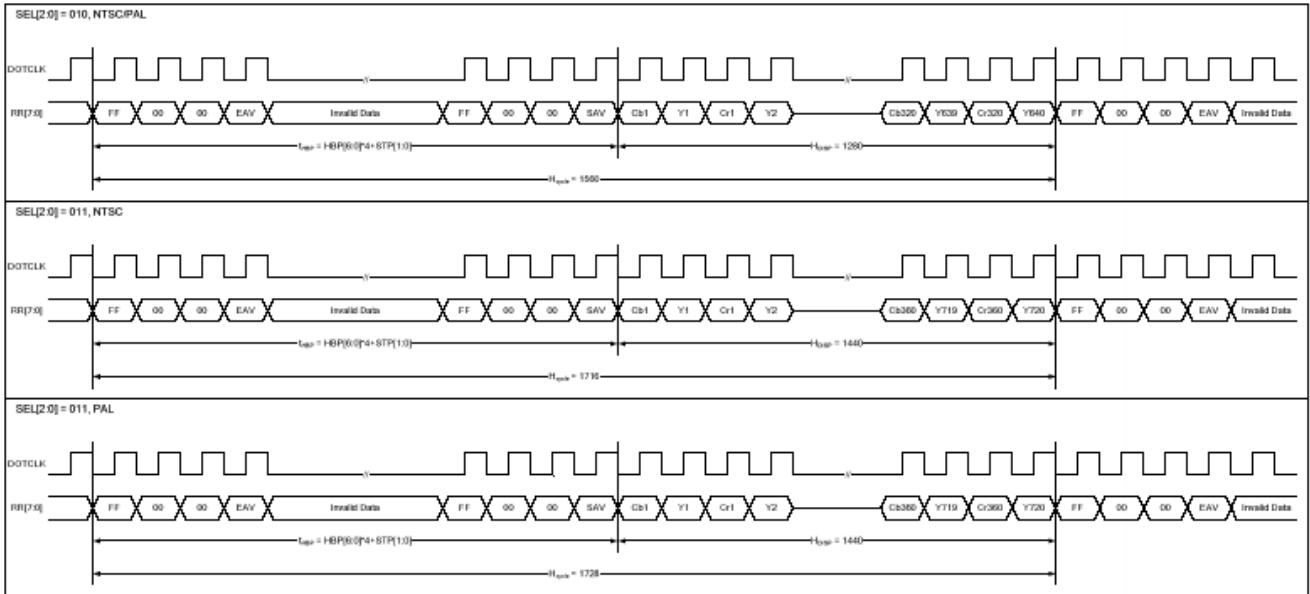


Figure 10. 11 CCIR656 Horizontal Timing

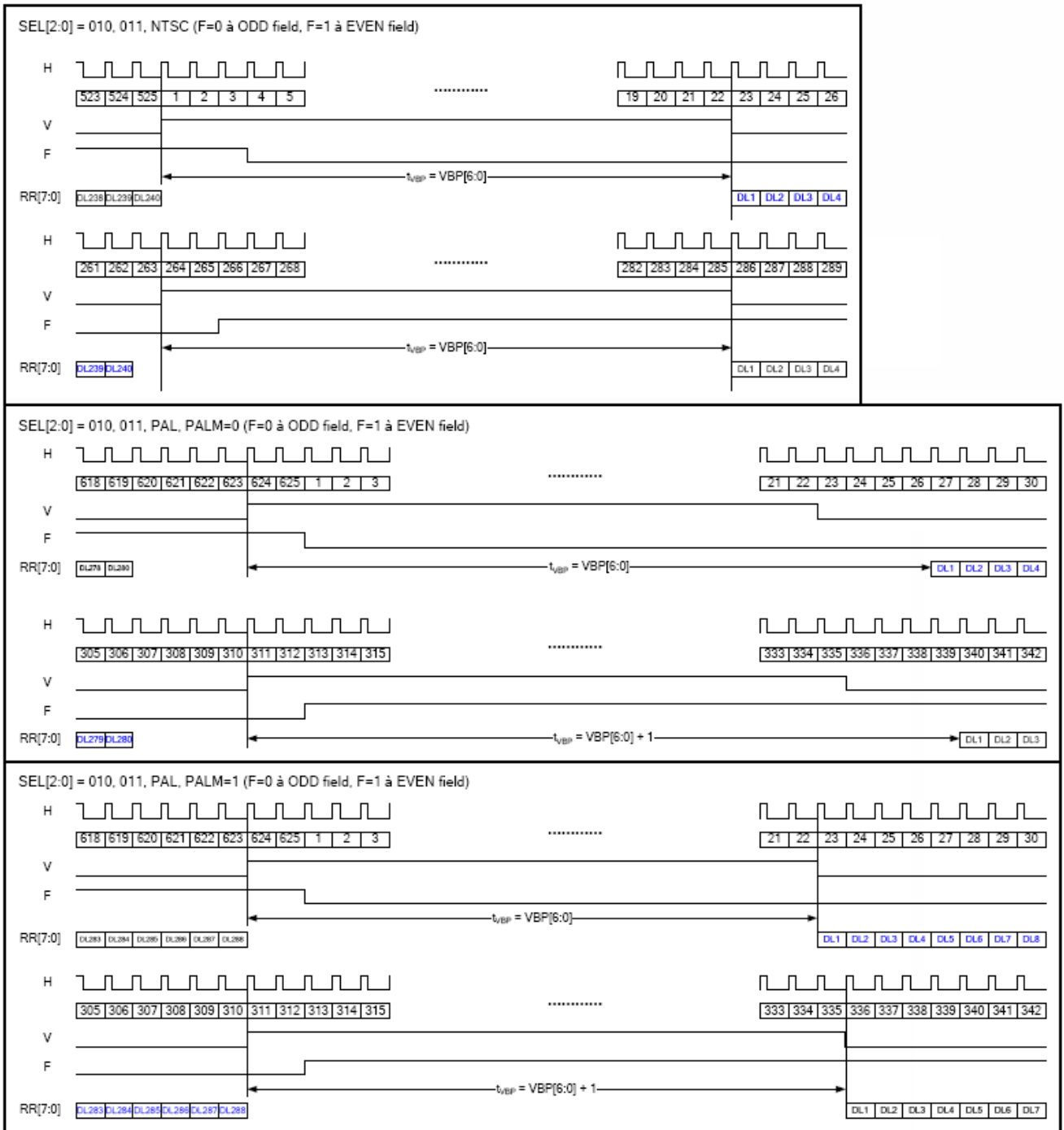
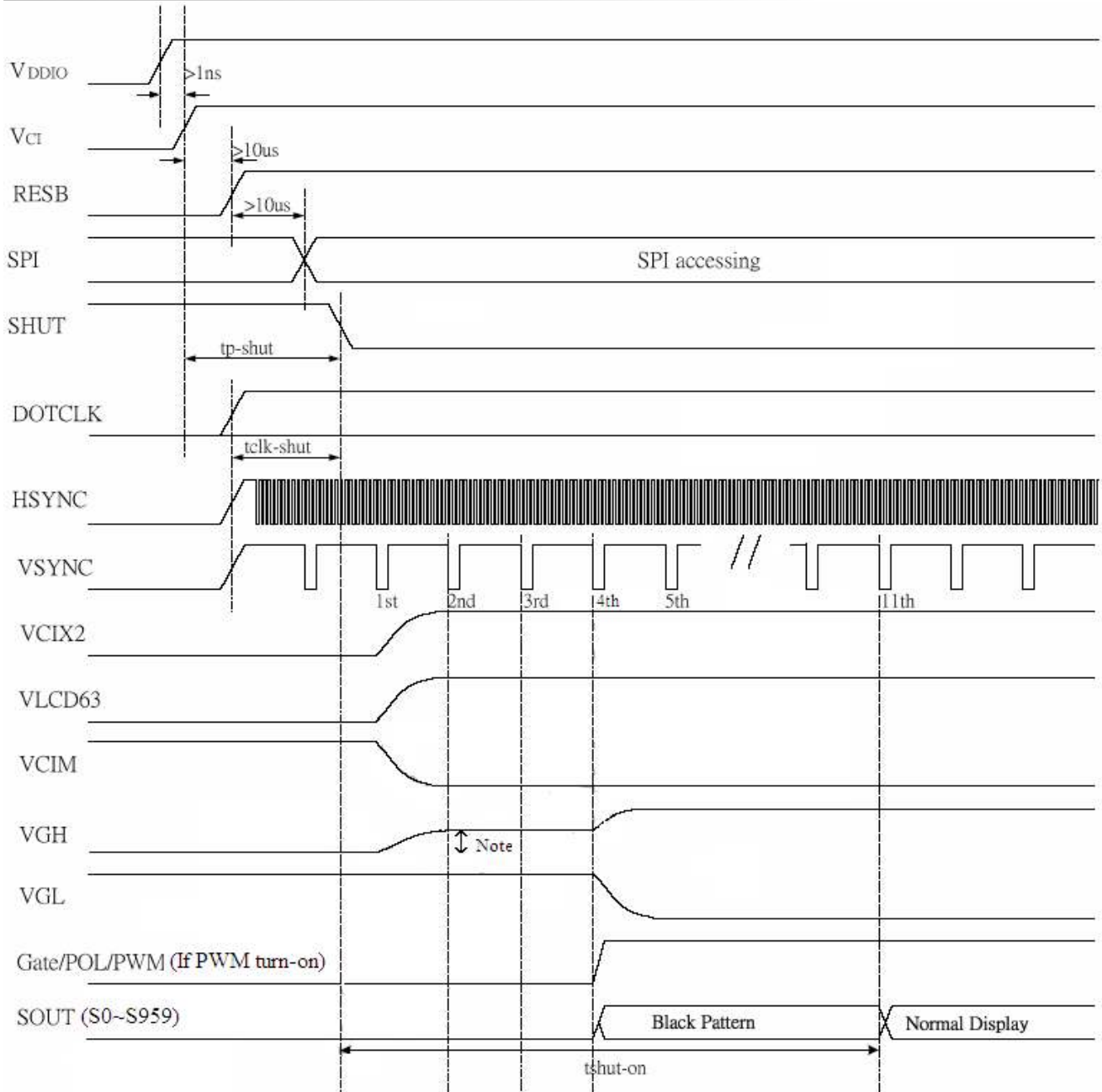


Figure 10. 12 CCIR656 Vertical Timing



Note: There is a diode between VCIX2 and VGH. Switch on VCIX2 will move VGH up.

Figure 10. 13 Power Up Sequence

Characteristics	Symbol	Min.	Typ.	Max.	Unit
VCI/ VDDIO on to falling edge of SHUT	tp-shut	1	-	-	us
DOTCLK to falling edge of SHUT	tclk-shut (Note1)	1	-	-	clk
Falling edge of SHUT to display start - 1 line: 408 clk - 1 frame: 262 line - DOTCLK = 6.5MHz	tshut-on (Note2)	-	-	11	frame

Table 10. 3 Power Up Sequence

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.

Note2: Display starts at 11th falling edge of VSTNC after the falling edge of SHUT. The display starts at the falling edge of VSYNC which is determined by BLT[1:0] of R04h.

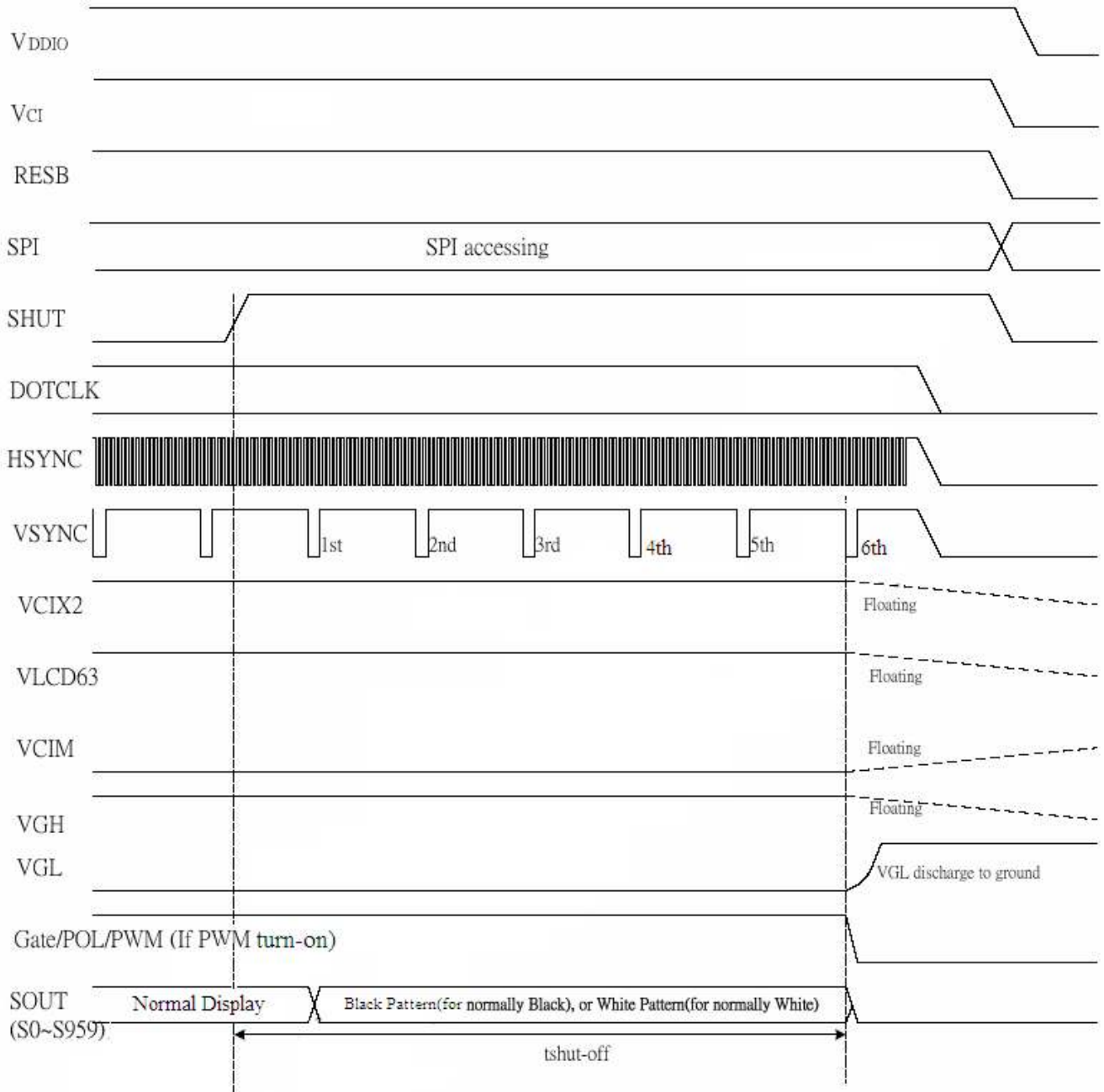


Figure 10. 14 Power Down Sequence

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Rising edge of SHUT to display off - 1 line: 408 clk - 1 frame: 262 line - DOTCLK = 6.5MHz	tshut-off	-	-	6	frame

Note: DOTCLK must be maintained at lease 6 frames after the rising edge of SHUT.
 Display become off at the 6nd falling edge of VSTNC after the falling edge of SHUT.
 If RESET signal is necessary for power down, provide it after the 6-frames-cycle of the SHUT period.

Table 10. 4 Power Down Sequence

11. Serial Interface

The SPI is available through the chip select line (CSB), serial transfer clock line (SCK), serial data input (SDI), and serial data output (SDO).

The Driver IC recognizes the start of data transfer at the falling edge of CSB input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of CSB input. The Driver IC is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the Driver IC are compared and both 6-bit data correspond. The identification code must be 011100. Two different chip addresses must be assigned to the Driver IC because the seventh bit of the start byte is assigned to a register select bit (R/S). When R/S = 0, index register write or status read is executed. When the R/S = 1, instruction write. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

After receiving the start byte, the Driver IC starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted (9th SCK started). All Driver IC instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (15th to 0th ~24th SCK).

R/S	R/W	Status
0	0	Write SPI address
0	1	Read gate line number (Note)
1	0	Write SPI data
1	1	Read SPI data

Table 11.1 R/S & R/W setting

Note: this function could let user know which gate line was turned on at that time.

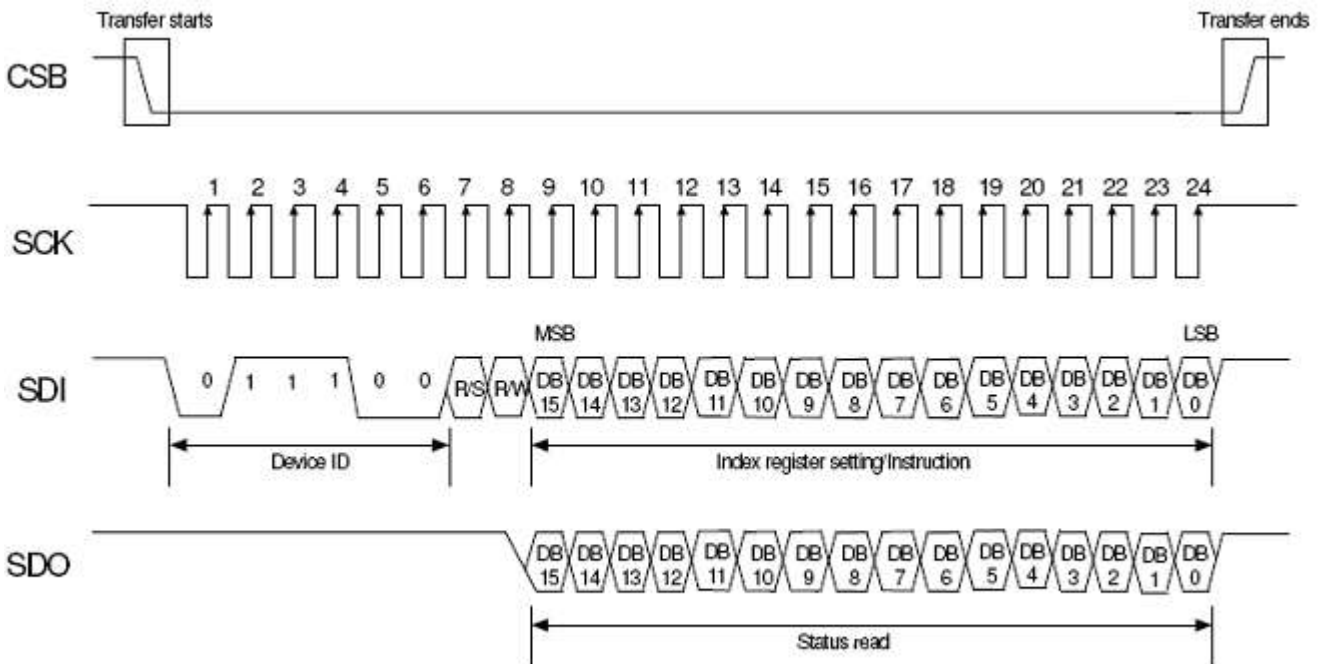


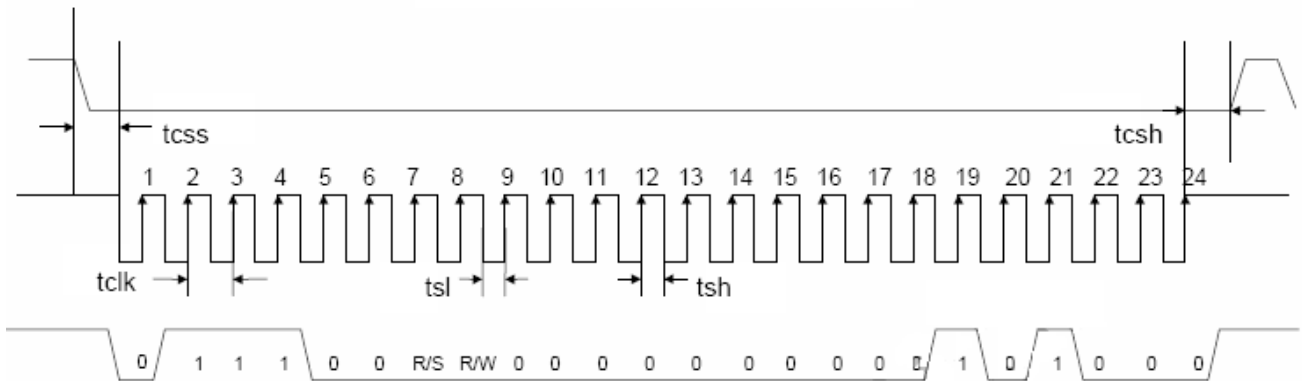
Figure 11.1 SPI Timing

PD035QX2 supports 24-bit serial bus interface. 24-bit data are latched by SCK's rising edge step-by-step. Serial bus interface is active while CSB=L (from CSB's falling to CSB's rising). After CSB has transmitted twenty-four units of CLK, it has to change into High.

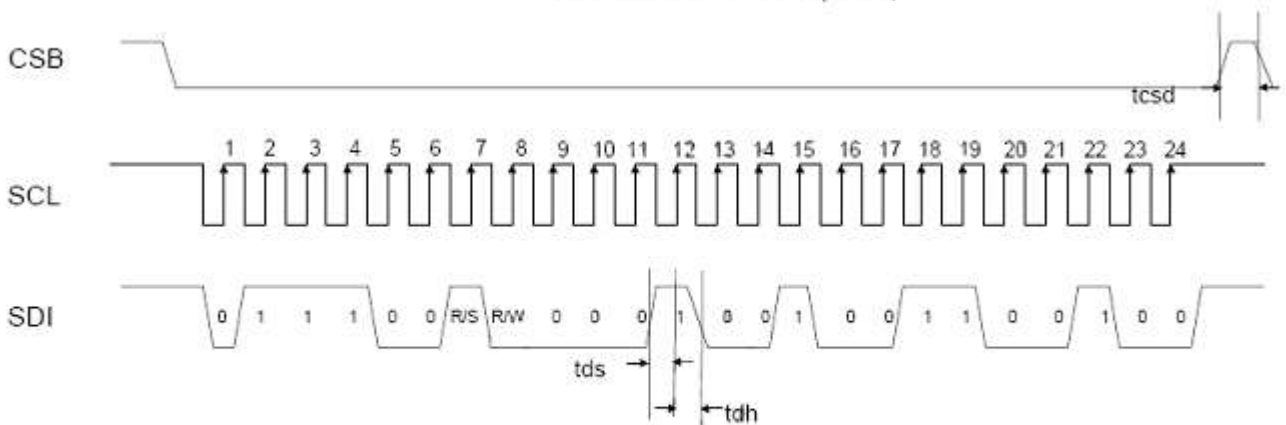
Under the standard condition, the number of CLK is twenty-four units. While CSB=L, if SCK < 24 cycles is input, then the input data won't be latched and will become invalid data. While CSB=L, if SCK > 24 cycles is input, the 24-bit data in front of CSB's rising edge will become valid.

Serial data is still active even at sleep mode. The SCK can be High or Low when CSB=High.

First Transmission (Register)

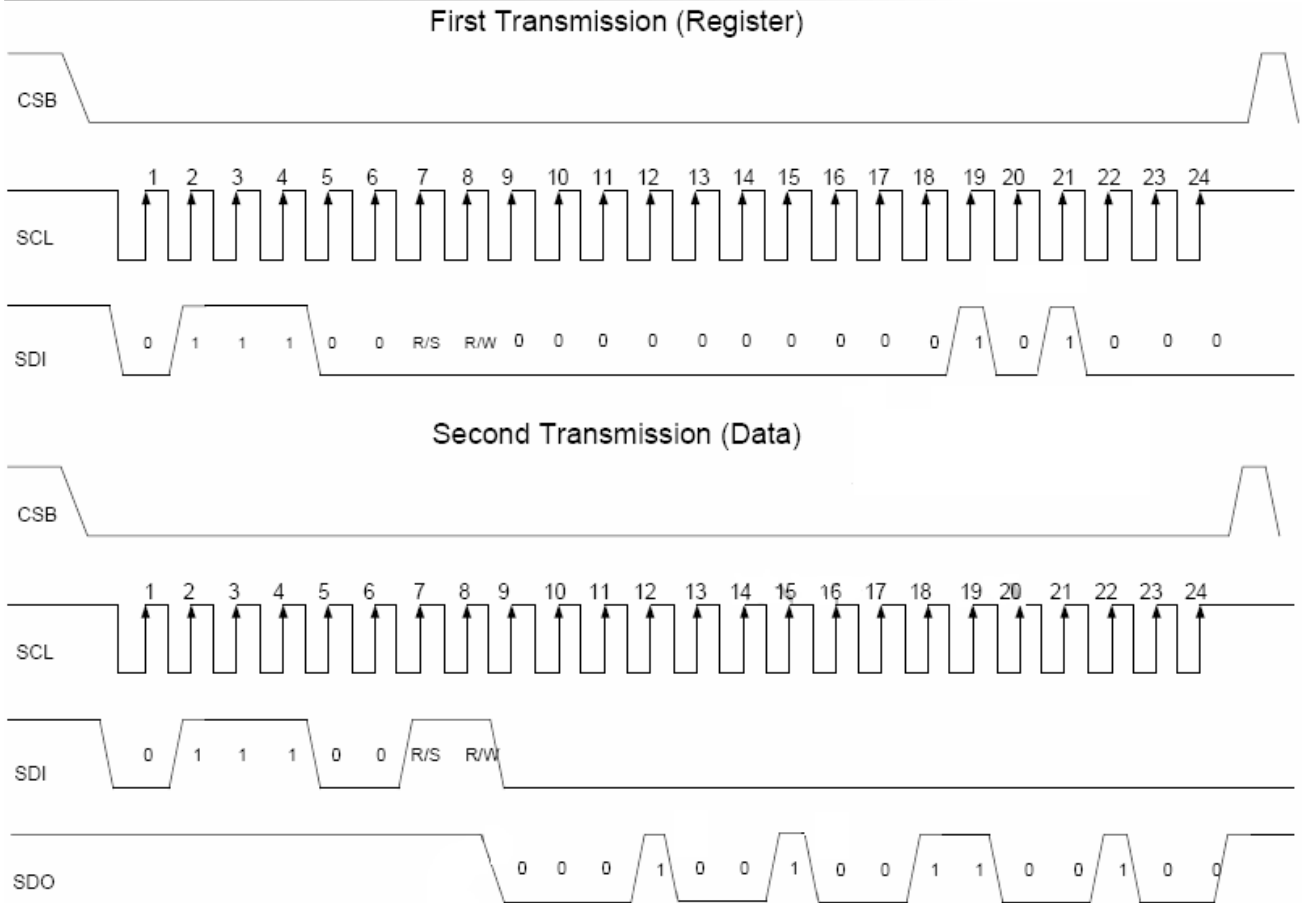


Second Transmission (Data)



Note: The example writes "0x1264h" to register R28h.
SPID connected to VSS.

Figure 11.2 SPI interface Timing Diagram & Write SPI Example



Note: The example Read "0x1264h" from register R28h.

Figure 11.3 Rising/Falling time

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Clock Rising Time	trs	-	-	30	ns
Clock Falling Time	tfl	-	-	30	ns
Chip Select Setup Time	tcss	0	-	-	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

Table 11.2 SPI Timing

Reference initial code :

Vgh, Vgl: 700003h, 726064h (Vgh = 15.3V, Vgl = -11.7V)

Vcomac : 70000Eh, 7236C0h (6Vpp)

Vcomdc : 70001Eh, 7200F7h (1.6V)

Data Control

The display data and frame position information from the controller is synchronized with the Gate Drive circuit and shift registered for the Source Driver circuit.

Gamma/Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma-adjusting resistor. 262K possible colors can be displayed.

Boost and Regulator Circuit

These two functional blocks generate the voltage of VGH, VGL, VCOMH, VCOML and VLCD63, which are necessary for operating a TFT LCD.

Shift Register

The shift registers control the direction of line scanning of source.

Data Latches

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the Source Driver to output the required voltage level.

Aging Mode

If only DOTCLK is sent into driver IC without VSYNC, HSYNC, and DEN signals, HX8238-A will enter Aging Mode after power on. In Aging Mode, the display will show Black, White, Red, Green, and Blue images in series automatically.

Reset Circuit

This block is integrated into the Interface Logic, which includes Power On Reset circuitry and the hardware reset pin, /RES. Both of these having the same reset function. Once the /RES pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10us. The status of the chip after reset is given by:

Reg#	Hex Code	Register Bit Value
R01h	6300	RL = '1', SM = "0", TB = '1'
R02h	0200	B/C = "1"
R03h	6364	DCT = "0110", BT = "011", BTF = "0", DC = "0110", AP = "010"
R04h	04XX	PALM = "1", BLT = "00", OEA = Note(2), SEL = "000"
R05h		GHN="1", XDK="0", GDIS="1", LPF="1", DEP="0", CKP="1", VSP= Note(2), HSP="0", DEO="1", DIT="1"
R0Ah	4008	BR = "1000000" CON = "01000"
R0Bh	D400	NO = "11" SDT = "01" EQ = "100"
R0Dh	3229	VRC = "011" VDS = "10" VRH = "101001"
R0Eh	3200	VDV = "1001000"
R0Fh	0000	SCN = "00000000"
R16h	9F80	XLIM = "100111111"
R17h		STH = "00" HBP = Note(2) VBP = Note(2)
R1Eh	0052	nOTP = "0" VCM = "1010010"
R30h	0000	PKP1 = "000" PKP0 = "000"
R31h	0407	PKP3 = "100" PKP2 = "111"
R32h	0202	PKP5 = "010" PKP4 = "010"
R33h	0000	PRP1 = "000" PRP0 = "000"
R34h	0505	PKN1 = "101" PKN0 = "101"
R35h	0003	PKN3 = "000" PKN2 = "011"
R36h	0707	PKN5 = "111" PKN4 = "111"
R37h	0000	PRN1 = "000" PRN0 = "000"
R3Ah	0904	VRP1 = "01001" VRP0 = "0100"
R3Bh	0904	VRN1 = "01001" VRN0 = "0100"

Note: (1) X means the bit is refer to the logic stage of the corresponding hardware pin.

(2) The default values of the VSP

Default Value auto setting			VSP	OEA[1:0]	HBP[6:0]	VBP[6:0]
SEL[2:0] = 000	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
PALM=1		0010010				
SEL[2:0] = 001	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
PALM=1		0010010				
SEL[2:0] = 010	NTSC		0	01	1000101	0010110
	PAL	PALM=0	0	10	1000101	0011100
PALM=1		0011000				
SEL[2:0] = 011	NTSC		0	01	1000100	0010110
	PAL	PALM=0	0	10	1000111	0011100
PALM=1		0011000				
SEL[2:0] = 100	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
PALM=1		0010100				
SEL[2:0] = 101	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
PALM=1		0010100				
SEL[2:0] = 110	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
PALM=1		0010100				
SEL[2:0] = 111	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
PALM=1		0010100				

Table 11. 3 Registers Default Value

12. Command Table

Reg#	Register	R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	
R01h	Driver output control	0	1	0	RL	1	0	0	SM	TB	1	0	0	0	0	0	0	0	0	
R02h	LCD driver AC control	0	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0	
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0	
R04h	Data and color filter control	0	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	1	1	1	
R05h	Function control	0	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	0	0	1	0	0	
R0Ah	Function control	0	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0	
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0	
R0Dh	Power control (2)	0	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	
R0Eh	Power control (3)	0	1	0	0	1	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	
R0Fh	Gate scan starting Position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	
R16h	Horizontal Porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0	
R17h	Vertical Porch	0	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	
R1Eh	Power control (4)	0	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	
R30h	y control (1)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00	
R31h	y control (2)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20	
R32h	y control (3)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40	
R33h	y control (4)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00	
R34h	y control (5)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00	
R35h	y control (6)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20	
R36h	y control (7)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40	
R37h	y control (8)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00	
R3Ah	y control (9)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	y control (10)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Note: means don't care Software settings will override hardware pin (eg, BGR bits override BGR pin definition)

13. Command Description

Status Read

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The status read instruction reads the internal status of the HX8238-A.

L7-0: Indicate the driving raster-row position where the liquid crystal display is being driven.

Driver Output Control (R01h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	RL	1	0	0	SM	TB	1	0	0	0	0	0	0	0	0

SM: Change the division of gate driver. When SM = "0", odd/even division (interlace mode) is selected. When SM = "1", upper/lower division is selected. Select the division mode according to the mounting method.

TB: Selects the output shift direction of the gate driver. When TB = "1", G0 shifts to G239. When TB = "0", G239 shifts to G0.

RL: Selects the output shift direction of the source driver. When RL = "1", S0 shifts to S959 and <R><G> color is assigned from S0. When RL = "0", S959 shifts to S0 and <R><G> color is assigned from S959. Set RL bit and BGR bit when changing the dot order of R, G and B.

Note: The default setting of register bits TB and RL are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.

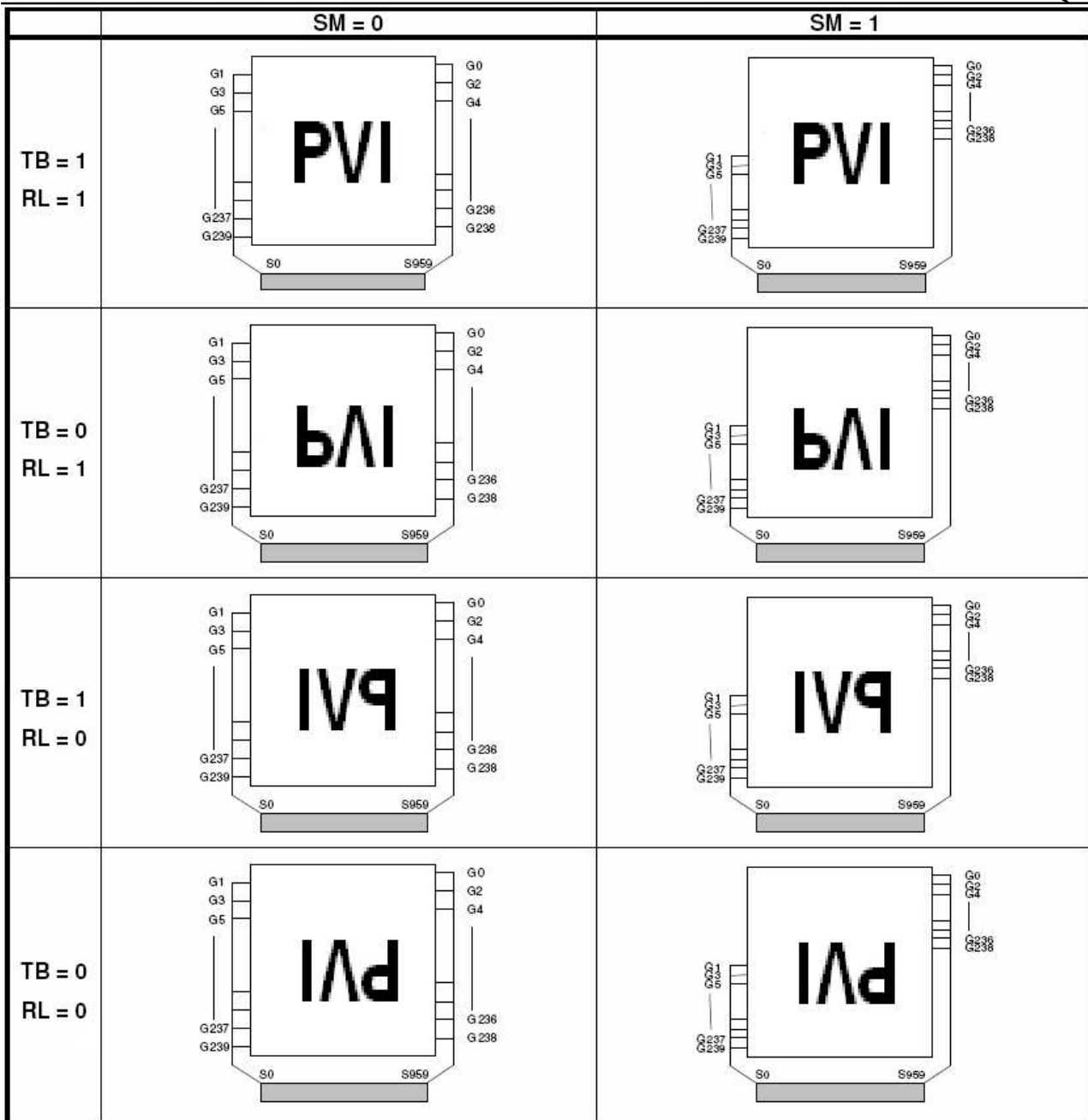


Figure 13.1 Scan Direction & Display

LCD-Driving-Waveform Control (R02h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0

B/C: When B/C = 0, frame inversion of the LCD driving signal is enabled. When B/C =1, line inversion waveform is generated

Power control 1 (R03h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0

DCT3-0: Set the step-up cycle of the step-up circuit for 8-color mode (CM = VDDIO). When the cycle is accelerated, the Vcim and Vcix2 driving ability of the step-up circuit increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption. VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table 13.2 Step-up Cycle

* Fline = horizontal frequency (Fline Typ. 15KHz)

BT2-0 & BTF: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power supply voltage to be used.

BT F	BT 2	BT 1	BT 0	VGH output	VGL output
0	0	0	0	VCIX2j X 3	-(VCIX2j X 3) + VCI
0	0	0	1	VCIX2j X 3	-(VCIX2j X 2)
0	0	1	0	VCIX2j X 3	-(VCIX2j X 3)
0	0	1	1	VCIX2j X 2 + VCI	-(VCIX2j X 2) - VCI
0	1	0	0	VCIX2j X 2 + VCI	-(VCIX2j X 2)
0	1	0	1	VCIX2j X 2 + VCI	-(VCIX2j X 2) + VCI
0	1	1	0	VCIX2j X 2	-(VCIX2j X 2)
0	1	1	1	VCIX2j X 2	-(VCIX2j X 2) + VCI
1	X	X	X	VCIX2j X 3	- VCIX2j

Table 13.3 VGH and VGL Booster Ratio

DC3-0: Set the step-up cycle of the step-up circuit for 262k-color mode (CM = VSS). When the cycle is accelerated, the Vcim and Vcix2 driving ability of the step-up circuit increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption. VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table13.4 Step-up Cycle

Note: Fline = horizontal frequency (Fline Typ. 15KHz)

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode, set AP2-0 = “000” to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

BTF	AP2	AP1	AP0	Op-amp power
0	0	0	0	Least
0	0	0	1	Small
0	0	1	0	Small to medium
0	0	1	1	Medium
0	1	0	0	Medium to large
0	1	0	1	Large
0	1	1	0	Large to Maximum
0	1	1	1	Maximum

Input Data and Color Filter Control (R04h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	0	0	0	0	PALM	BLT	BLT	OEA1	OEA0	SEL2	SEL1	SEL0	1	1	1

SEL2-0: Define the input interface mode.

BTF	SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	0	Parallel-RGB data format (only support stripe type color filter)	6.5MHz
0	0	0	1	Serial-RGB data format	19.5MHz
0	0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	0	1	1	CCIR 656 data format (720RGB)	27MHz
0	1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
0	1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
0	1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
0	1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Table 13.6 Interface Type

OEA1-0: Odd/Even field advanced function.

OEA1	OEA0	
0	0	Display Start @ VBP delay for Odd field and @ VBP-1 for Even field.
0	1	Display Start @ VBP delay for Odd field and @ VBP for Even field.
1	0	Display Start @ VBP delay for Odd field and @ VBP+1 for Even field.
1	1	No use

Table 13.7 Odd/Even Field Advanced Function

BLT [1:0]: Set the initial power on black image insertion time.

00: 10 fields

01: 20 fields

10: 40 fields

11: 80 fields

PALM: Set the input data line number in PAL mode

0: 280 lines

1: 288 lines

Function Control (R05h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIP	0	0	0	1	0	0

DIT: When DIT=0, dithering function is turned off. When DIT=1, dithering function is enabled.

DEO: When DEO=0, VSYNC/HSYNC are also needed in DE mode. Under this condition, vertical back porch is defined by VBP [6:0] and the horizontal first valid data is defined by DE signal. When DEO=1, only DEN signal is needed in DE mode.

HSP: When HSP=0, HSYNC is negative polarity. When HSP=1, HSYNC is positive polarity.

VSP: When VSP=0, VSYNC is negative polarity. When VSP=1, VSYNC is positive polarity.

CKP: When CKP=0, data is latched in CLK falling edge. When CKP=1, data is latched by CLK rising edge.

DEP: When DEP=0, DEN is negative polarity active. When DEP=1, DEN is positive polarity active.

LPF: When LPF=0, the low pass filter function in YUV mode is disabled. When LPF=1, the low pass filter function in YUV mode is enabled.

GDIS: When GDIS=0, VGL has no discharge path to VSS in sleep mode. When GDIS=1, VGL will discharge to VSS in sleep mode. When CPE=0, GDIS is fixed to 0, and you can't change it by SPI.

XDK: When XDK=0, VCIX2 is 2 stage pumping from VCI. (VCIX2=3 x VCI) When XDK=1, VCIX2 is 2 phase pumping from VCI. (VCIX2=2 x VCI)

GHN: When GHN=0, all gate outputs are forced to VGH. When GHN=1, gate driver is normal operation.

Contrast/Brightness Control (R0Ah)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0

CON4-0: Display Contrast level adjustment. (0.125/step) Adjust range from 00h (level =0) to 1Fh (level = 3.875). Default value is 08h (level = 1).

BR6-0: Display Brightness level adjustment. (2/step) Adjust range from 00h (level = -128) to 7Fh (level = +126). Default value is 40h (level = 0).

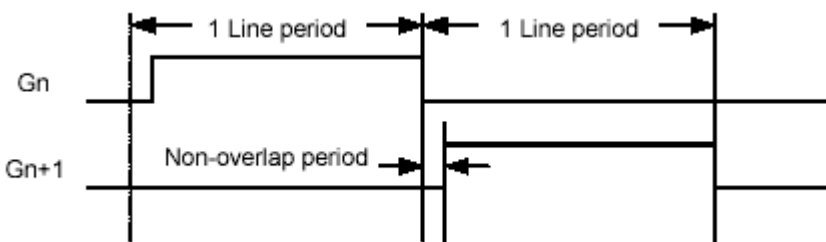
Frame Cycle Control (R0Bh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0

NO1-0: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	1.5 us
0	1	3 us
1	0	4.5 us
1	1	6 us

Table 13.8 Amount of Non-overlap



SDT1-0: Set delay amount from the gate output signal falling edge to the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	1μs
0	1	3μs
1	0	5μs
1	1	7μs

Table13.9 Delay Amount of Source Output

EQ2-0: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	3 μ s
0	1	0	4 μ s
0	1	1	5 μ s
1	0	0	6 μ s
1	0	1	7 μ s
1	1	0	8 μ s
1	1	1	9 μ s

Table 13.10 EQ Period

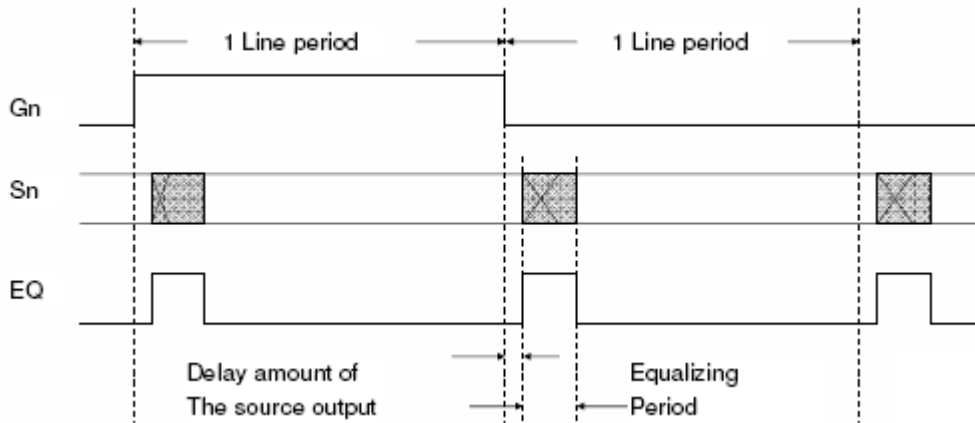


Figure 13.2 EQ Timing Diagram

Power Control 2 (R0Dh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

VRC [2:0]: set the VCIX2 charge pump voltage clamp.

VRC [2:0]=000, 5.1V

VRC [2:0]=001, 5.3V

VRC [2:0]=010, 5.5V

VRC [2:0]=011, 5.7V

VRC [2:0]=100, 5.9V

VRC [2:0]=101, reserved

VRC [2:0]=110, reserved

VRC [2:0]=111, reserved

VDS [1:0]: set the VDD regulator voltage if pin “REGVDD” is set to VDDIO.

VDS [1:0]=00, 1.8V

VDS [1:0]=01, 2.0V

VDS [1:0]=10, 2.2V

VDS [1:0]=11, 2.5V

VRH5-0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 2.456 to 4.472 times the Vref voltage set by VRH5-0.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63 Voltage	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63 Voltage
0	0	0	0	0	0	Vref x 2.456	1	0	0	0	0	0	Vref x 3.480
0	0	0	0	0	1	Vref x 2.488	1	0	0	0	0	1	Vref x 3.512
0	0	0	0	1	0	Vref x 2.520	1	0	0	0	1	0	Vref x 3.544
0	0	0	0	1	1	Vref x 2.552	1	0	0	0	1	1	Vref x 3.576
0	0	0	1	0	0	Vref x 2.584	1	0	0	1	0	0	Vref x 3.608
0	0	0	1	0	1	Vref x 2.616	1	0	0	1	0	1	Vref x 3.640
0	0	0	1	1	0	Vref x 2.648	1	0	0	1	1	0	Vref x 3.672
0	0	0	1	1	1	Vref x 2.680	1	0	0	1	1	1	Vref x 3.704
0	0	1	0	0	0	Vref x 2.712	1	0	1	0	0	0	Vref x 3.736
0	0	1	0	0	1	Vref x 2.744	1	0	1	0	0	1	Vref x 3.768
0	0	1	0	1	0	Vref x 2.776	1	0	1	0	1	0	Vref x 3.800
0	0	1	0	1	1	Vref x 2.808	1	0	1	0	1	1	Vref x 3.832
0	0	1	1	0	0	Vref x 2.840	1	0	1	1	0	0	Vref x 3.864
0	0	1	1	0	1	Vref x 2.872	1	0	1	1	0	1	Vref x 3.896
0	0	1	1	1	0	Vref x 2.904	1	0	1	1	1	0	Vref x 3.928
0	0	1	1	1	1	Vref x 2.936	1	0	1	1	1	1	Vref x 3.960
0	1	0	0	0	0	Vref x 2.968	1	1	0	0	0	0	Vref x 3.992
0	1	0	0	0	1	Vref x 3.000	1	1	0	0	0	1	Vref x 4.024
0	1	0	0	1	0	Vref x 3.032	1	1	0	0	1	0	Vref x 4.056
0	1	0	0	1	1	Vref x 3.064	1	1	0	0	1	1	Vref x 4.088
0	1	0	1	0	0	Vref x 3.096	1	1	0	1	0	0	Vref x 4.120
0	1	0	1	0	1	Vref x 3.128	1	1	0	1	0	1	Vref x 4.152
0	1	0	1	1	0	Vref x 3.160	1	1	0	1	1	0	Vref x 4.184
0	1	0	1	1	1	Vref x 3.192	1	1	0	1	1	1	Vref x 4.216
0	1	1	0	0	0	Vref x 3.224	1	1	1	0	0	0	Vref x 4.248
0	1	1	0	0	1	Vref x 3.256	1	1	1	0	0	1	Vref x 4.280
0	1	1	0	1	0	Vref x 3.288	1	1	1	0	1	0	Vref x 4.312
0	1	1	0	1	1	Vref x 3.320	1	1	1	0	1	1	Vref x 4.344
0	1	1	1	0	0	Vref x 3.352	1	1	1	1	0	0	Vref x 4.376
0	1	1	1	0	1	Vref x 3.384	1	1	1	1	0	1	Vref x 4.408
0	1	1	1	1	0	Vref x 3.416	1	1	1	1	1	0	Vref x 4.440
0	1	1	1	1	1	Vref x 3.448	1	1	1	1	1	1	Vref x 4.472

Table 13.11 VLCD63 Voltage

Note: Vref is the internal reference voltage equals to 1.25V.

Power Control 3 (R0Eh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	0	1	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0

VDV6-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM amplitude 0.6 to 1.2525 times the VLCD63 voltage. External voltage at VCOMR is referenced when VDV = “01111xx”.

VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	0	0	VLCD63 x 0.6000
0	0	0	0	0	0	1	VLCD63 x 0.6075
0	0	0	0	0	1	0	VLCD63 x 0.6150
⋮							Step = 0.0075
0	0	1	1	0	1	0	VLCD63 x 1.0350
0	0	1	1	0	1	1	VLCD63 x 1.0425
0	1	1	1	1	*	*	Reference from external voltage (VCOMR)
1	0	0	0	0	0	0	VLCD63 x 1.0500
1	0	0	0	0	0	1	VLCD63 x 1.0575
⋮							Step = 0.0075
1	0	1	1	0	1	0	VLCD63 x 1.2450
0	0	0	1	1	1	0	VLCD63 x 1.2525

Table 13.12 VCOM Amplitude

Gate Scan Position (R0Fh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN8-0: Set the scanning starting position of the gate driver.

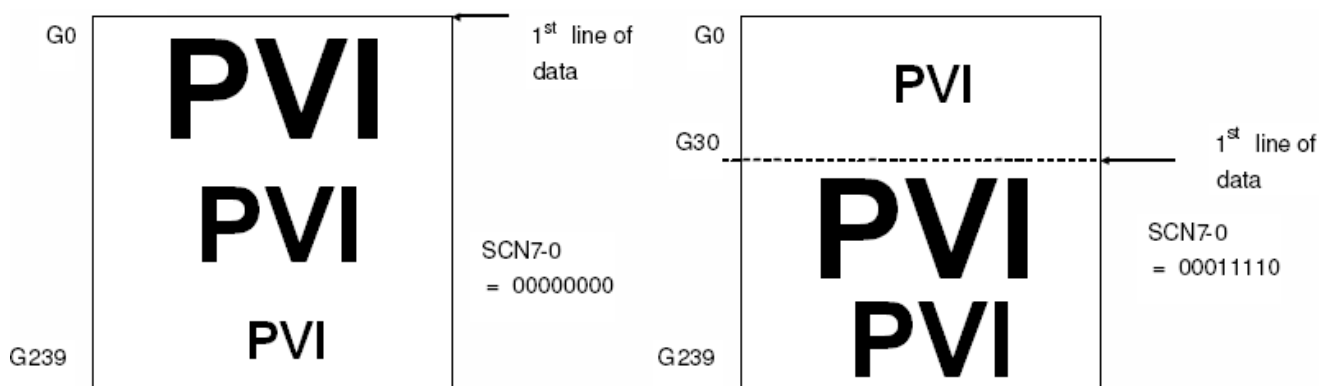


Figure 8. 15 Gate scan display position

Horizontal Porch (R16h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0

XLIM8-0: Set the number of valid pixel per line.

XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	1	0	3
⋮									⋮
⋮									STEP=1
⋮									⋮
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320

Table 13.13 No. of Pixel Per Line

Vertical Porch (R17h)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

HBP6-0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XLIM8-0 and before the first valid data will be treated as dummy data. The setting is only effective in SYNC mode timing.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of Clock Cycle		
							Parallel	Serial	YUV
0	0	0	0	0	0	0	Can't set		
⋮									
0	0	0	1	0	0	0			
0	1	1	1	0	0	1	9	27	36
0	1	1	1	0	1	0	10	30	40
⋮							⋮	⋮	⋮
⋮							step=1	step=3	step=4
⋮							⋮	⋮	⋮
1	1	1	1	1	1	0	126	378	504
1	1	1	1	1	1	1	127	381	508

Table 13.14 No. of Clock Cycle of Clock

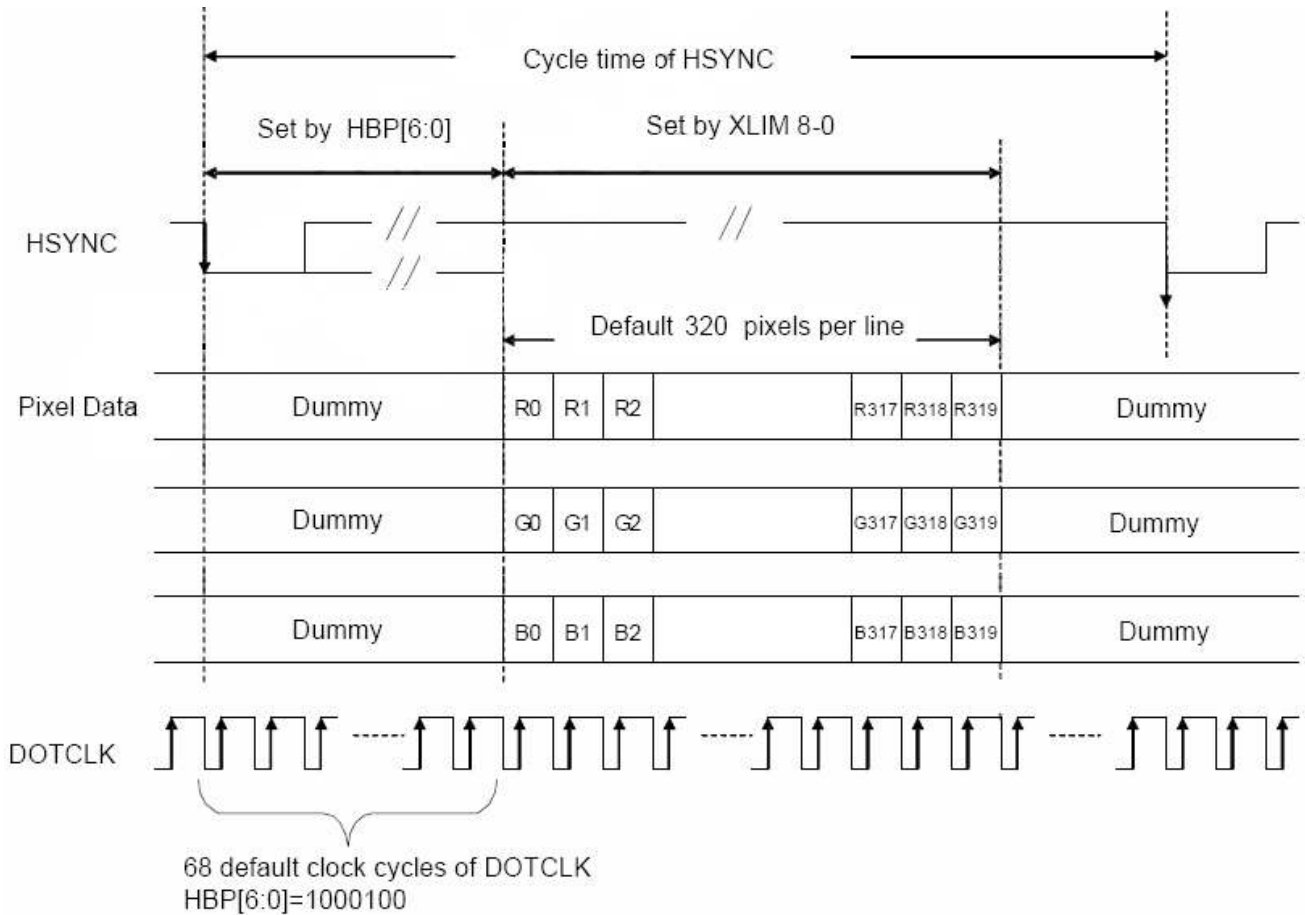


Figure13.3 No. of Clock Cycle of Clock (Parallel RGB)

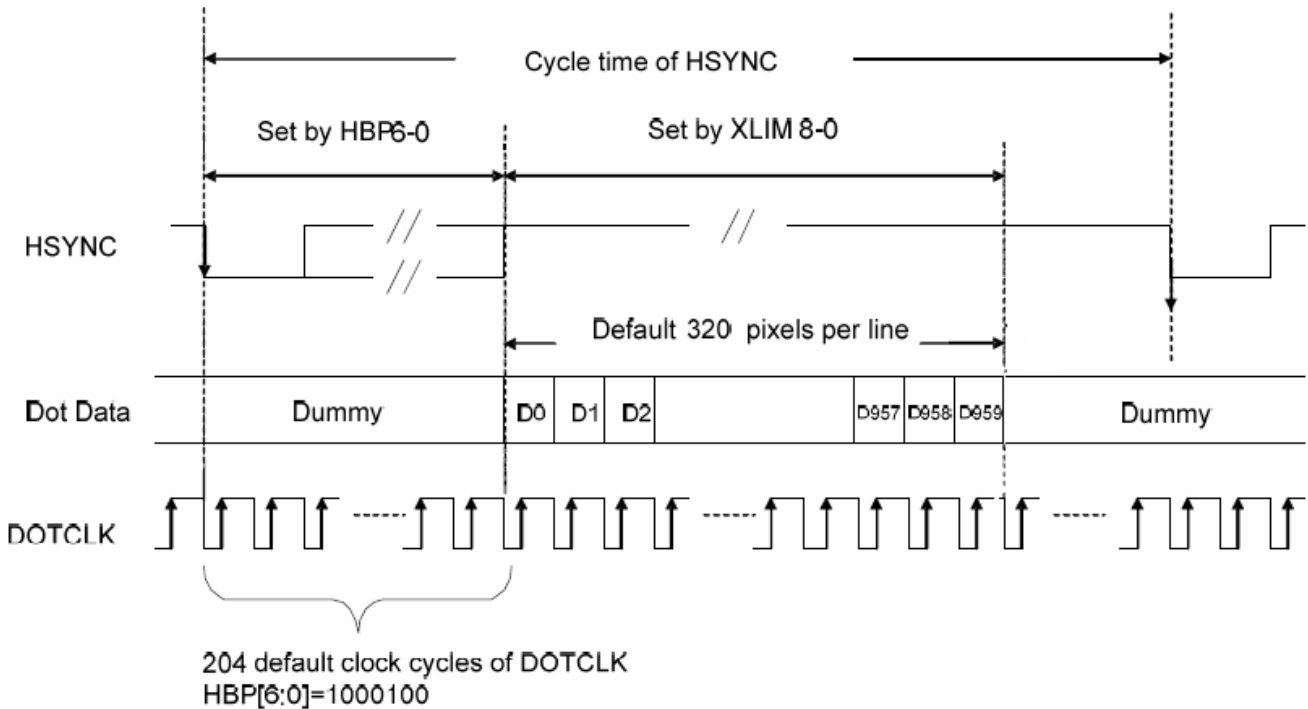


Figure 13.4 No. of Clock Cycle of Clock (Serial RGB)

STH1-0: Adjust the first valid data by dot clock. This setting is not valid in parallel RGB input interface.

- STH = 00: +0 dot clock
- STH = 01: +1 dot clock
- STH = 10: +2 dot clock
- STH = 11: +3 dot clock

VBP6-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line. The setting is only effective in SYNC mode timing.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
							:
							step=1
							:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 13.15 No. of Clock Cycle of HSYNC

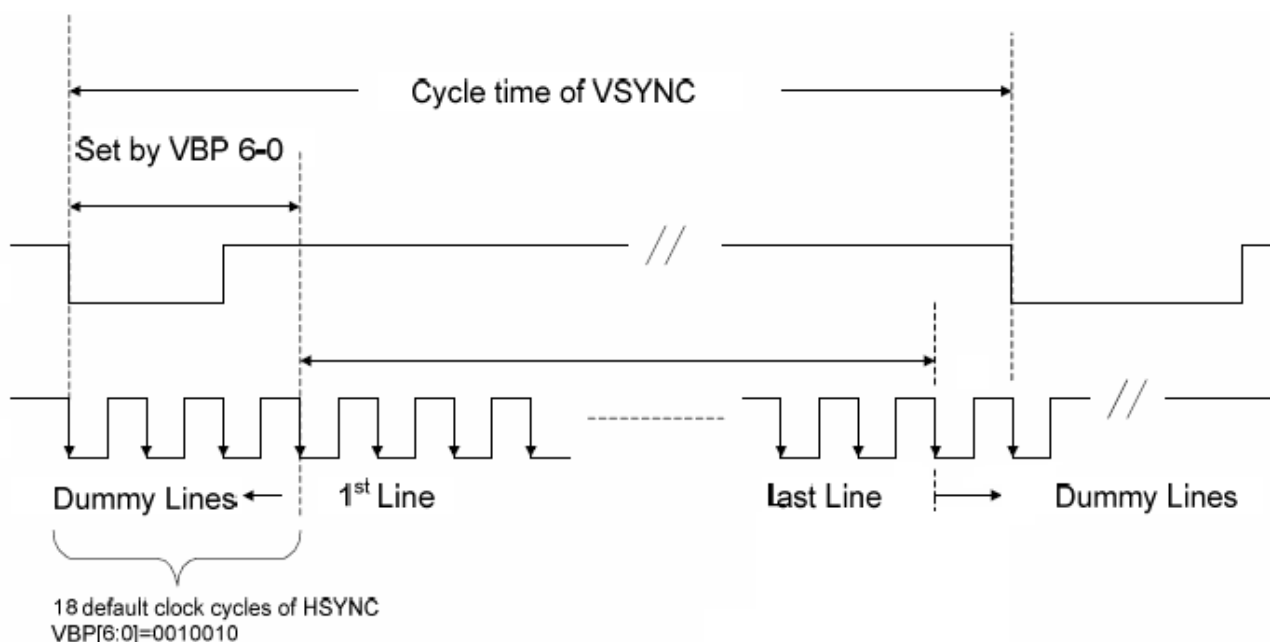


Figure13.5 No. of Clock Cycle of HSYNC (Parallel RGB)

Power Control 4 (R1Eh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

nOTP: nOTP equals to “0” after power on reset and VCOMH voltage equals to programmed OTP value. When nOTP set to “1”, setting of VCM6-0 becomes valid and voltage of VCOMH can be adjusted.
VCM6-0: Set the VCOMH voltage if nOTP = “1”. These bits amplify the VCOMH voltage 0.36 to 0.995 times the VLCD63 voltage.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VLCD63 x 0.360
0	0	0	0	0	0	1	VLCD63 x 0.365
0	0	0	0	0	1	0	VLCD63 x 0.370
0	0	0	0	0	1	1	VLCD63 x 0.375
0	0	0	0	1	0	0	VLCD63 x 0.380
							: step=0.005 :
1	1	1	1	1	1	0	VLCD63 x 0.990
1	1	1	1	1	1	1	VLCD63 x 0.995

Table13.16 VCOMH

Note: $2V < VCOMH < VLCD63$ **Gamma Control 1 (R30h to R37h)**

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00

PKP52-00: Gamma micro adjustment registers for the positive polarity output.**PRP12-00:** Gradient adjustment registers for the positive polarity output.**PKN52-00:** Gamma micro adjustment registers for the negative polarity output.**PRN12-00:** Gradient adjustment registers for the negative polarity output.

Gamma Control 2 (R3Ah to R3Bh)

R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

VRP14-00: Adjustment registers for amplification adjustment of the positive polarity output.

VRN14-00: Adjustment registers for the amplification adjustment of the negative polarity output.

(Refer to Gamma Adjustment Function for details)

14. Gamma Adjustment Function

The HX8238-A incorporates gamma adjustment function for the 262K-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel’s specification.

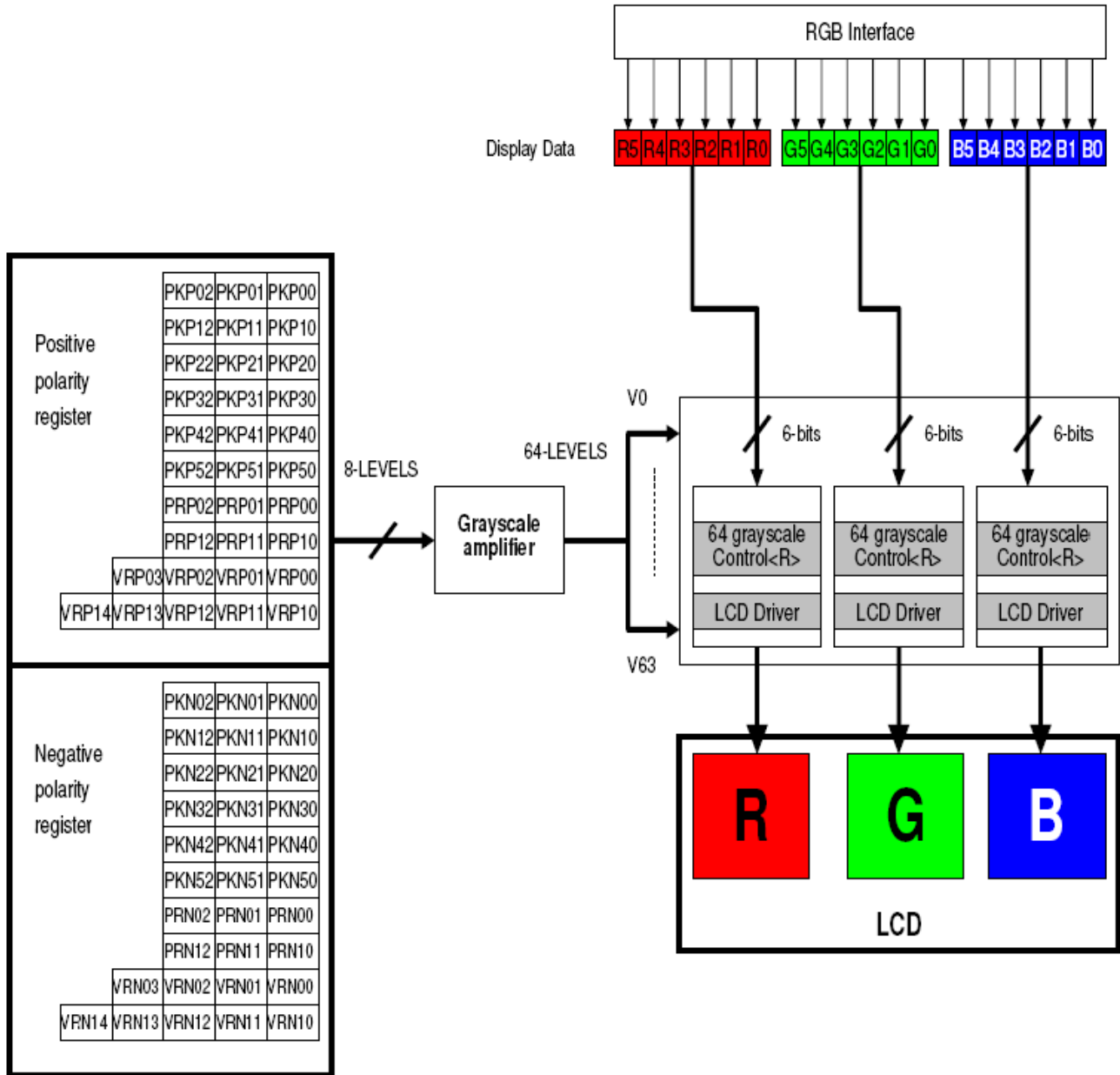


Figure 14. 1 Grayscale Control Block

14-1) Structure of Grayscale Amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.

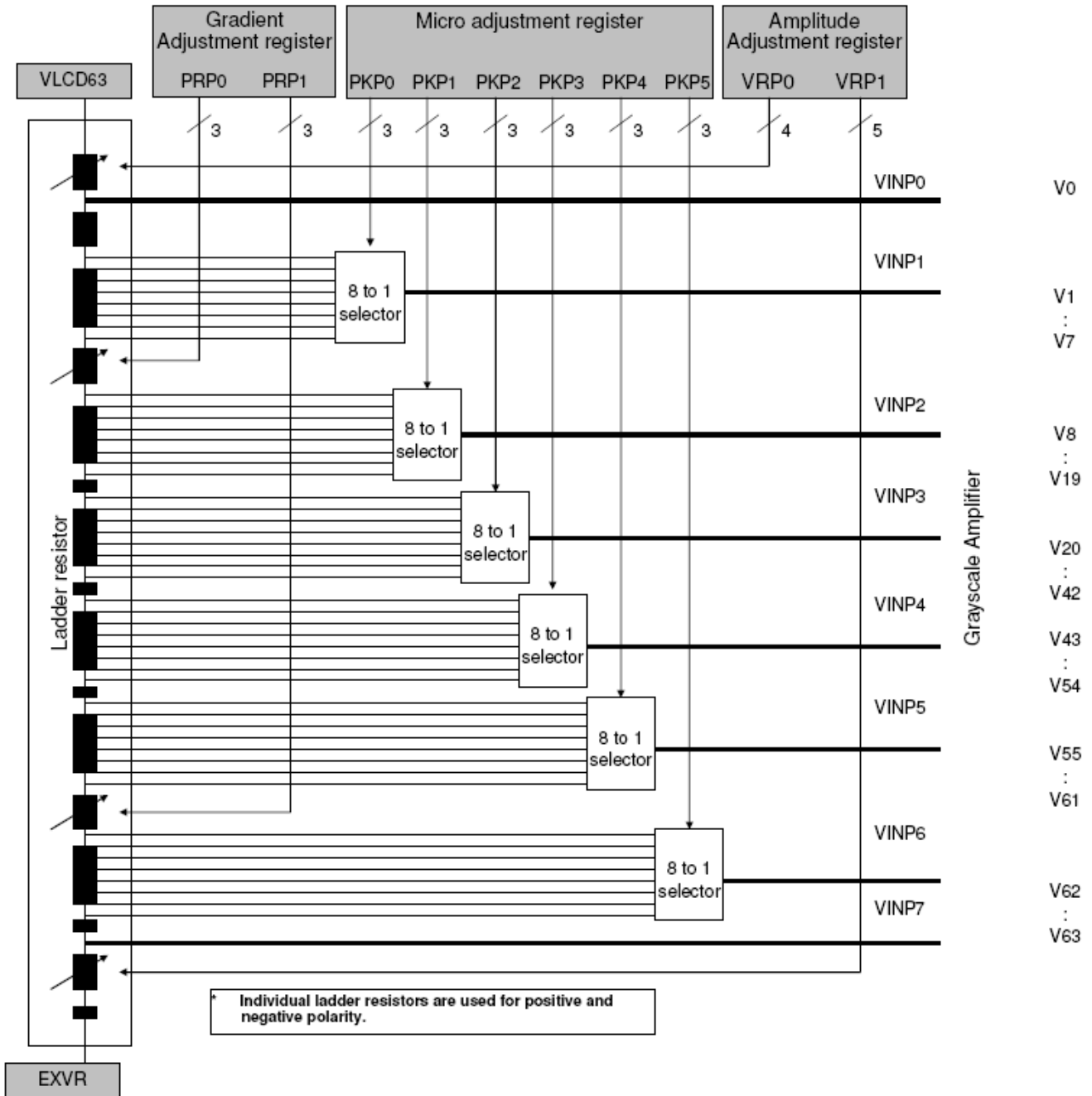


Figure 14. 2 Grayscale Amplifier

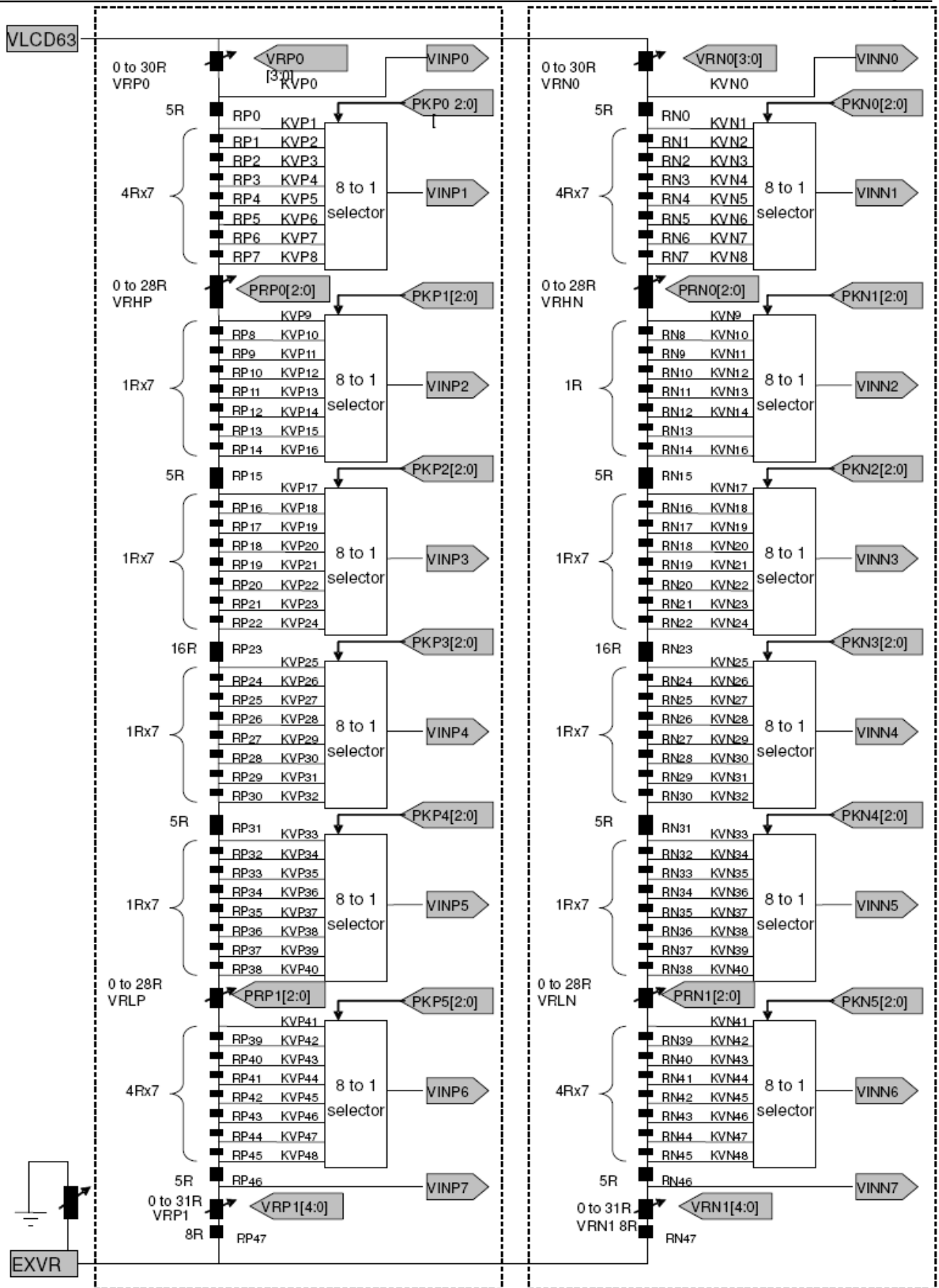


Figure 14.3 Resistor Ladder for Gamma Voltages Generation

14-2) Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD

panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.

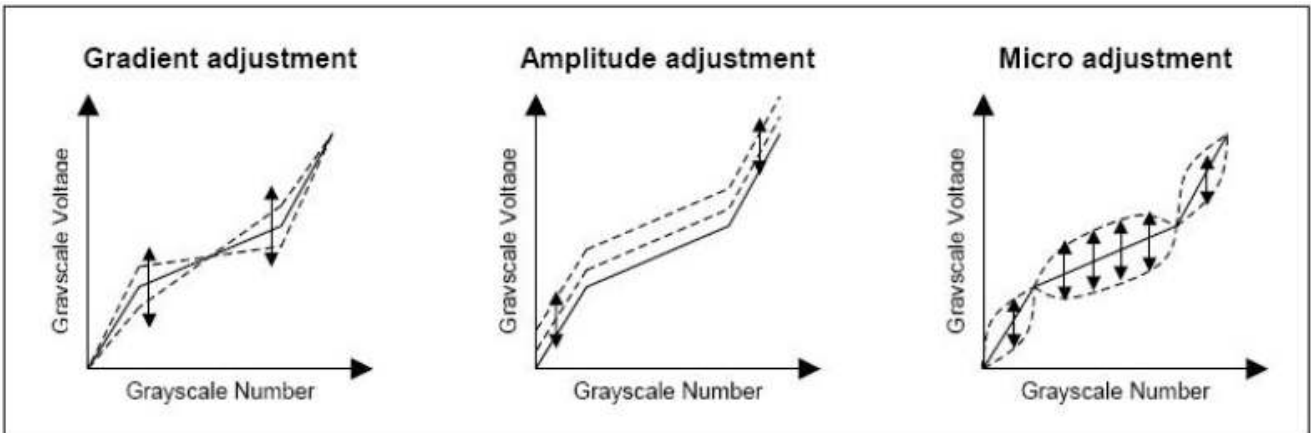


Figure 14. 4 Gamma Adjustment Function

14-2-1) Gradient Adjusting Register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP (N) 0 / PRP (N) 1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

14-2-2) Amplitude Adjusting Register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP (N) 0 / VRP (N) 1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

14-2-3) Micro Adjusting Register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

14-3) Ladder Resistor / 8 to 1 Selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors. Also, there has pin (EXVR) that can be connected to VSS or an external variable resistor for compensating the dispersion of length between one panel to another.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP (N) 0 / PRP (N) 1) and (VRP (N) 0 / VRP (N) 1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 14. 1 PRP (N)

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
:	:
Step = 2R	:
:	:
1110	28R
1111	30R

Table 14. 2 VRP (N) 0

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
:	:
Step = 1R	:
:	:
11110	30R
11111	31R

Table 14. 3 VRP (N) 1

8 to 1 Selector

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro adjusting register and the selecting voltage.

Register PKP[2:0]	Positive polarity						Register PKN[2:0]	Negative polarity					
	Selected voltage							Selected voltage					
	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6		VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Table 14. 4 PKP and PKN

Grayscale voltage	Positive Polarity	Negative Polarity
V0	VINP0	VINN7
V1	VINP1	VINN6
V2	$V8+(V1-V8)*(2241/2703)$	$V1+(V8-V1)*(462/2703)$
V3	$V8+(V1-V8)*(1671/2703)$	$V1+(V8-V1)*(1032/2703)$
V4	$V8+(V1-V8)*(1209/2703)$	$V1+(V8-V1)*(1494/2703)$
V5	$V8+(V1-V8)*(849/2703)$	$V1+(V8-V1)*(1854/2703)$
V6	$V8+(V1-V8)*(567/2703)$	$V1+(V8-V1)*(2136/2703)$
V7	$V8+(V1-V8)*(294/2703)$	$V1+(V8-V1)*(2409/2703)$
V8	VINP2	VINN5
V9	$V20+(V8-V20)*(1533/1767)$	$V8+(V20-V8)*(234/1767)$
V10	$V20+(V8-V20)*(1356/1767)$	$V8+(V20-V8)*(411/1767)$
V11	$V20+(V8-V20)*(1188/1767)$	$V8+(V20-V8)*(579/1767)$
V12	$V20+(V8-V20)*(993/1767)$	$V8+(V20-V8)*(774/1767)$
V13	$V20+(V8-V20)*(843/1767)$	$V8+(V20-V8)*(924/1767)$
V14	$V20+(V8-V20)*(693/1767)$	$V8+(V20-V8)*(1074/1767)$
V15	$V20+(V8-V20)*(543/1767)$	$V8+(V20-V8)*(1224/1767)$
V16	$V20+(V8-V20)*(441/1767)$	$V8+(V20-V8)*(1326/1767)$
V17	$V20+(V8-V20)*(336/1767)$	$V8+(V20-V8)*(1431/1767)$
V18	$V20+(V8-V20)*(213/1767)$	$V8+(V20-V8)*(1554/1767)$
V19	$V20+(V8-V20)*(81/1767)$	$V8+(V20-V8)*(1686/1767)$
V20	VINP3	VINN4
V21	$V43+(V20-V43)*(1887/1965)$	$V20+(V43-V20)*(78/1965)$
V22	$V43+(V20-V43)*(1779/1965)$	$V20+(V43-V20)*(186/1965)$
V23	$V43+(V20-V43)*(1653/1965)$	$V20+(V43-V20)*(312/1965)$
V24	$V43+(V20-V43)*(1536/1965)$	$V20+(V43-V20)*(429/1965)$
V25	$V43+(V20-V43)*(1437/1965)$	$V20+(V43-V20)*(528/1965)$
V26	$V43+(V20-V43)*(1362/1965)$	$V20+(V43-V20)*(603/1965)$
V27	$V43+(V20-V43)*(1278/1965)$	$V20+(V43-V20)*(687/1965)$
V28	$V43+(V20-V43)*(1191/1965)$	$V20+(V43-V20)*(774/1965)$
V29	$V43+(V20-V43)*(1098/1965)$	$V20+(V43-V20)*(867/1965)$
V30	$V43+(V20-V43)*(1008/1965)$	$V20+(V43-V20)*(957/1965)$
V31	$V43+(V20-V43)*(927/1965)$	$V20+(V43-V20)*(1038/1965)$
V32	$V43+(V20-V43)*(843/1965)$	$V20+(V43-V20)*(1122/1965)$
V33	$V43+(V20-V43)*(750/1965)$	$V20+(V43-V20)*(1215/1965)$
V34	$V43+(V20-V43)*(678/1965)$	$V20+(V43-V20)*(1287/1965)$
V35	$V43+(V20-V43)*(612/1965)$	$V20+(V43-V20)*(1353/1965)$
V36	$V43+(V20-V43)*(528/1965)$	$V20+(V43-V20)*(1437/1965)$
V37	$V43+(V20-V43)*(450/1965)$	$V20+(V43-V20)*(1515/1965)$
V38	$V43+(V20-V43)*(375/1965)$	$V20+(V43-V20)*(1590/1965)$
V39	$V43+(V20-V43)*(303/1965)$	$V20+(V43-V20)*(1662/1965)$
V40	$V43+(V20-V43)*(222/1965)$	$V20+(V43-V20)*(1743/1965)$
V41	$V43+(V20-V43)*(147/1965)$	$V20+(V43-V20)*(1818/1965)$
V42	$V43+(V20-V43)*(87/1965)$	$V20+(V43-V20)*(1878/1965)$
V43	VINP4	VINN3
V44	$V55+(V43-V55)*(936/1014)$	$V43+(V55-V43)*(78/1014)$
V45	$V55+(V43-V55)*(867/1014)$	$V43+(V55-V43)*(147/1014)$
V46	$V55+(V43-V55)*(792/1014)$	$V43+(V55-V43)*(222/1014)$
V47	$V55+(V43-V55)*(723/1014)$	$V43+(V55-V43)*(291/1014)$
V48	$V55+(V43-V55)*(648/1014)$	$V43+(V55-V43)*(366/1014)$
V49	$V55+(V43-V55)*(561/1014)$	$V43+(V55-V43)*(453/1014)$
V50	$V55+(V43-V55)*(465/1014)$	$V43+(V55-V43)*(549/1014)$

V51	$V55+(V43-V55)*(387/1014)$	$V43+(V55-V43)*(627/1014)$
V52	$V55+(V43-V55)*(291/1014)$	$V43+(V55-V43)*(723/1014)$
V53	$V55+(V43-V55)*(201/1014)$	$V43+(V55-V43)*(813/1014)$
V54	$V55+(V43-V55)*(111/1014)$	$V43+(V55-V43)*(903/1014)$
V55	VINP5	VINN2
V56	$V62+(V55-V62)*(1218/1317)$	$V55+(V62-V55)*(99/1317)$
V57	$V62+(V55-V62)*(1092/1317)$	$V55+(V62-V55)*(225/1317)$
V58	$V62+(V55-V62)*(936/1317)$	$V55+(V62-V55)*(381/1317)$
V59	$V62+(V55-V62)*(774/1317)$	$V55+(V62-V55)*(543/1317)$
V60	$V62+(V55-V62)*(579/1317)$	$V55+(V62-V55)*(738/1317)$
V61	$V62+(V55-V62)*(324/1317)$	$V55+(V62-V55)*(993/1317)$
V62	VINP6	VINN1
V63	VINP7	VINN0

Table 14.5 Grayscale Voltages Formulas

Reference	Formula	Micro-adjusting register	Reference voltage
KVP0	$VLCD63 - GV \times VRP0 / SUMRP$	-	VINP0
KVP1	$VLCD63 - GV \times (VRP0 + 5R) / SUMRP$	PKP0[2:0] = "000"	VINP1
KVP2	$VLCD63 - GV \times (VRP0 + 9R) / SUMRP$	PKP0[2:0] = "001"	
KVP3	$VLCD63 - GV \times (VRP0 + 13R) / SUMRP$	PKP0[2:0] = "010"	
KVP4	$VLCD63 - GV \times (VRP0 + 17R) / SUMRP$	PKP0[2:0] = "011"	
KVP5	$VLCD63 - GV \times (VRP0 + 21R) / SUMRP$	PKP0[2:0] = "100"	
KVP6	$KVP6 \text{ } VLCD63 - GV \times (VRP0 + 25R) / SUMRP$	PKP0[2:0] = "101"	
KVP7	$VLCD63 - GV \times (VRP0 + 29R) / SUMRP$	PKP0[2:0] = "110"	
KVP8	$VLCD63 - GV \times (VRP0 + 33R) / SUMRP$	PKP0[2:0] = "111"	
KVP9	$VLCD63 - GV \times (VRP0 + 33R + VRHP) / SUMRP$	PKP1[2:0] = "000"	VINP2
KVP10	$VLCD63 - GV \times (VRP0 + 34R + VRHP) / SUMRP$	PKP1[2:0] = "001"	
KVP11	$VLCD63 - GV \times (VRP0 + 35R + VRHP) / SUMRP$	PKP1[2:0] = "010"	
KVP12	$VLCD63 - GV \times (VRP0 + 36R + VRHP) / SUMRP$	PKP1[2:0] = "011"	
KVP13	$VLCD63 - GV \times (VRP0 + 37R + VRHP) / SUMRP$	PKP1[2:0] = "100"	
KVP14	$VLCD63 - GV \times (VRP0 + 38R + VRHP) / SUMRP$	PKP1[2:0] = "101"	
KVP15	$VLCD63 - GV \times (VRP0 + 39R + VRHP) / SUMRP$	PKP1[2:0] = "110"	
KVP16	$VLCD63 - GV \times (VRP0 + 40R + VRHP) / SUMRP$	PKP1[2:0] = "111"	
KVP17	$VLCD63 - GV \times (VRP0 + 45R + VRHP) / SUMRP$	PKP2[2:0] = "000"	VINP3
KVP18	$VLCD63 - GV \times (VRP0 + 46R + VRHP) / SUMRP$	PKP2[2:0] = "001"	
KVP19	$VLCD63 - GV \times (VRP0 + 47R + VRHP) / SUMRP$	PKP2[2:0] = "010"	
KVP20	$VLCD63 - GV \times (VRP0 + 48R + VRHP) / SUMRP$	PKP2[2:0] = "011"	
KVP21	$VLCD63 - GV \times (VRP0 + 49R + VRHP) / SUMRP$	PKP2[2:0] = "100"	
KVP22	$VLCD63 - GV \times (VRP0 + 50R + VRHP) / SUMRP$	PKP2[2:0] = "101"	
KVP23	$VLCD63 - GV \times (VRP0 + 51R + VRHP) / SUMRP$	PKP2[2:0] = "110"	
KVP24	$VLCD63 - GV \times (VRP0 + 52R + VRHP) / SUMRP$	PKP2[2:0] = "111"	
KVP25	$VLCD63 - GV \times (VRP0 + 68R + VRHP) / SUMRP$	PKP3[2:0] = "000"	VINP4
KVP26	$VLCD63 - GV \times (VRP0 + 69R + VRHP) / SUMRP$	PKP3[2:0] = "001"	
KVP27	$VLCD63 - GV \times (VRP0 + 70R + VRHP) / SUMRP$	PKP3[2:0] = "001"	
KVP28	$VLCD63 - GV \times (VRP0 + 71R + VRHP) / SUMRP$	PKP3[2:0] = "011"	
KVP29	$VLCD63 - GV \times (VRP0 + 72R + VRHP) / SUMRP$	PKP3[2:0] = "100"	
KVP30	$VLCD63 - GV \times (VRP0 + 73R + VRHP) / SUMRP$	PKP3[2:0] = "101"	
KVP31	$VLCD63 - GV \times (VRP0 + 74R + VRHP) / SUMRP$	PKP3[2:0] = "110"	
KVP32	$VLCD63 - GV \times (VRP0 + 75R + VRHP) / SUMRP$	PKP3[2:0] = "111"	
KVP33	$VLCD63 - GV \times (VRP0 + 80R + VRHP) / SUMRP$	PKP4[2:0] = "000"	VINP5
KVP34	$VLCD63 - GV \times (VRP0 + 81R + VRHP) / SUMRP$	PKP4[2:0] = "001"	
KVP35	$VLCD63 - GV \times (VRP0 + 82R + VRHP) / SUMRP$	PKP4[2:0] = "010"	
KVP36	$VLCD63 - GV \times (VRP0 + 83R + VRHP) / SUMRP$	PKP4[2:0] = "011"	
KVP37	$VLCD63 - GV \times (VRP0 + 84R + VRHP) / SUMRP$	PKP4[2:0] = "100"	
KVP38	$VLCD63 - GV \times (VRP0 + 85R + VRHP) / SUMRP$	PKP4[2:0] = "101"	
KVP39	$VLCD63 - GV \times (VRP0 + 86R + VRHP) / SUMRP$	PKP4[2:0] = "110"	
KVP40	$VLCD63 - GV \times (VRP0 + 87R + VRHP) / SUMRP$	PKP4[2:0] = "111"	
KVP41	$VLCD63 - GV \times (VRP0 + 87R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "000"	VINP6
KVP42	$VLCD63 - GV \times (VRP0 + 91R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "001"	
KVP43	$VLCD63 - GV \times (VRP0 + 95R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "010"	
KVP44	$VLCD63 - GV \times (VRP0 + 99R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "011"	
KVP45	$VLCD63 - GV \times (VRP0 + 103R + VRHP + VRLP) / SUMRP$	PKP5[2:0] = "100"	

KVP46	$\text{VLCD63} - \text{GV} \times (\text{VRP0} + 107\text{R} + \text{VRHP} + \text{VRLP}) / \text{SUMRP}$	PKP5[2:0] = "101"	
KVP47	$\text{VLCD63} - \text{GV} \times (\text{VRP0} + 111\text{R} + \text{VRHP} + \text{VRLP}) / \text{SUMRP}$	PKP5[2:0] = "110"	
KVP48	$\text{VLCD63} - \text{GV} \times (\text{VRP0} + 115\text{R} + \text{VRHP} + \text{VRLP}) / \text{SUMRP}$	PKP5[2:0] = "111"	
KVP49	$\text{VLCD63} - \text{GV} \times (\text{VRP0} + 120\text{R} + \text{VRHP} + \text{VRLP}) / \text{SUMRP}$	-	VINP7

Table 14. 6 Reference Voltages of Positive Polarity

SUMRP: Total of the positive polarity ladder resistance = $128\text{R} + \text{VRHP} + \text{VRLP} + \text{VRP0} + \text{VRP1}$

GV: Voltage difference between VLCD63 and of EXVR.

Reference	Formula	Micro-adjusting register	Reference voltage
KVN0	$VLCD63 - GV \times VRN0 / SUMRN$	-	VINN0
KVN1	$VLCD63 - GV \times (VRN0 + 5R) / SUMRN$	PKN0[2:0] = "000"	VINN1
KVN2	$VLCD63 - GV \times (VRN0 + 9R) / SUMRN$	PKN0[2:0] = "001"	
KVN3	$VLCD63 - GV \times (VRN0 + 13R) / SUMRN$	PKN0[2:0] = "010"	
KVN4	$VLCD63 - GV \times (VRN0 + 17R) / SUMRN$	PKN0[2:0] = "011"	
KVN5	$VLCD63 - GV \times (VRN0 + 21R) / SUMRN$	PKN0[2:0] = "100"	
KVN6	$KVN6 \text{ } VLCD63 - GV \times (VRN0 + 25R) / SUMRN$	PKN0[2:0] = "101"	
KVN7	$VLCD63 - GV \times (VRN0 + 29R) / SUMRN$	PKN0[2:0] = "110"	
KVN8	$VLCD63 - GV \times (VRN0 + 33R) / SUMRN$	PKN0[2:0] = "111"	
KVN9	$VLCD63 - GV \times (VRN0 + 33R + VRHN) / SUMRN$	PKN1[2:0] = "000"	VINN2
KVN10	$VLCD63 - GV \times (VRN0 + 34R + VRHN) / SUMRN$	PKN1[2:0] = "001"	
KVN11	$VLCD63 - GV \times (VRN0 + 35R + VRHN) / SUMRN$	PKN1[2:0] = "010"	
KVN12	$VLCD63 - GV \times (VRN0 + 36R + VRHN) / SUMRN$	PKN1[2:0] = "011"	
KVN13	$VLCD63 - GV \times (VRN0 + 37R + VRHN) / SUMRN$	PKN1[2:0] = "100"	
KVN14	$VLCD63 - GV \times (VRN0 + 38R + VRHN) / SUMRN$	PKN1[2:0] = "101"	
KVN15	$VLCD63 - GV \times (VRN0 + 39R + VRHN) / SUMRN$	PKN1[2:0] = "110"	
KVN16	$VLCD63 - GV \times (VRN0 + 40R + VRHN) / SUMRN$	PKN1[2:0] = "111"	
KVN17	$VLCD63 - GV \times (VRN0 + 45R + VRHN) / SUMRN$	PKN2[2:0] = "000"	VINN3
KVN18	$VLCD63 - GV \times (VRN0 + 46R + VRHN) / SUMRN$	PKN2[2:0] = "001"	
KVN19	$VLCD63 - GV \times (VRN0 + 47R + VRHN) / SUMRN$	PKN2[2:0] = "010"	
KVN20	$VLCD63 - GV \times (VRN0 + 48R + VRHN) / SUMRN$	PKN2[2:0] = "011"	
KVN21	$VLCD63 - GV \times (VRN0 + 49R + VRHN) / SUMRN$	PKN2[2:0] = "100"	
KVN22	$VLCD63 - GV \times (VRN0 + 50R + VRHN) / SUMRN$	PKN2[2:0] = "101"	
KVN23	$VLCD63 - GV \times (VRN0 + 51R + VRHN) / SUMRN$	PKN2[2:0] = "110"	
KVN24	$VLCD63 - GV \times (VRN0 + 52R + VRHN) / SUMRN$	PKN2[2:0] = "111"	
KVN25	$VLCD63 - GV \times (VRN0 + 68R + VRHN) / SUMRN$	PKN3[2:0] = "000"	VINN4
KVN26	$VLCD63 - GV \times (VRN0 + 69R + VRHN) / SUMRN$	PKN3[2:0] = "001"	
KVN27	$VLCD63 - GV \times (VRN0 + 70R + VRHN) / SUMRN$	PKN3[2:0] = "001"	
KVN28	$VLCD63 - GV \times (VRN0 + 71R + VRHN) / SUMRN$	PKN3[2:0] = "011"	
KVN29	$VLCD63 - GV \times (VRN0 + 72R + VRHN) / SUMRN$	PKN3[2:0] = "100"	
KVN30	$VLCD63 - GV \times (VRN0 + 73R + VRHN) / SUMRN$	PKN3[2:0] = "101"	
KVN31	$VLCD63 - GV \times (VRN0 + 74R + VRHN) / SUMRN$	PKN3[2:0] = "110"	
KVN32	$VLCD63 - GV \times (VRN0 + 75R + VRHN) / SUMRN$	PKN3[2:0] = "111"	
KVN33	$VLCD63 - GV \times (VRN0 + 80R + VRHN) / SUMRN$	PKN4[2:0] = "000"	VINN5
KVN34	$VLCD63 - GV \times (VRN0 + 81R + VRHN) / SUMRN$	PKN4[2:0] = "001"	
KVN35	$VLCD63 - GV \times (VRN0 + 82R + VRHN) / SUMRN$	PKN4[2:0] = "010"	
KVN36	$VLCD63 - GV \times (VRN0 + 83R + VRHN) / SUMRN$	PKN4[2:0] = "011"	
KVN37	$VLCD63 - GV \times (VRN0 + 84R + VRHN) / SUMRN$	PKN4[2:0] = "100"	
KVN38	$VLCD63 - GV \times (VRN0 + 85R + VRHN) / SUMRN$	PKN4[2:0] = "101"	
KVN39	$VLCD63 - GV \times (VRN0 + 86R + VRHN) / SUMRN$	PKN4[2:0] = "110"	
KVN40	$VLCD63 - GV \times (VRN0 + 87R + VRHN) / SUMRN$	PKN4[2:0] = "111"	
KVN41	$VLCD63 - GV \times (VRN0 + 87R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "000"	VINN6
KVN42	$VLCD63 - GV \times (VRN0 + 91R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "001"	
KVN43	$VLCD63 - GV \times (VRN0 + 95R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "010"	
KVN44	$VLCD63 - GV \times (VRN0 + 99R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "011"	
KVN45	$VLCD63 - GV \times (VRN0 + 103R + VRHN + VRLN) / SUMRN$	PKN5[2:0] = "100"	

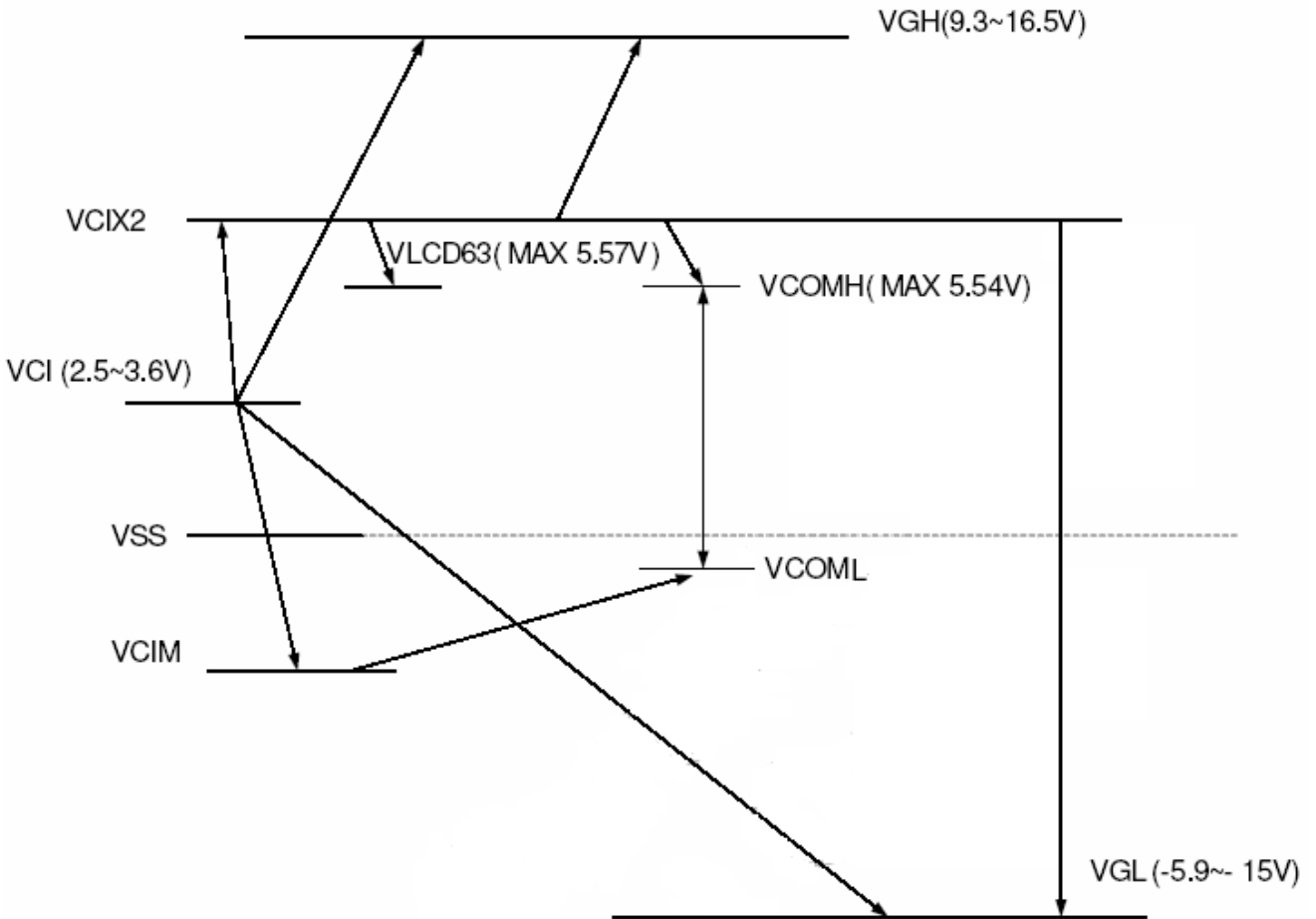
KVN46	$\text{VLCD63} - \text{GV} \times (\text{VRN0} + 107\text{R} + \text{VRHN} + \text{VRLN}) / \text{SUMRN}$	$\text{PKN5}[2:0] = \text{''101''}$	
KVN47	$\text{VLCD63} - \text{GV} \times (\text{VRN0} + 111\text{R} + \text{VRHN} + \text{VRLN}) / \text{SUMRN}$	$\text{PKN5}[2:0] = \text{''110''}$	
KVN48	$\text{VLCD63} - \text{GV} \times (\text{VRN0} + 115\text{R} + \text{VRHN} + \text{VRLN}) / \text{SUMRN}$	$\text{PKN5}[2:0] = \text{''111''}$	
KVN49	$\text{VLCD63} - \text{GV} \times (\text{VRN0} + 120\text{R} + \text{VRHN} + \text{VRLN}) / \text{SUMRN}$	-	VINN7

Table 14. 7 Reference Voltages of Negative Polarity

SUMRN: Total of the negative polarity ladder resistance = $128\text{R} + \text{VRHN} + \text{VRLN} + \text{VRN0} + \text{VRN1}$

GV: Voltage difference between VLCD63 and of EXVR.

15. Power on Sequence



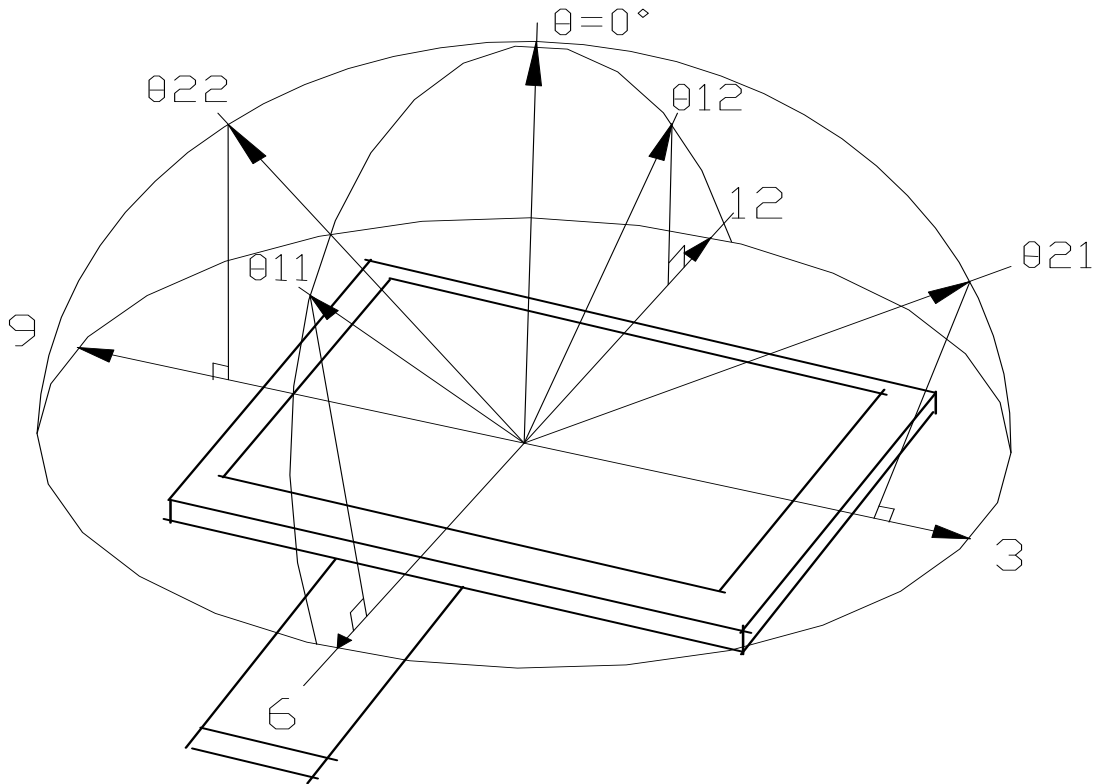
16. Optical Characteristics

16-1) Specification:

 $T_a=25^{\circ}\text{C}$

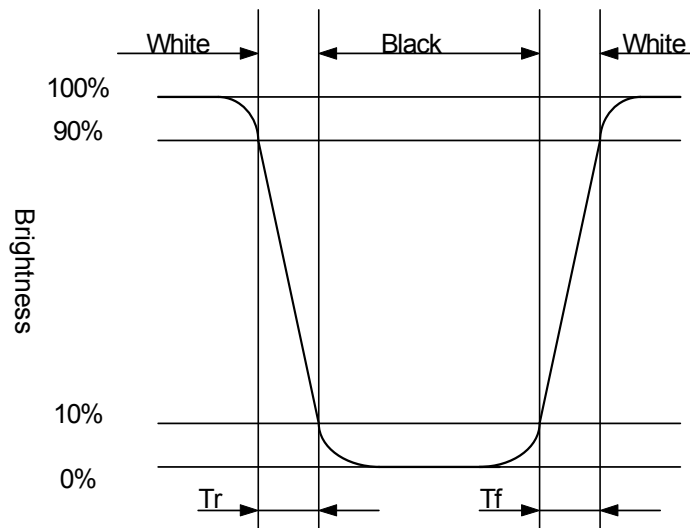
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ (Horizontal)	CR > 10	70	75	--	deg	Note 16-1
	Vertical	θ (12 o'clock)		45	50	--	deg	
		θ (6 o'clock)		55	60	--	deg	
Contrast Ratio		CR	At optimized Viewing angle	400	500	--	-	Note 16-2
Response time	Rise	Tr	$\theta=0^{\circ}$	--	15	30	ms	Note 16-3
	Fall	Tf		--	25	50	ms	
Brightness		L	$\theta=0^{\circ}/\varphi=0$	450	500	-	cd/m ²	Note 16-4
Luminance Uniformity		U	-	75	80	--	%	Note 16-6
White Chromaticity		x	$\theta=0^{\circ}/\varphi=0$	0.28	0.32	0.36	-	
		y		0.30	0.34	0.38	-	
LED Life Time			+25°C	20000	--	--	hrs	Note 16-5
Cross Talk			$\theta=0^{\circ}$	--	--	3.5	%	Note 16-7

Note 16-1: The definitions of viewing angles are as follow



Note 16-2: The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 16-3: Definition of Response Time T_r and T_f



Note 16-4: Topcon BM-5A or BM-7 fast luminance meter 1° field of view is used in the testing

Note 16-5: The “LED Life time “ is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25°C and $I_{LED} = 60\text{mA}$.

Note 16-6: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

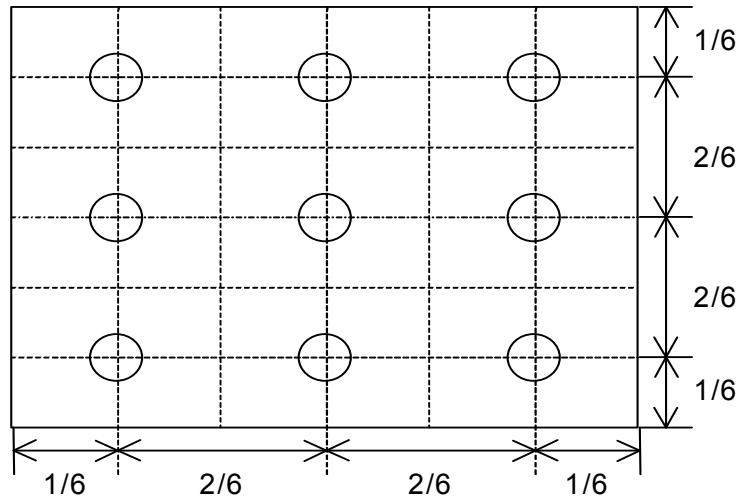
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).



Note 16-7: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A

YB: Brightness of Pattern B

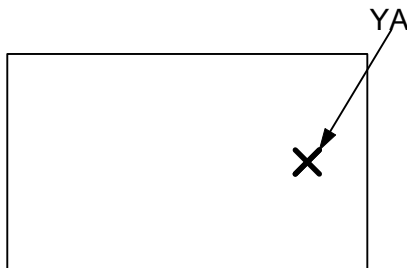
Luminance meter : BM 5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

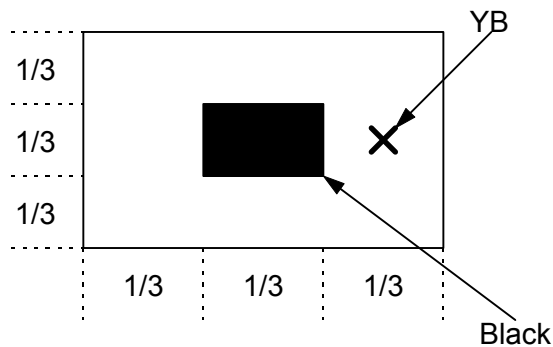
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

Pattern A
(Gray Level 31)



Pattern B
(Gray Level 31, central black box exclusive)



X: Measuring Point (A and B are at the same point.)

(Gray Level 0)

17. Handling Cautions

17-1) Mounting of module

- a) Please power off the module when you connect the input/output connector.
- b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- c) Protective film (Laminator) is applied on surface to protect it against scratches and dirt's.
- d) Please follow the tear off direction as figure 17-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

17-2) Precautions in mounting

- a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- c) TFT-LCD module uses glass, which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

17-3) Adjusting module

- a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
- b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

17-4) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- e) Observe all other precautionary requirements in handling general electronic components.
- f) Please adjust the voltage of common electrode as material of attachment by 1 module.

17-5) Polarizer mark

The polarizer mark is to describe the direction of wide view angle film how to mach up with the rubbing direction.

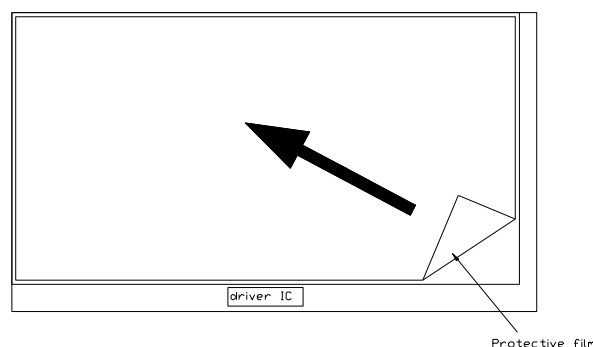


Figure 17-1 the way to peel off protective film

18. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = 95°C, 240 hrs
2	Low Temperature Storage Test	Ta = -40°C, 240 hrs
3	High Temperature Operation Test	Ta = 85°C, 240 hrs
4	Low Temperature Operation Test	Ta = -30°C, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = 60°C, 90%RH, 240 hrs (No Condensation)
6	Thermal Cycling Test (non-operating)	-25°C → 70°C, 200 Cycles 30min 30min
7	Vibration Test (non-operating)	Frequency : 10 ~ 55 Hz, Amplitude : 1 mm Sweep time: 11 min Test Period: 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal

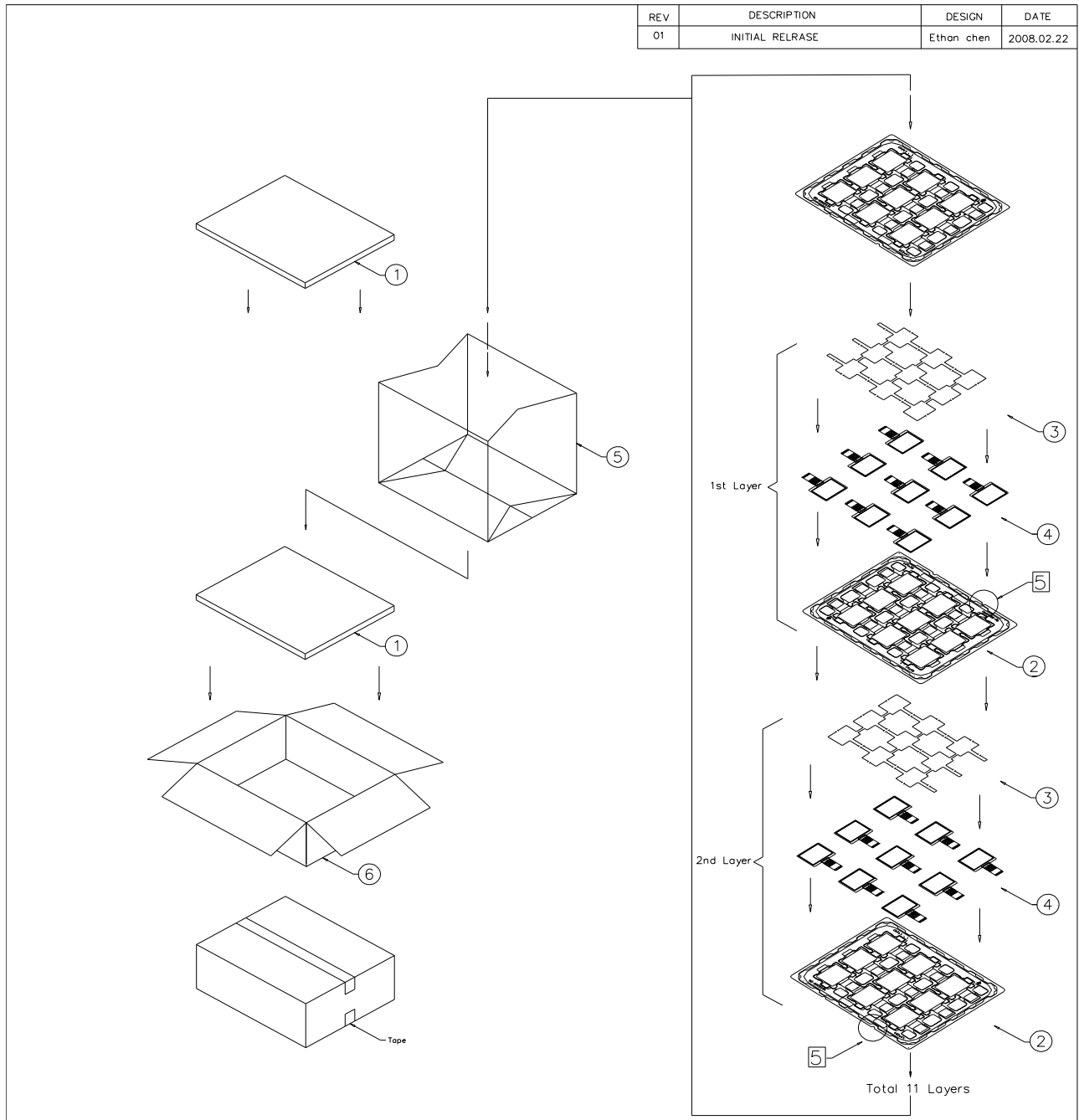
Ta: ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image).All the cosmetic specification is judged before the reliability stress.


19. Packing Diagram



NOTE:

- 1. One layer include: 1 piece of cushion sheet, 9 pcs panel & 1 piece of tray.
- 2. Q'TY: 99 pcs panel/carton.
- 3. Dimension: 455*375*190mm
- 4. Weight: 6.5 KG
- 5. tray需180°交叉堆疊, 堆疊後可從側邊檢視圓弧防呆方向是否正確

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
6	50-0100091	CARTON INTERNAL	1	
5	50-0500041	摺口袋450*380*700mm	1	抗靜電
4		PD035QX2	99	
3	50-0200117	EPE CUSHION SHEET	11	抗靜電
2	50-0302031	TRAY	12	抗靜電
1	50-0300491	EPE FOAM	2	

MTL.SPEC.		UNSPECIFIED TOL'S ±5.0mm		REMARK		 元太科技股份有限公司 Prime View International Co.,Ltd.	
		ANGLE					
		ROUGHNESS				DWG.TITLE	
APPROVE	Frank Shin	'08.02.22	SCALE	UNIT	SHEET	PD035QX2 PACKING Dim	
CHECK	Frank Shin	'08.02.22	1:1	mm	1 OF 1		
DESIGN	Ethan chen	'08.02.22	MTL.NO.		DWG.NO.		REV. 01
							A4
							SIZE