MI980

Intel ® 4th Generation Core / QM87 PCH
Mini ITX Motherboard

USER'S MANUAL

Version 1.0

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Introduction

Product Description

The MI980 Mini ITX motherboard is based on the latest Intel® QM87 chipset. The platform supports onboard 4th generation Intel® Core processor family features an integrated dual-channel DDR3 memory controller as well as a graphics core.

The latest Intel® processors provide advanced performance in both computing and graphics quality. This meets the requirement of customers in the gaming, POS, digital signage and server market segment.

The QM87 platform is made with 22-nanometer technology that supports Intel's first processor architecture to unite the CPU and the graphics core on the transistor level. The MI980 Mini ITX board utilizes the dramatic increase in performance provided this Intel's latest cutting-edge technology. Measuring 170mm x 170mm, the MI980 offers fast 6Gbps SATA support, USB3.0 and interfaces for DVI-D, DVI-I, LVDS and DP displays.

Checklist

Your MI980 package should include the items listed below.

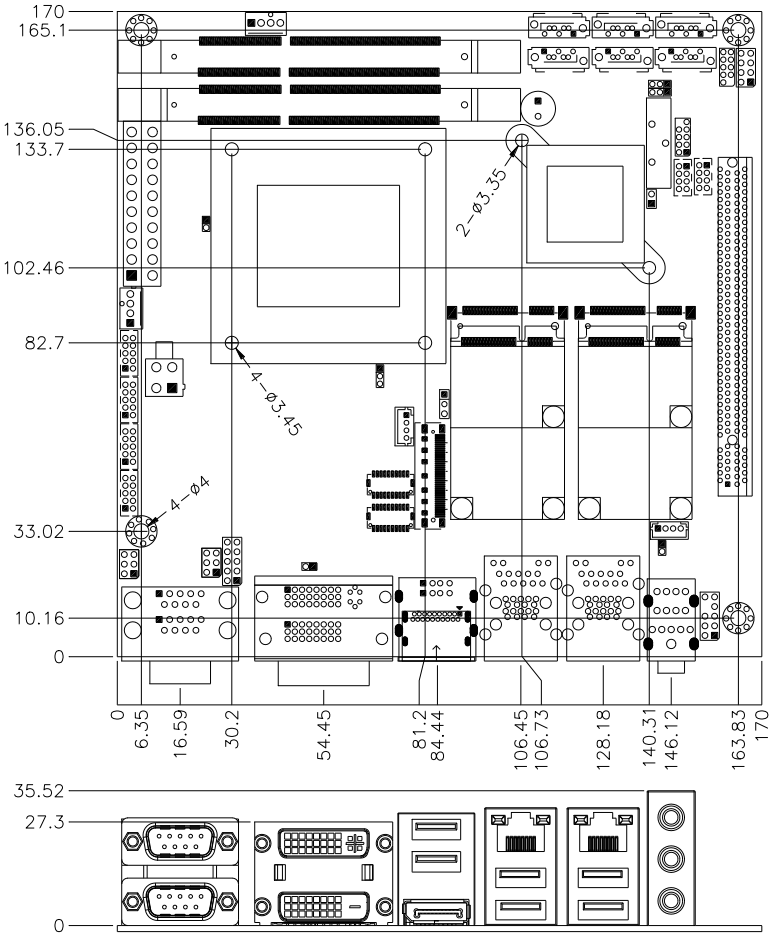
- The MI980 MINI ITX motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Serial ATA cable

MI980 Specifications

Product Name	**MI980VF [Supports iAMT 9.0 & vPro]** **MI980F [Supports EuP/ErP]**
Form Factor	Mini-ITX
CPU Type	- Intel® 4th Generation Core mobile processors (22nm monolithic) - BGA1364 , Package= 37.5 mmx 32 mm [Performance Halo SKUs] - TDP = 47W (QC) / 37W(DC)
Cache	Up to 8MB
Chipset	Intel® QM87 PCH Mobile Platform Controller Hub Package =23 mm x 22 mm, 0.65 mm ball pitch; TDP = 3W QM87 for MI980VF ; HM86 for MI980F
BIOS	AMI BIOS [16MB SPI ROM]
Memory	Intel® 4th Generation Core mobile processors integrated memory controller DDRIII 1600 MHz (supports dual channel DDR3/DDR3L) - SO-DIMM [204-pin vertical type] x 2 (Non-ECC), Max. 16GB
VGA	Intel® 4th Generation Core mobile processor integrated HD Gfx, supports 3 independent displays, Direct X 11.1, OpenGL 3.2, Open CL 1.2 ● DVI-I X 1 (Thru port B, via VGA@ QM87 PCH+ Level shifter ASM1442) ● DVI-D x 1 (Thru port C, with level shifter ASM1442) ● DisplayPort x 1 (Thru port D) ● LVDS (Thru eDP, via NXP PTN3460)
LAN	1. Intel® Clarkville I217LM GbE PHY [For MI980VF] or I217V GbE PHY [For MI980F] ** Package = 6mm x 6mm, QFN48** 2. Intel® Pearsonville I211AT as 2nd GbE
USB	USB 2.0 host controller [QM87 PCH integrated], supports **8** ports - 2 ports in the rear panel - 4 ports via onboard pin header (2.0mm pitch) - 2 ports via MiniPCIe sockets USB 3.0 host controller [QM87 PCH integrated] supports **4** ports - 4 ports in the rear panel for MI980VF
Serial ATA	Intel® QM87 PCH built-in SATA controller, supports 6 ports **4** x SATA (3.0) 6Gbps & shared mSATA for 1 port (SATA port #5) **2** x SATA (2.0) 3Gbps ** QM87 supports 4 x SATA III ; HM86 supports 2 x SATA III only**
Audio	Intel® Mobile QM87 PCH built-in High Definition Audio controller + Realtek ALC892 w/ 7.1 channels
LPC I/O	Fintek **F81866AD-I** (128-pin LQFP [14mm x 14 mm]) - COM #1 (RS232/422/485) supports ring-in with power @500mA (selectable for 5V or 12V) [EXAR SP339EER1 232/422/485 transceiver x 1 for jumper-less] - COM #2 (RS232 only), supports ring-in with power @500mA (selectable for 5V or 12V) - COM #3~COM #6 (RS232 only) Hardware Monitor (2 thermal, 4 voltage monitor inputs & 2 fan headers) - CPU fan x 1(PWM fan type, 4-pin connector) - SYS fan x 1 (DC/PWM Auto-Detect fan type, 4-pin connector)]
Digital IO	4 in & 4 out
TPM 1.2	Nuvoton WPCT210AA0WX (MI980VF only) **Operation temperature for 0 ~ +60 degree C only**
iAMT	Intel® Mobile QM87 PCH built-in - Intel® Active Management Technology, version 9.0 (MI980VF only)
Expansion Slots	- PCI-Express (16x) x1 [Gen 3.0 PEG] - Mini PCI-Express x 2 port [Full-sized], both support USB 2.0 - One slot supports mSATA (6Gbps)

Edge Connectors	Dual DB9 stack connector for COM #1 / #2 DVI-D + DVI-I stack connector x 1 DisplayPort + dual USB (2.0) stack connector x 1 RJ-45 + dual USB (3.0) stack connector x 2 Triplet type Jack 3 x 1 for HD Audio
Onboard Header/Connector	4 ports x SATA **III** [Blue color] (For MI980VF) 2 ports x SATA **III** [Blue color] (For MI980F) 2 ports x SATA **II** DF-11 8-pin connector x 2 for 4 ports USB 2.0 DF-20 20-pin connector x 2 for dual –channel LVDS eDP LVDS panel connector x 1 2x5 pin-header x 1 for front panel audio [supports 7.1 Channel] DF-11 10-pin header x 4 for COM3 ~ COM6 2x5 pin-header x 1 for Digital IO 4-pin box header x 1 for LCD backlight control
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
System Voltage	ATX standard 20-pin type 4 pin type (+12V only)[For full system loading usage]
Others	- vPro [MI980VF only] - ErP feature (F81866AD-I integrated, WOL from 2nd GbE) - iSMART (via TI MSP430G2433 MCU) - AT24C02C EEPROM [SO8 type] via SMbus (Reserved)
Board Size	170mm x 170mm

Board Dimensions



Installations

This section provides information on how to use the jumpers and connectors on the MI980 in order to set up a workable system. The topics covered are:

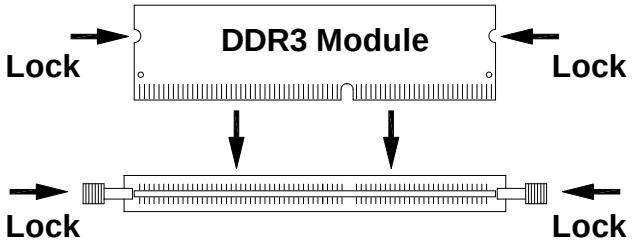
Installing the Memory

The MI980 board supports two DDR3 memory socket for a maximum total memory of 16GB in DDR3 SODIMM memory type.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

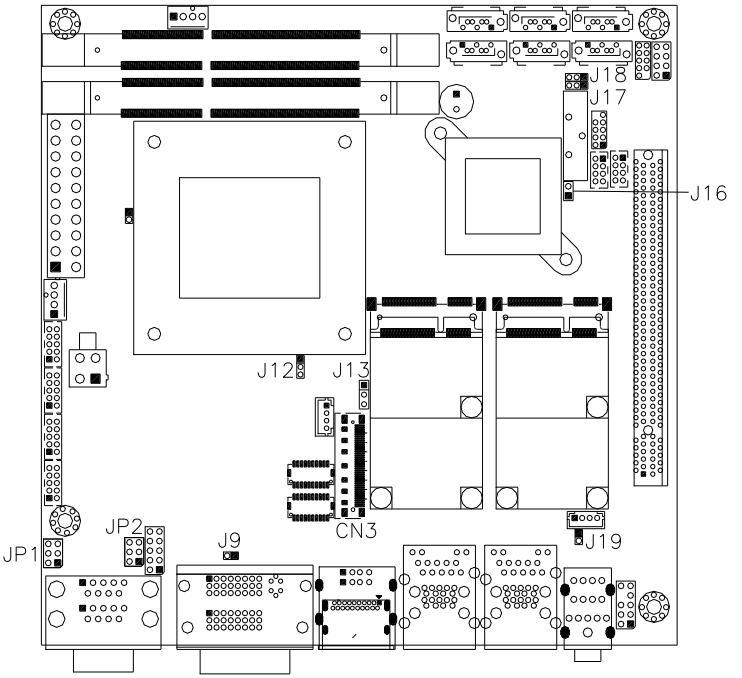
1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.
2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.
3. To remove the DDR3 module, press the clips with both hands.



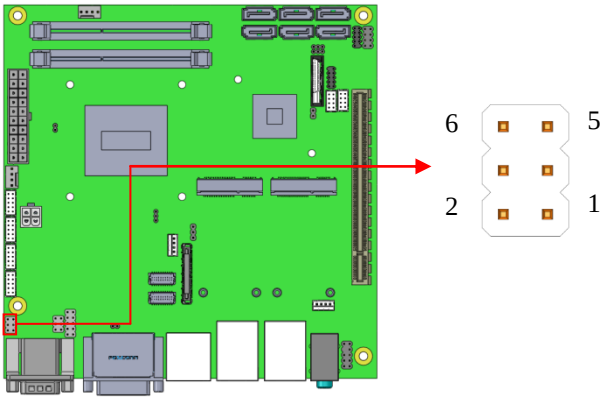
Setting the Jumpers

Jumpers are used on MI980 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on MI980 and their respective functions.

Jumper Locations on MI980

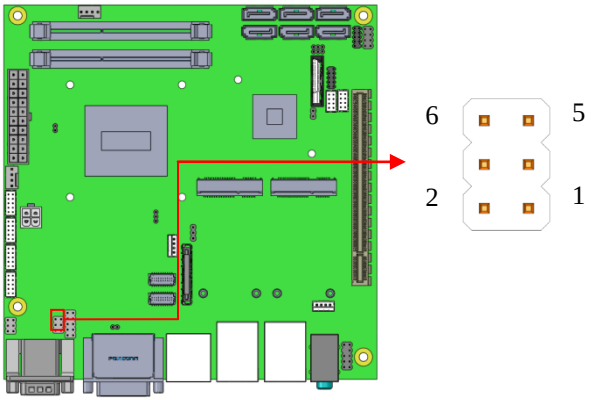


JP1: COM2 RS232 RI/+5V/+12V Power Setting



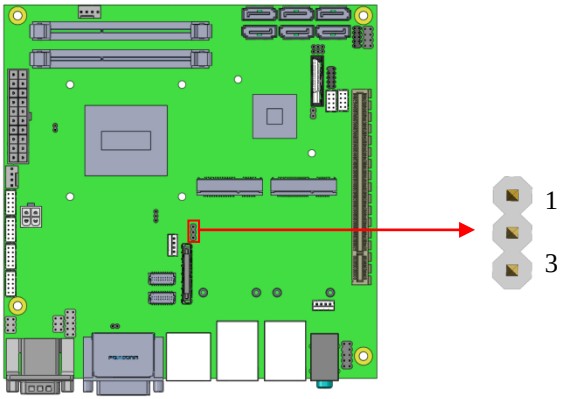
JP1	Setting	Function
	Pin 1-3, Short/Closed	+12V
	Pin 3-4, Short/Closed	RI
	Pin 3-5, Short/Closed	+5V

JP2: COM1 RS232 RI/+5V/+12V Power Setting



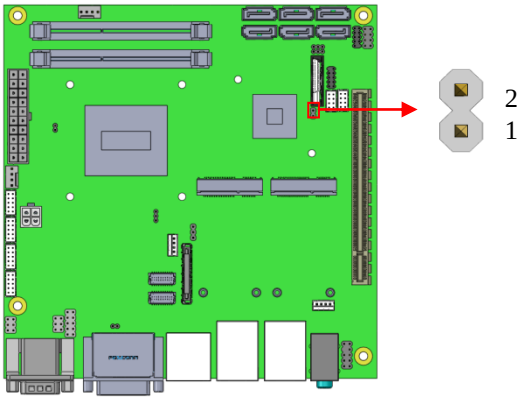
JP2	Setting	Function
	Pin 1-3, Short/Closed	+12V
	Pin 3-4, Short/Closed	RI
	Pin 3-5, Short/Closed	+5V

J13: LCD Panel Power Selection



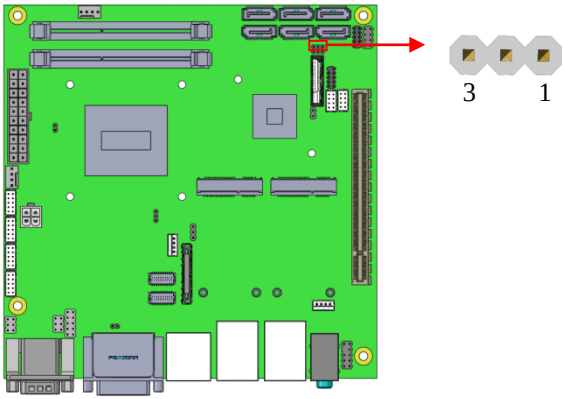
J13	LCD Panel Power
	3.3V
	5V

J16: Flash Descriptor Security Override (Factory use only)



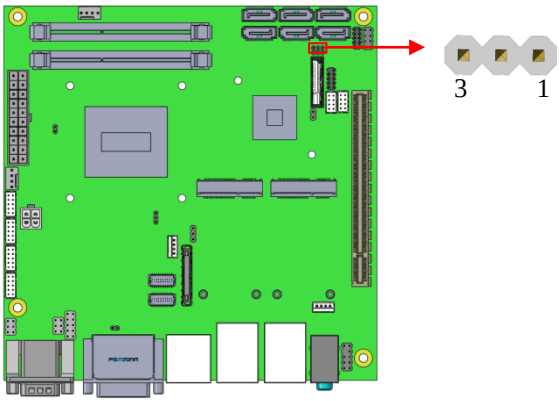
J16	Flash Descriptor Security Override
Open	Disabled (Default)
Close	Enabled

J17: Clear CMOS Contents



J17	Setting	Function
1 2 3	Pin 1-2 Short/Closed	Normal
1 2 3	Pin 2-3 Short/Closed	Clear CMOS

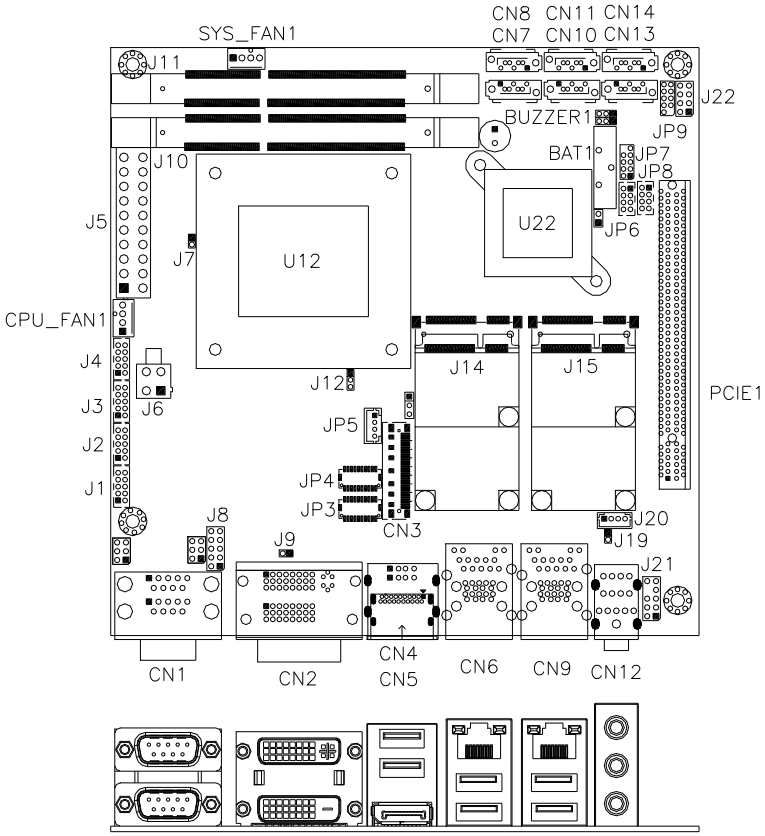
J18: Clear ME Contents

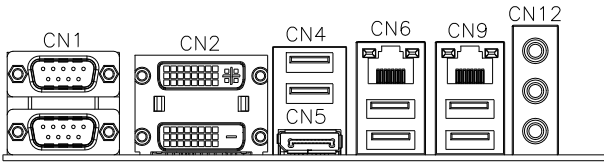


J18	Setting	Function
1 2 3	Pin 1-2 Short/Closed	Normal
1 2 3	Pin 2-3 Short/Closed	Clear CMOS

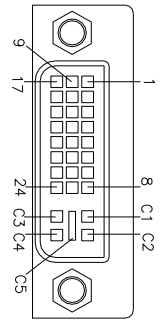
Connectors on MI980

Connector Locations on MI980

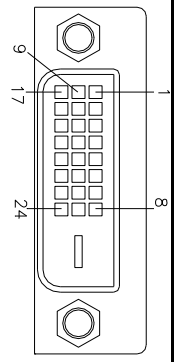




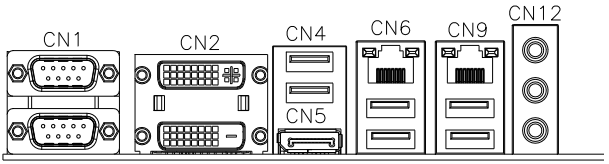
CN2: DVI-I and DVI-D Connector



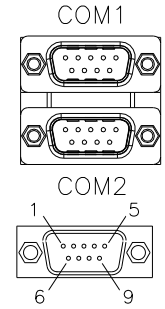
Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	HOT POWER
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
Analog VSYNC	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	Analog Red
SHIELD 1/3	11	C2	Analog Green
DATA 3-	12	C3	Analog Blue
DATA 3+	13	C4	Analog HSYNC
DDC POWER	14	C5	A GROUND2
A GROUND 1	15	C6	A GROUND3



Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	HOT POWER
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
N.C	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	N.C.
SHIELD 1/3	11	C2	N.C.
DATA 3-	12	C3	N.C.
DATA 3+	13	C4	N.C.
DDC POWER	14	C5	N.C.
A GROUND 1	15	C6	N.C.



CN1: COM1 and COM2 Serial Ports



Pin #	Signal Name		
	RS-232	R2-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC
10	NC	NC	NC

CN4: Display Port

Signal Name	Pin #	Pin #	Signal Name
LANE0_P	1	11	GND
GND	2	12	LANE3_N
LANE0_N	3	13	GND
LANE1_P	4	14	GND
GND	5	15	AUX_P
LANE1_N	6	16	GND
LANE2_P	7	17	AUX_N
GND	8	18	HPD
LANE2_N	9	19	GND
LANE3_P	10	20	VCC3.

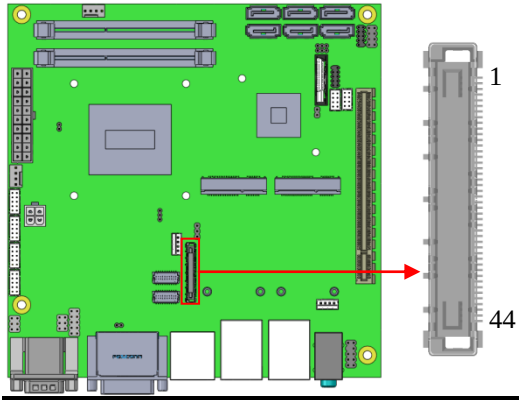
CN5: USB2 #6/#7

CN6: Gigabit LAN (I217) + USB3 #0/#1

CN7, CN8: SATA3 Connectors

CN9: Gigabit LAN (I211) + USB3 #2/#3

CN3: eDP Connector (JAE_FI-TD44SB-E-R750)



Signal Name	Pin #	Pin #	Signal Name
3.3V	1	23	TXN0
3.3V	2	24	TXP0
3.3V	3	25	GND
3.3V	4	26	AUXP
3.3V	5	27	AUXN
GND	6	28	NC
GND	7	29	VCC3
GND	8	30	NC
GND	9	31	VCC12
HPD	10	32	NC
NC	11	33	GND
NC	12	34	VCC5
GND	13	35	NC
NC	14	36	Brightness
NC	15	37	BKLT_EN
GND	16	38	VCC12
NC	17	39	VCC3
NC	18	40	GND
GND	19	41	SMB_THRM_CLK
TXN1	20	42	SMB_THRM_DATA
TXP1	21	43	NC
GND	22	44	NC

CN10: SATA2 Connector (MI980VF only)

CN11: SATA2 Connectors

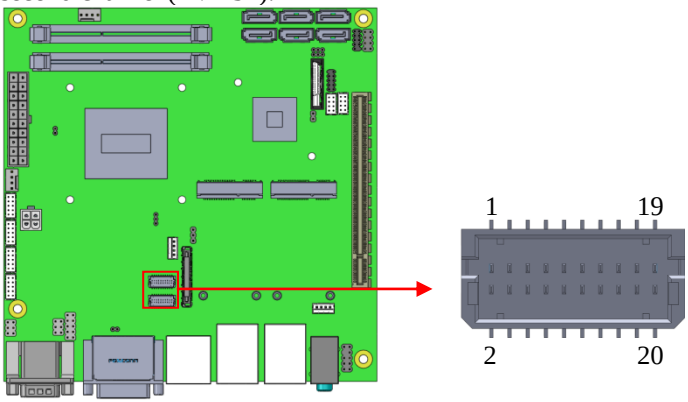
CN12: HD Audio Connector

CN13: SATA3 Connector (MI980VF only)

CN14: SATA3 Connector support MI980VF
Or SATA2 Connector support MI980F

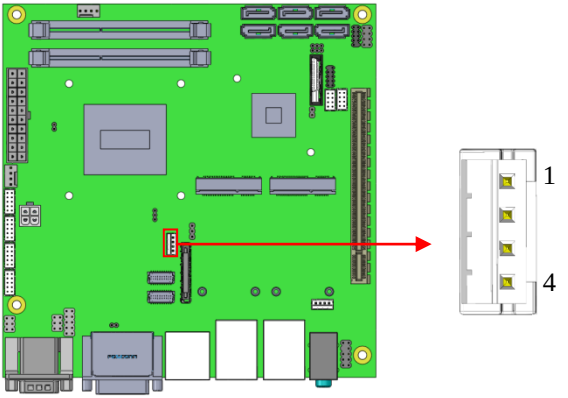
JP3, JP4: LVDS Connectors (LVDS2, LVDS1) Hirose DF20G-20DP-1V

The LVDS connectors on board consist of the first channel (LVDS1) and second channel (LVDS2).



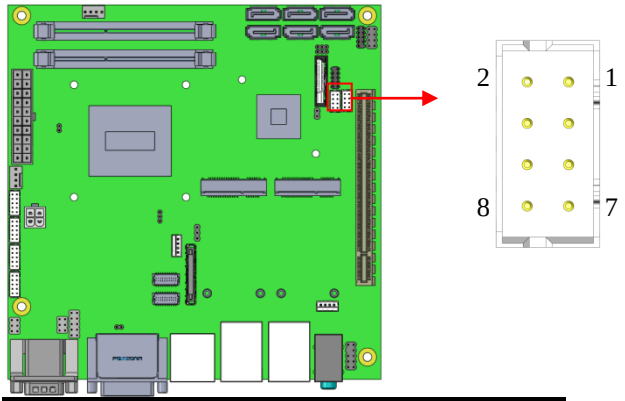
Signal Name	Pin #	Pin #	Signal Name
TX0N	2	1	TX0P
Ground	4	3	Ground
TX1N	6	5	TX1P
Ground	8	7	Ground
TX2N	10	9	TX2P
Ground	12	11	Ground
CLKN	14	13	CLKP
Ground	16	15	Ground
TX3N	18	17	TX3P
Power	20	19	Power

JP5: LCD Backlight Connector



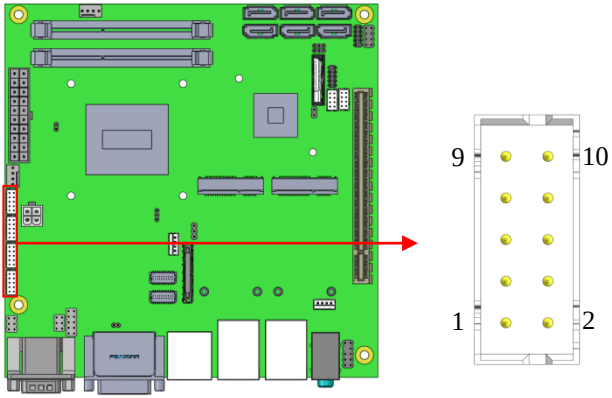
Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Brightness Control
4	Ground

JP6, JP8: USB2 #8/#9, USB2 #4/#5 Connectors



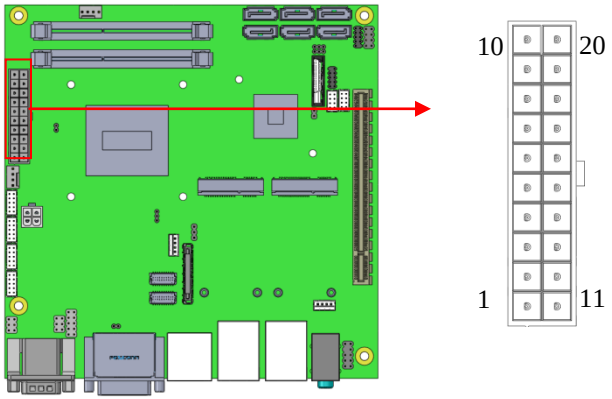
Signal Name	Pin #	Pin #	Signal Name
Vcc	1	2	Ground
D0-	3	4	D1+
D0+	5	6	D1-
Ground	7	8	Vcc

J1, J2, J3, J4: COM6, COM5, COM3, COM4 RS232 Serial Ports (HIROSE DF11-10DP-2DSA)



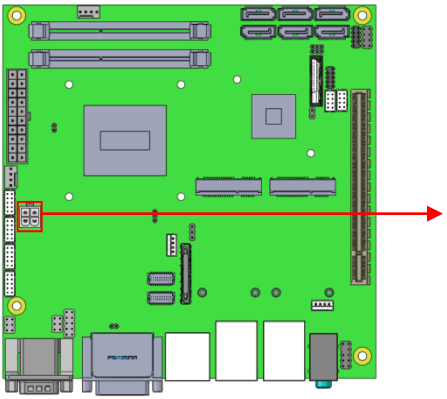
Signal Name	Pin #	Pin #	Signal Name
DCD#	1	2	SIN#
SOUT	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS#
RI#	9	X	KEY

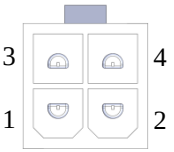
J5: ATX Power Supply Connector



Signal Name	Pin #	Pin #	Signal Name
3.3V	11	1	3.3V
-12V	12	2	3.3V
Ground	13	3	Ground
PS-ON	14	4	+5V
Ground	15	5	Ground
Ground	16	6	+5V
Ground	17	7	Ground
-5V	18	8	Power good
+5V	19	9	5VSB
+5V	20	10	+12V

J6: ATX 12V Power Connector





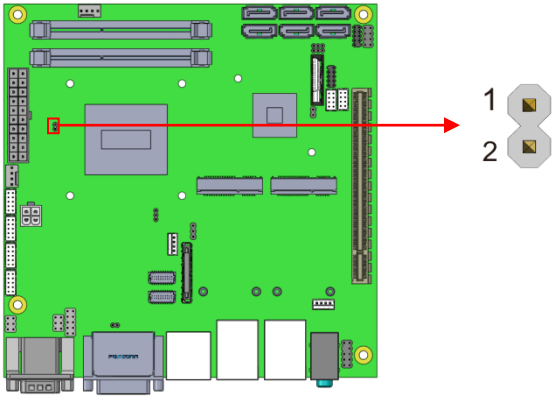
This connector supplies the CPU operating voltage.

Pin #	Signal Name
1	Ground
2	Ground
3	+12V
4	+12V

JP7: LPC debug Connector (Factory use only)

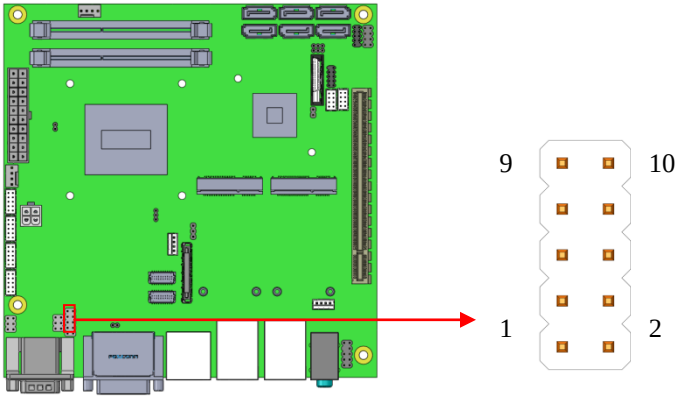
JP9: SPI Flash Connector (Factory use only)

J7: PCIE1 Configuration



J7	PCIE1 Configuration
Open	PCIE X16 (Default)
Short	PCIE X8, X8

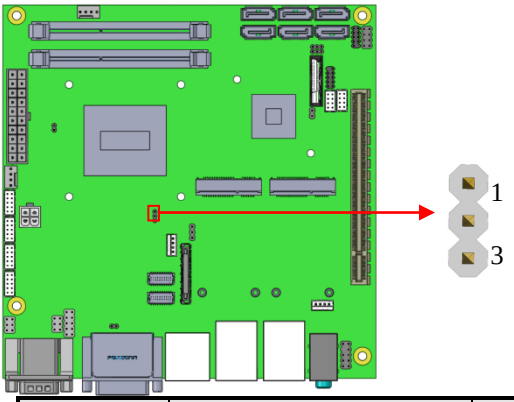
J8: Digital I/O Connector (4 in, 4 out)



Signal Name	Pin #	Pin #	Signal Name
Ground	1	2	+5V
Out3	3	4	Out1
Out2	5	6	Out0
IN3	7	8	IN1
IN2	9	10	IN0

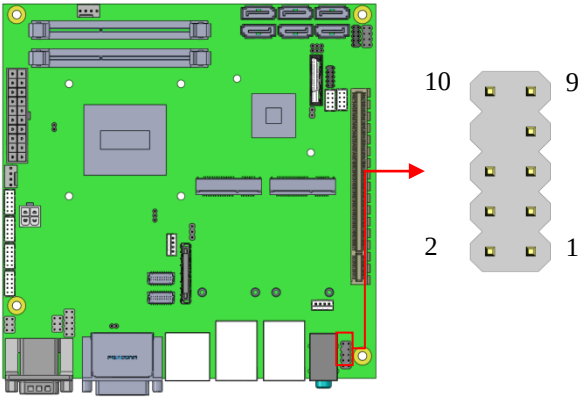
J10, J11: DDR3 SO-DIMM Socket

J12: LVDS/eDP Select



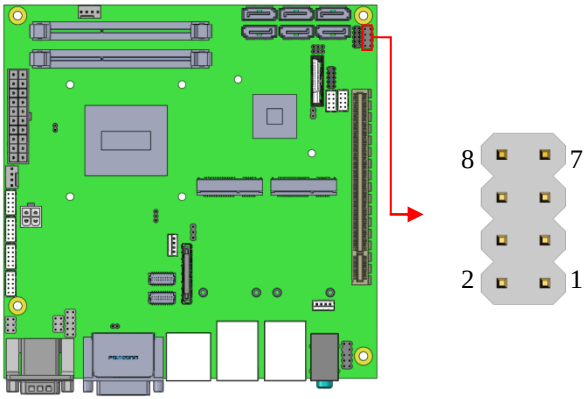
J12	Setting	Function
	Pin 1-2, Short/Closed	eDP Connector
	Pin 2-3, Short/Closed	LVDS

J21: Audio Pin Header for Chassis Front Panel



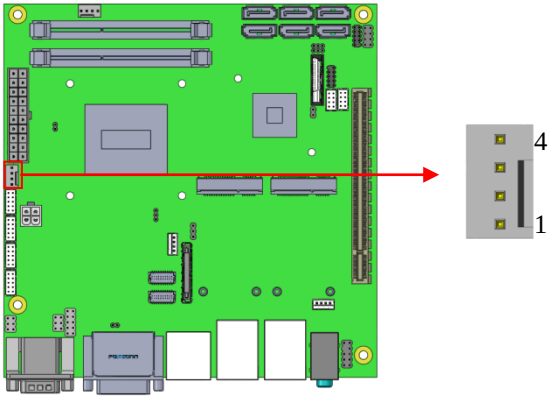
Signal Name	Pin #	Pin #	Signal Name
MIC IN_L	1	2	Ground
MIC IN_R	3	4	DET
LINE_R	5	6	Ground
Sense	7	8	KEY
LINE_L	9	10	Ground

J22: Front Panel



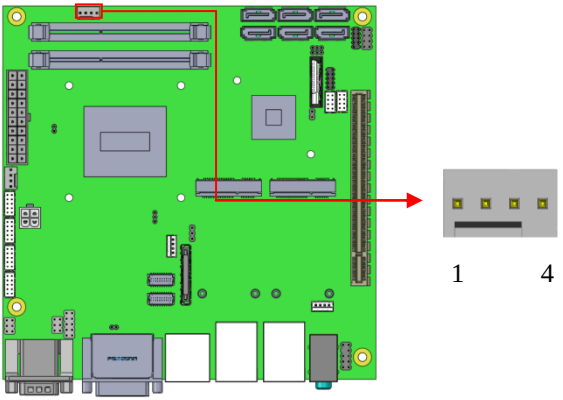
Signal Name	Pin #	Pin #	Signal Name
Power BTN	1	2	Power BTN
HDD LED+	3	4	HDD LED-
Reset BTN	5	6	Reset BTN
Power LED+	7	8	Power LED-

CPU_FAN1: CPU Fan Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Control

SYS_FAN2: System Fan Power Connector (DC/PWM Auto-Detect)



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Control

J14: Mini PCIE/mSATA (share with CN7) Connector

J15: Mini PCIE Connector

BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

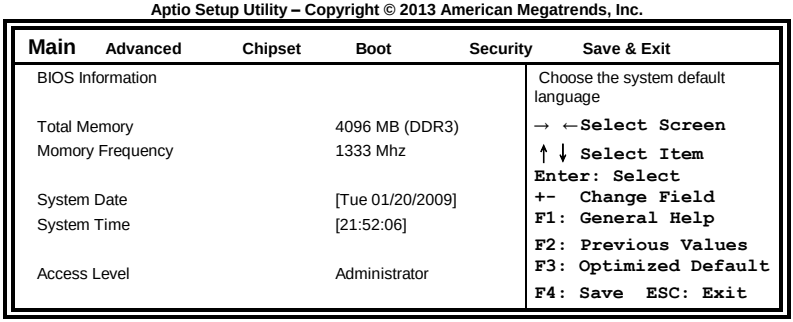
```
Press  <DEL>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

Main Settings



System Date

Set the Date. Use Tab to switch between Data elements.

System Time

Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

► PCI Subsystem Settings
► ACPI Settings
► Wake up event setting
► Trusted Computing
► CPU Configuration
► SATA Configuration
► Shutdown Temperature Configuration
► iSmart Controller
► AMT Configuration
► USB Configuration
► F81866 Super IO Configuration
► F81866 H/W Monitor

→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

PCI Subsystem Settings

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

PCI Bus Driver Version V 2.0502

PCI Common Settings
PCI Latency Timer 32 PCI Bus Clocks
VGA Palette Snoop Disabled
PERR# Generation Disabled
SERR# Generation Disabled

► PCI Express Settings

→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

PCI Latency Timer
Value to be programmed into PCI Latency Timer Register.

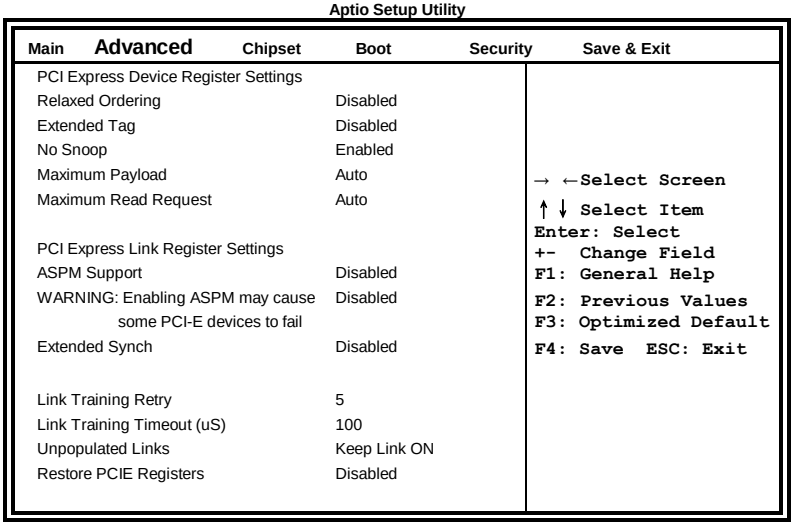
VGA Palette Snoop
Enables or disables VGA Palette Registers Snooping.

PERR# Generation
Enables or disables PCI device to generate PERR#.

SERR# Generation
Enables or disables PCI device to generate SERR#.

PCI Express Settings
Change PCI Express devices settings.

PCI Express Settings



Relaxed Ordering
Enables or disables PCI Express Device Relaxed Ordering.

Extended Tag
If ENABLED allows device to use 8-bit Tag field as a requester.

No Snoop
Enables or disables PCI Express Device No Snoop option.

Maximum Payload
Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Maximum Read Request
Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support
Set the ASPM Level: Force L0s – Force all links to L0s State:
AUTO – BIOS auto configure: DISABLE – Disables ASPM.

Extended Synch
If ENABLED allows generation of Extended Synchronization patterns.

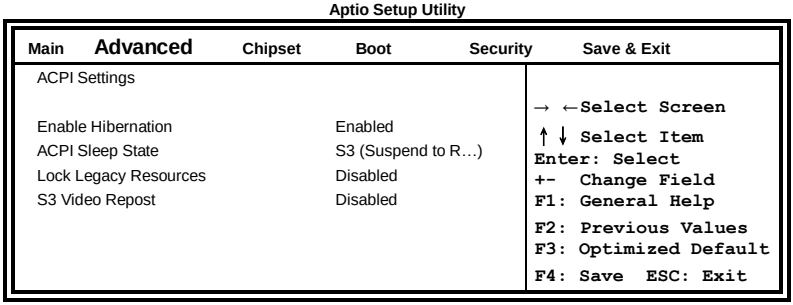
Link Training Retry
Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Link Training Timeout (uS)
Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

Unpopulated Links
In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

Restore PCIE Registers
On non-PCI Express aware OS's (Pre Windows Vista) some devices may not be correctly reinitialized after S3.Enabling this restore PCI Express device configuration on S3 resume
Warning: Enabling this may cause issues with other hardware after S3 resume.

ACPI Settings



Enable Hibernation

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State

Select ACPI sleep state the system will enter, when the *SUSPEND* button is pressed.

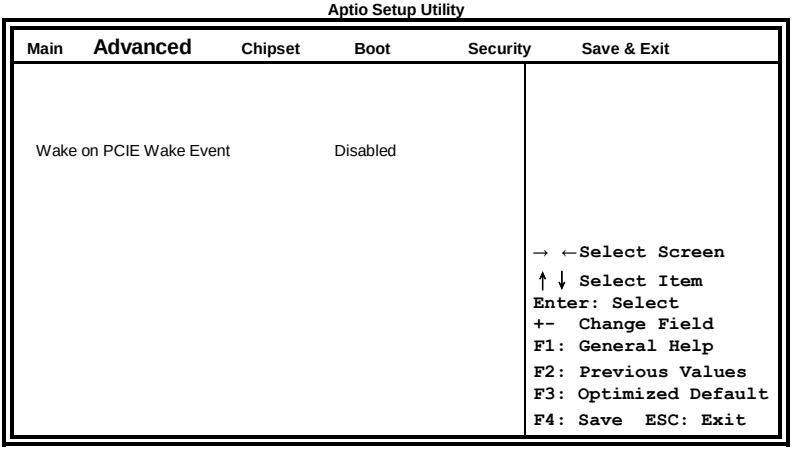
Lock Legacy Resources

Enabled or Disabled Lock of Legacy Resources.

S3 Video Repost

Enable or disable S3 Video Repost.

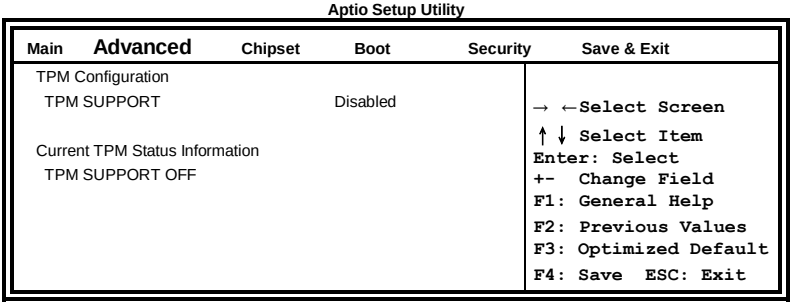
Wake up event settings



Wake on PCIE PME Wake Event

The options are Disabled and Enabled.

Trusted Computing



TPM Support

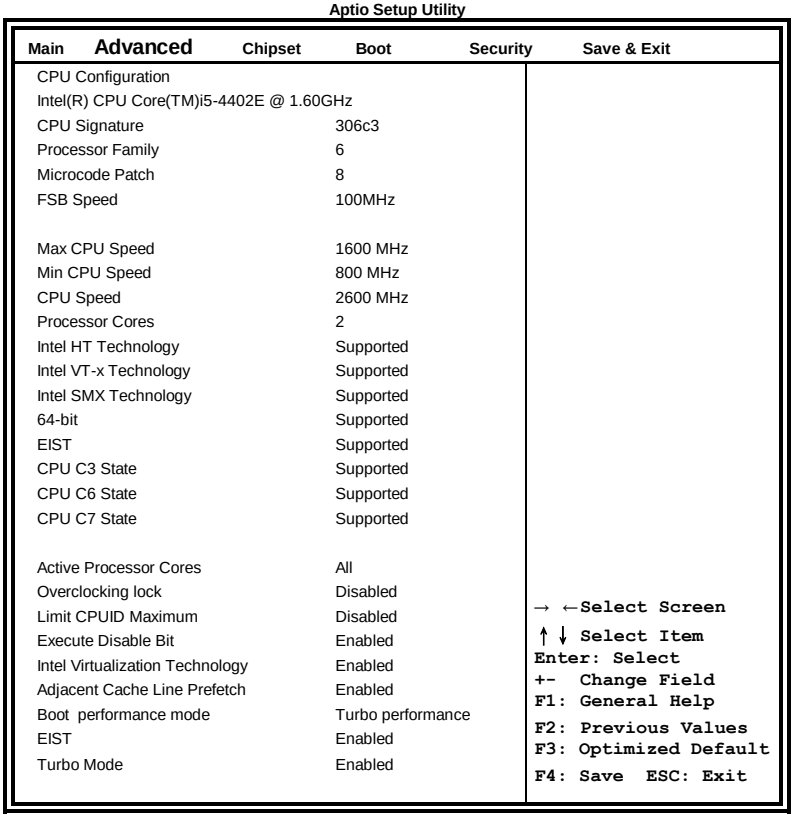
This configuration is supported only with MI980VF. Enables or Disables TPM support. O.S. will not show TPM. Reset of platform is required.

Security Device Support

Enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

CPU Configuration

This section shows the CPU configuration parameters.



Active Processor Cores

Number of cores to enable in each processor package.

Overclocking lock

Flex_RATIO(194)MSR

Limit CPUID Maximum

Disabled for Windows XP.

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS

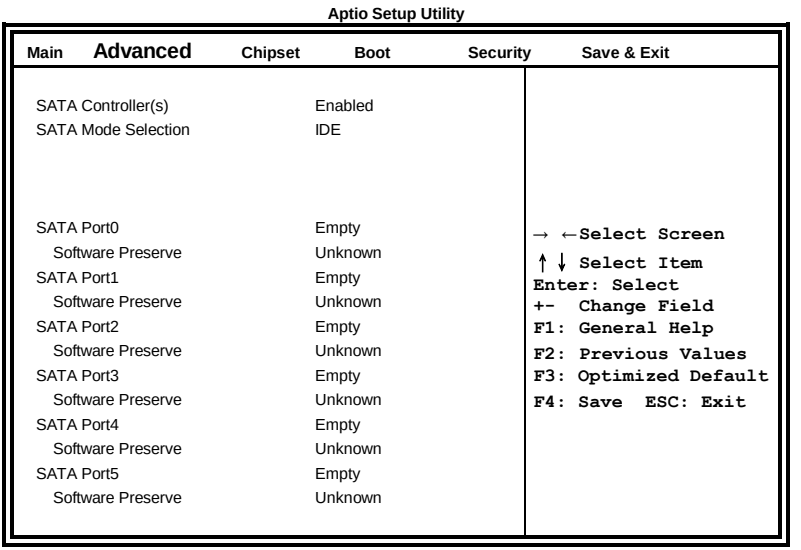
Intel Virtualization Technology
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Adjacent Cache Line Prefetch
To turn on/off prefetching of adjacent cache lines.

Boot Performance Mode
Select the performance state that the BIOS will set before OS handoff.

EIST
Enabled/Disabled Intel Speedstep.

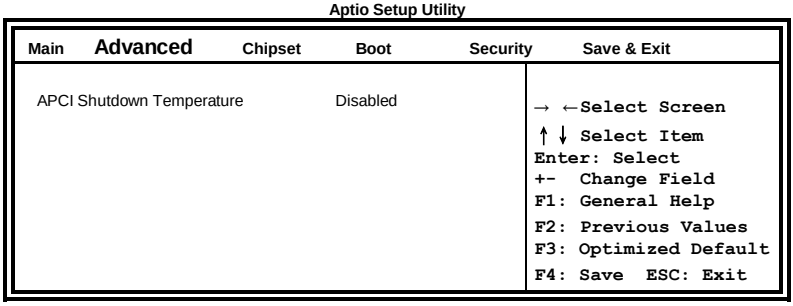
SATA Configuration
SATA Devices Configuration.



SATA Controller(s)
Enable / Disable Serial ATA Controller.

SATA Mode Selection
(1) IDE Mode.
(2) AHCI Mode.
(3) RAID Mode. (This configuration is supported only with MI980VF)

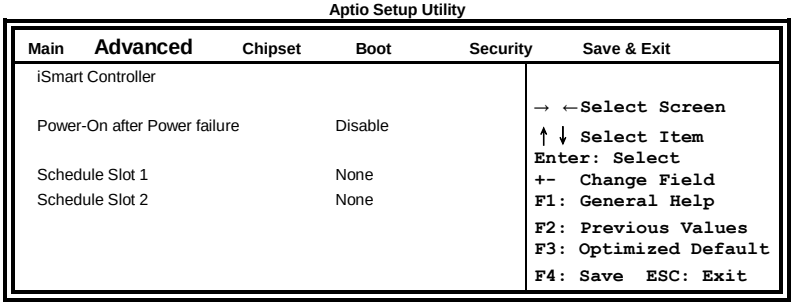
Shutdown Temperature Configuration



ACPI Shutdown Temperature

The default setting is Disabled.

iSmart Controller



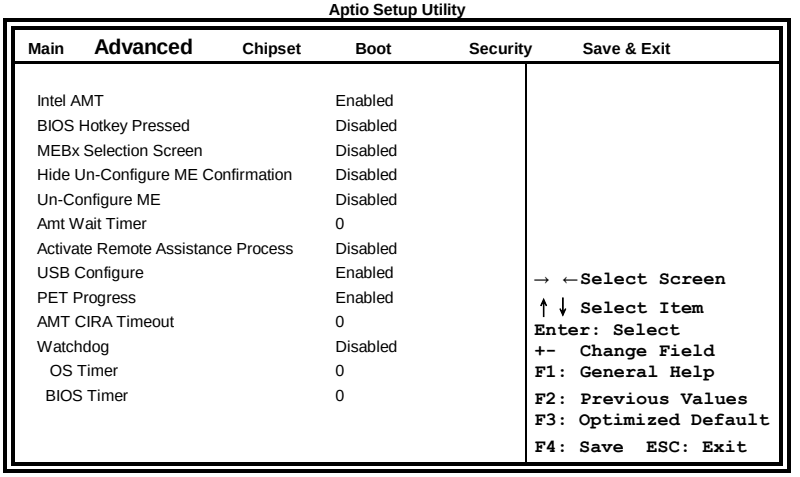
iSmart Controller

Setup the power on time for the system.

Schedule Slot 1 / 2

Setup the hour/minute for system power on.

AMT Configuration



AMT Configuration
This configuration is supported only with MI980VF (with iAMT function). Options are Enabled and Disabled.
Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

Unconfigure ME
Perform AMT/ME unconfigure without password operation.

Amt Wait Timer
Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

Activate Remote Assistance Process
Trigger CIRA boot.

PET Progress
User can Enable/Disable PET Events progress to receive PET events or not.

Watchdog Timer
Enable/Disable Watchdog Timer.

USB Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

USB Configuration		
USB Devices:		
2 Hubs		
Legacy USB Support	Enabled	→ ←Select Screen
USB3.0 Support	Enabled	↑ ↓ Select Item
XHCI Hand-off	Enabled	Enter: Select
EHCI Hand-off	Enabled	+- Change Field
USB Mass Storage Driver Support	Enabled	F1: General Help
USB hardware delays and time-outs:		F2: Previous Values
USB Transfer time-out	20 sec	F3: Optimized Default
Device reset tine-out	20 sec	F4: Save ESC: Exit
Device power-up delay	Auto	

Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

USB3.0 Support

Enable/Disable USB3.0 (XHCI) Controller support.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off

Enabled/Disabled. This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB Mass Storage Driver Support

Enable/Disable USB Mass Storage Driver Support.

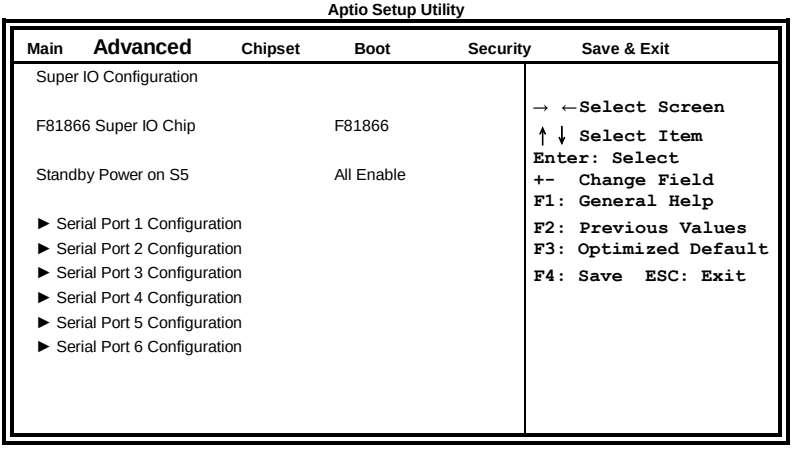
USB Transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

Device reset tine-out
USB mass Storage device start Unit command time-out.

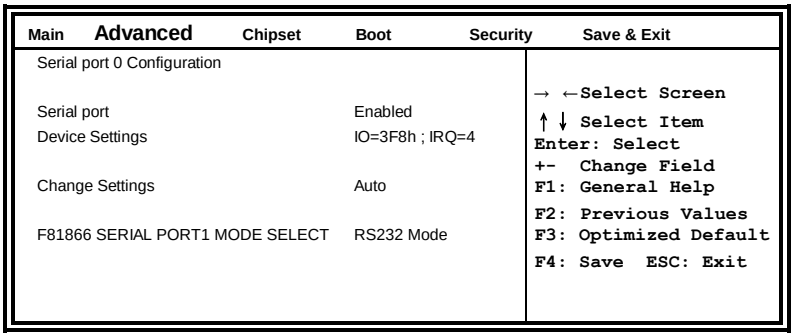
Device power-up delay
Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

F81866 Super IO Configuration



Standby Power On S5
This configuration is supported only with MI980F.
[Enable]Provide the standby power for devices.
[Disabled] Shutdown the standby power.

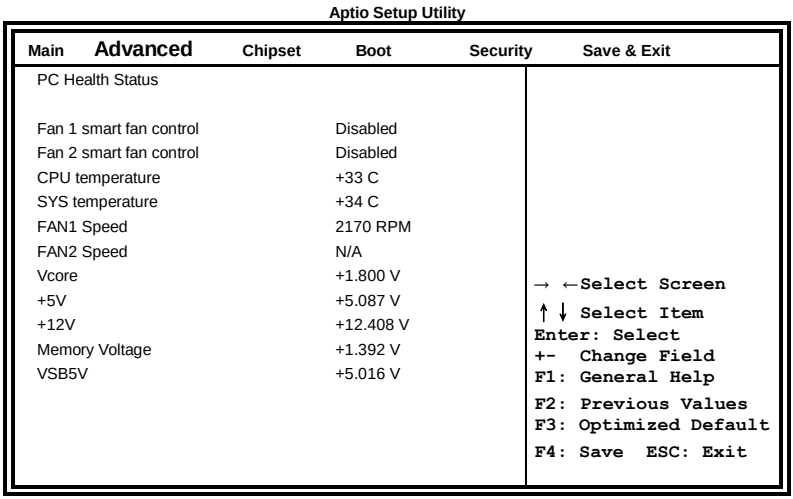
Serial Port Configuration
Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.



F81866 SERIAL PORT1 MODE SELECT

For RS232/RS422/RS485 mode select

F81866 H/W Monitor



Temperatures/Voltages

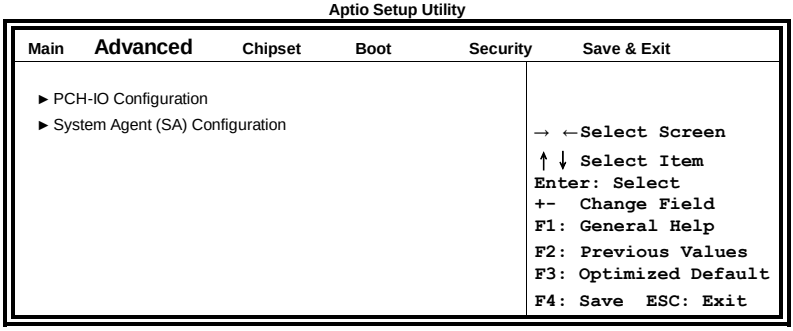
These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

Fan1/Fan2 Smart Fan Control

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

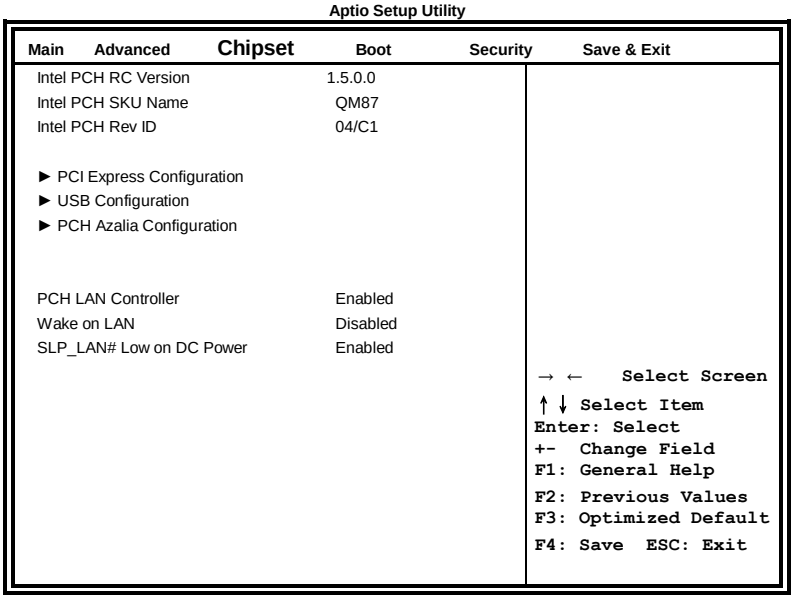
Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



PCH-IO Configuration

This section allows you to configure the North Bridge Chipset.



PCH LAN Controller

Enable or disable onboard NIC.

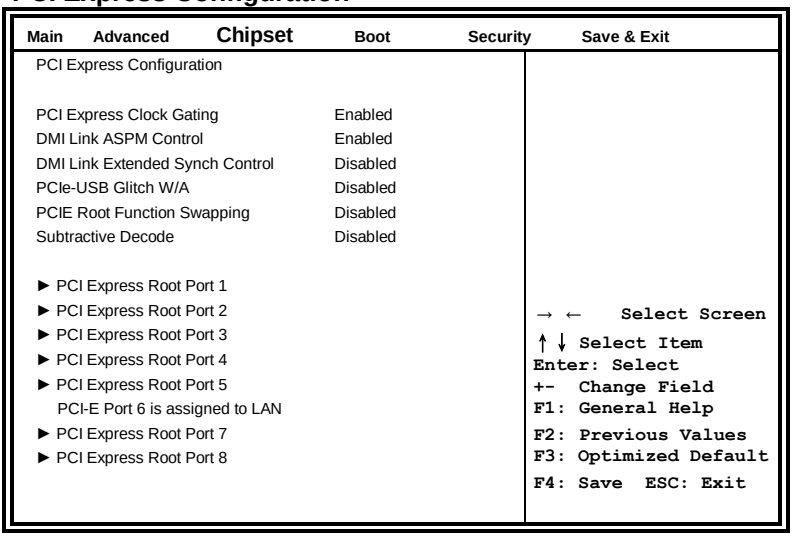
Wake on LAN

Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

SLP_LAN# Low on DC Power

Enable or Disable SLP_LAN# Low on DC Power

PCI Express Configuration



PCI Express Clock Gating

Enable or disable PCI Express Clock Gating for each root port.

DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI link.

PCIe-USB Glitch W/A

PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG port.

USB Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
USB Configuration					
USB Precondition			Disabled		→ ← Select Screen
xHCI Mode			Auto		↑ ↓ Select Item
USB Ports Per-Port Disable Control			Disabled		Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

USB Precondition

Precondition work on USB host controller and root ports for faster enumeration.

xHCI Mode

Mode of operation of xHCI controller.

USB Ports Per-Port Disable Control

Control each of the USB ports (0~13) disabling.

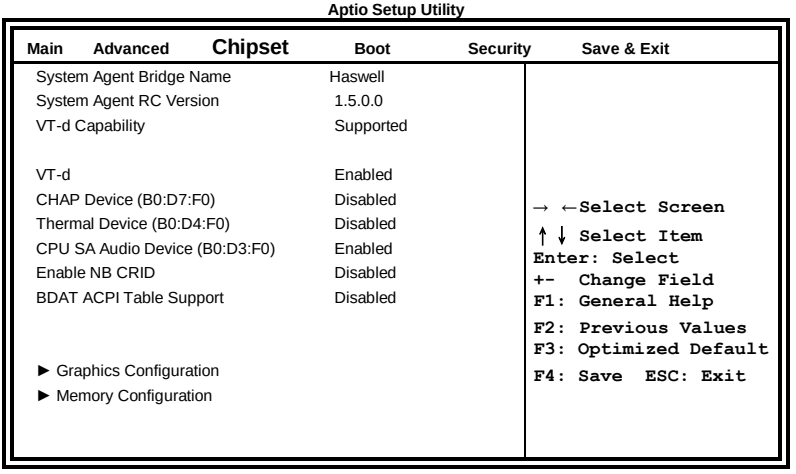
PCH Azalia Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
PCH Azalia Configuration					
Azalia			Auto		→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

Azalia

Control Detection of the Azalia device.
Disabled = Azalia will be unconditionally be disabled.
Enabled = Azalia will be unconditionally be enabled.
Auto = Azalia will be enabled if present, disabled otherwise.

System Agent (SA) Configuration



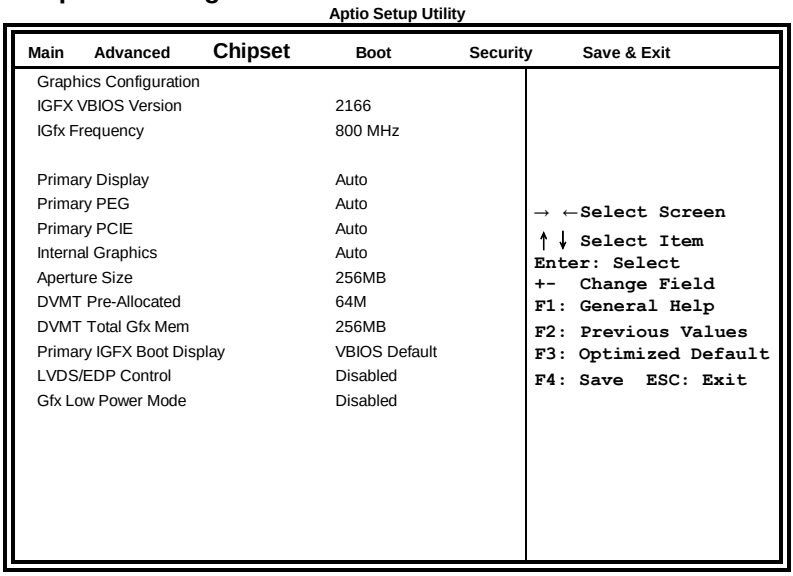
VT-d

Check to enable VT-d function on MCH.

Enable NB CRID

Enable or disable NB CRID WorkAround.

Graphics Configuration



Primary Display

Select which of IGFX/PEG/PCI graphics device should be primary display or select SG for switchable Gfx.

Primary PEG

Select PEGO/PEG1/PEG2/PEG3 Graphics device should be Primary PEG.

Primary PCIE

Select PCIE0/PCIE1/PCIE2/PCIE3/PCIE4/PCIE5/PCIE6PCIE7 Graphics device should be primary PCIE.

Internal Graphics

Keep IGD enabled based on the setup options.

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (Fixed) graphics memory size used by the internal graphics device.

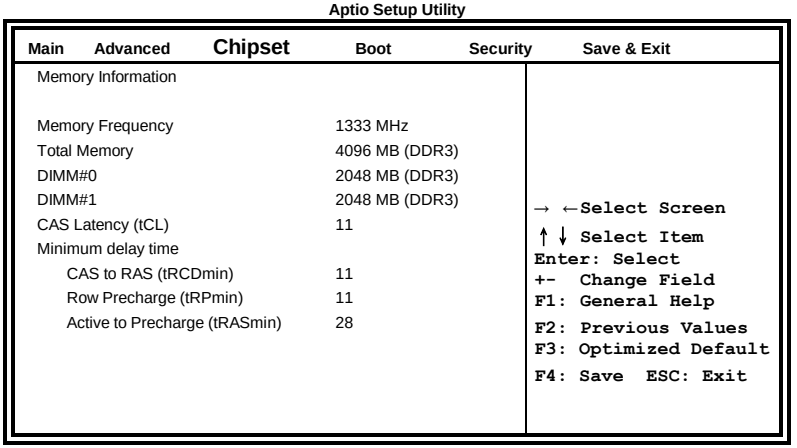
DVMT Total Gfx Mem
Select DVMT 5.0 total graphics memory size used by the internal graphics device.

Primary IGFX Boot Display
Select the Video Device that will be activated during POST. This has no effect if external graphics present. Secondary booty display selection will appear based on your selection. VGA modes will be supported only on primary display.

LVDS/EDP Control
LVDS/EDP Control

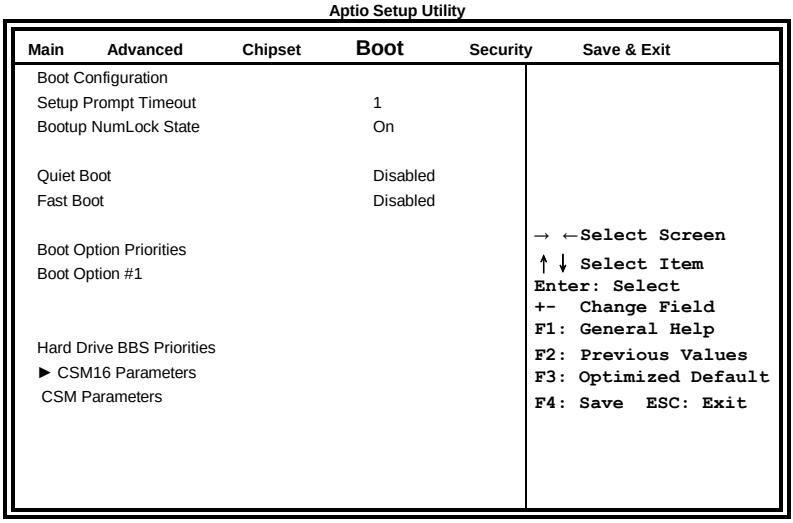
Gfx Low Power Mode
This option is applicable for SFF only.

Memory Configuration



Boot Settings

This section allows you to configure the boot settings.



Setup Prompt Timeout

Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables/Disables Quiet Boot option.

Fast Boot

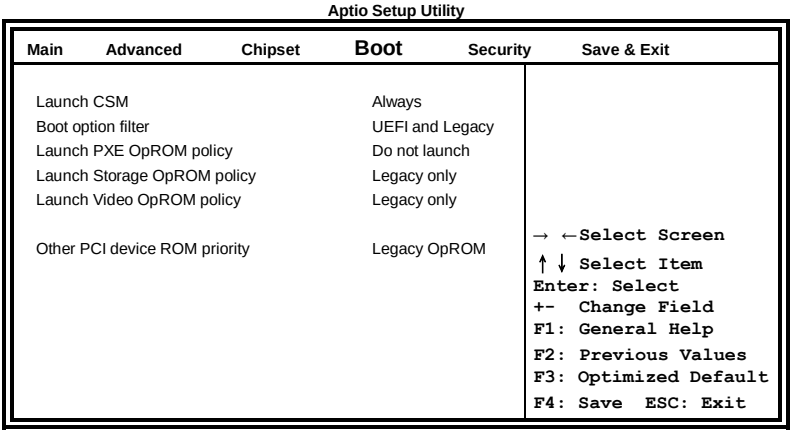
Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Boot Option Priorities

Sets the system boot order.

CSM parameters

This section allows you to configure the boot settings.



Boot Option Filter

This option controls what devices system can boot to.

Launch PXE OpROM Policy

Controls the execution of UEFI and Legacy PXE OpROM.

Launch Storatge OpROM Policy

Controls the execution of UEFI and Legacy Storage OpROM.

Launch Video OpROM Policy

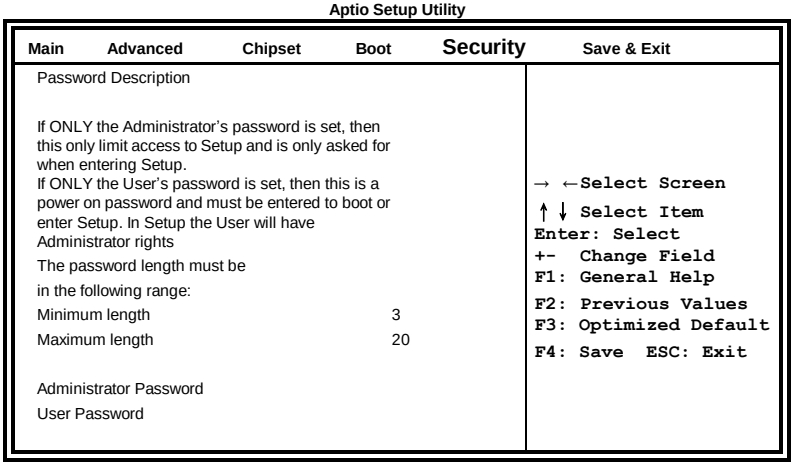
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI Device ROM Priority

For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



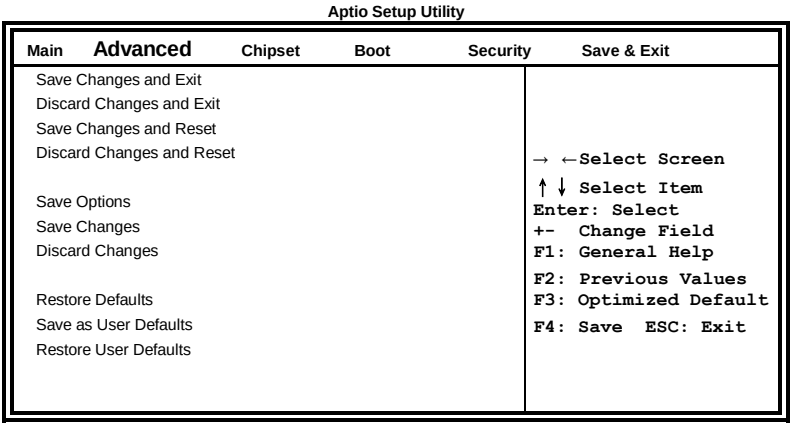
Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings



Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

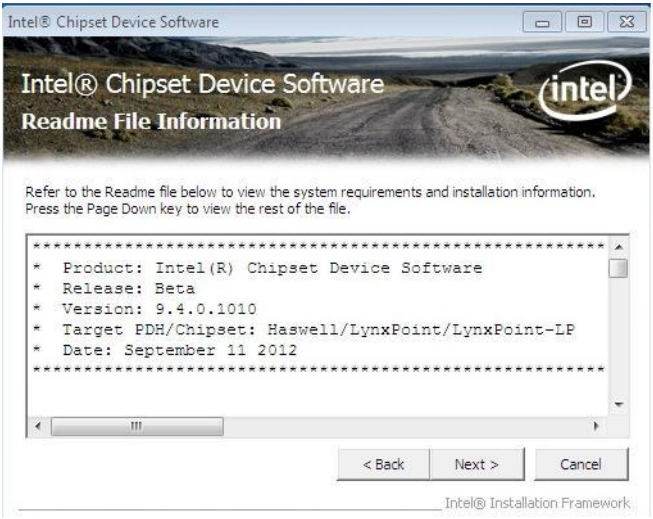
1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Intel(R) Chipset Software Installation Utility.***

3. When the Welcome screen to the Intel® Chipset Device Software appears, click ***Next*** to continue.

4. Click ***Yes*** to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click ***Next*** to continue the installation.



6. The Setup process is now complete. Click ***Finish*** to restart the computer and for changes to take effect.

VGA Drivers Installation

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

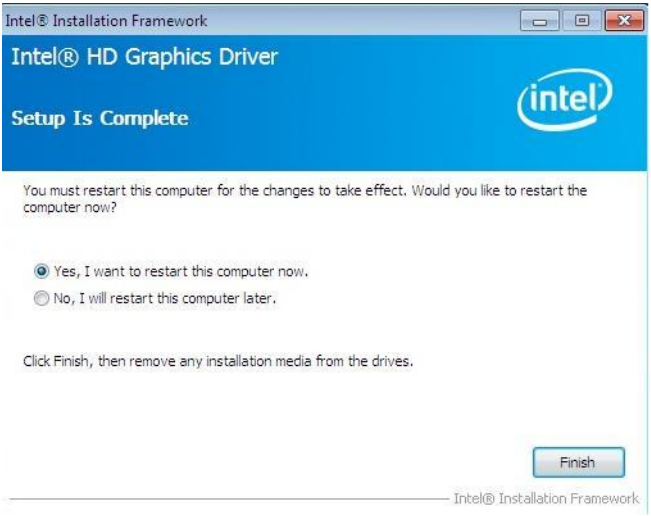
2. Click ***Intel(R) Core(TM) i3/i5/i7 Graphics Driver.***

3. When the Welcome screen appears, click ***Next*** to continue.

4. Click ***Yes*** to to agree with the license agreement and continue the installation.

5. On the screen shown below, click ***Install*** to continue.

6. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

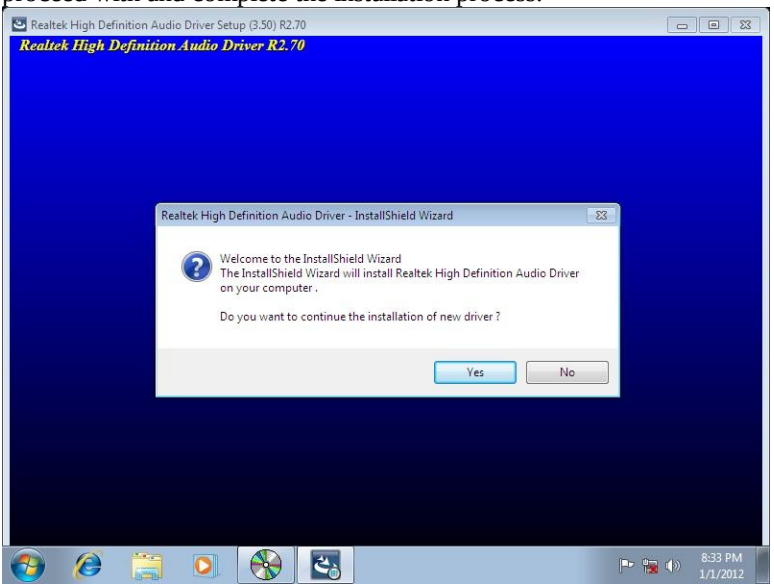


Realtek HD Audio Driver Installation

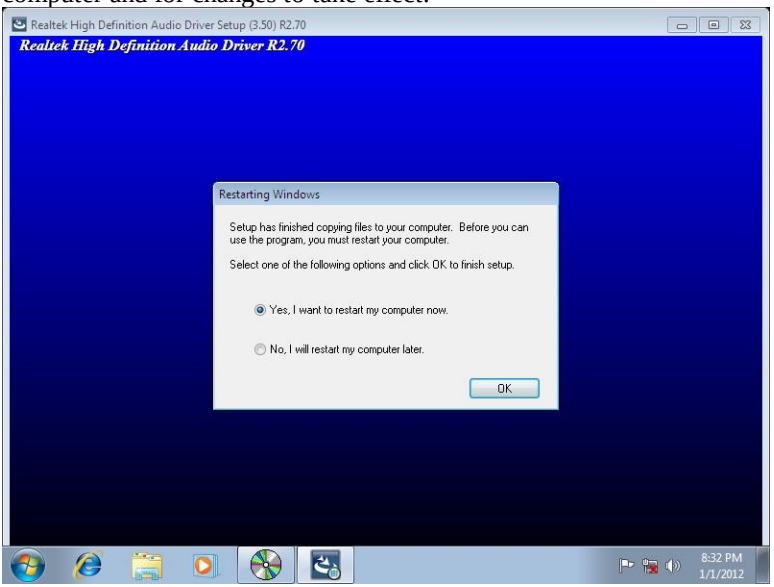
1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Realtek High Definition Audio Driver.***

3. On the Welcome to the InstallShield Wizard screen, click ***Yes*** to proceed with and complete the installation process.

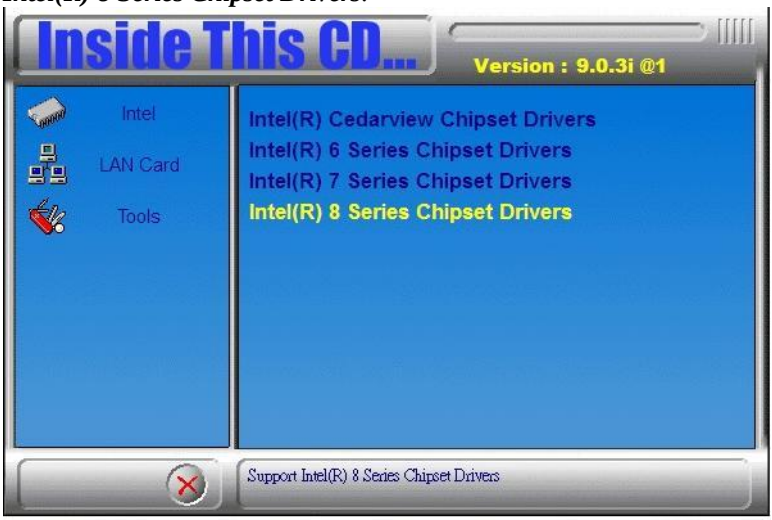


4. The InstallShield Wizard Complete. Click ***Finish*** to restart the computer and for changes to take effect.



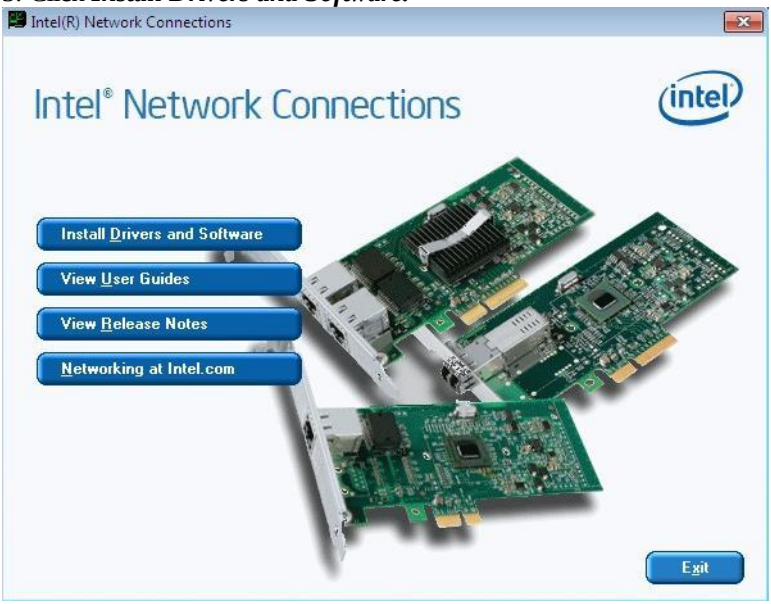
LAN Drivers Installation

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.



2. Click ***Intel(R) PRO LAN Network Driver.***

3. Click ***Install Drivers and Software.***

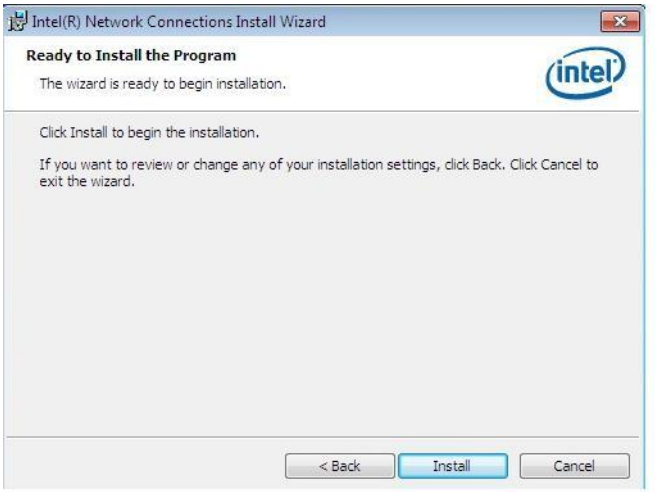


4. When the Welcome screen appears, click ***Next***.

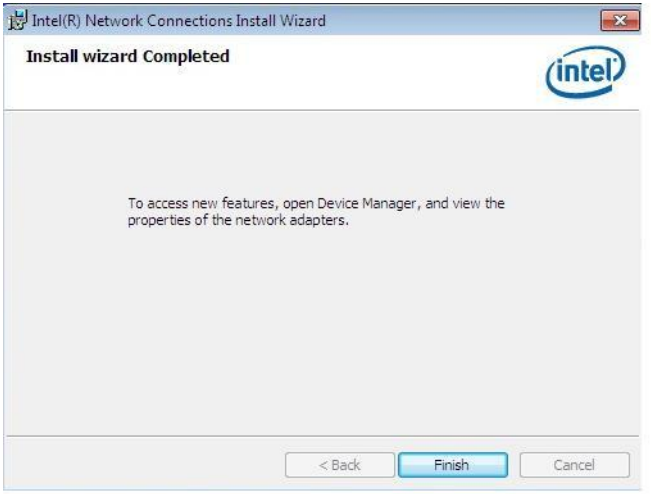
5. Click ***Next*** to to agree with the license agreement.

6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.

7. The wizard is ready to begin installation. Click ***Install*** to begin the installation.



8. When InstallShield Wizard is complete, click ***Finish***.



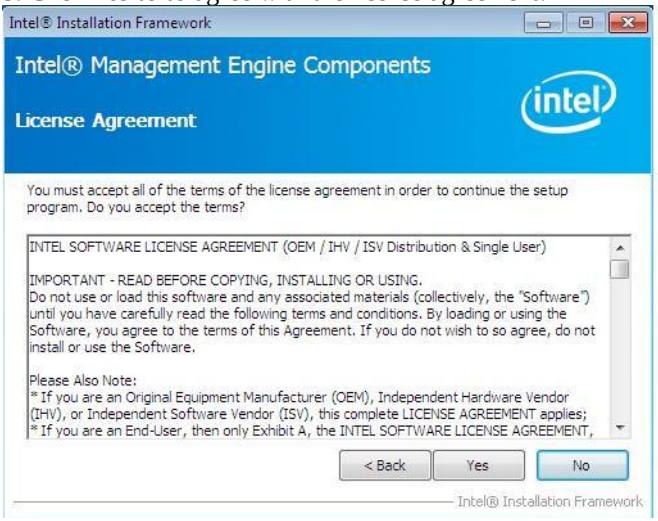
Intel® Management Engine Interface

Follow the steps below to install the Intel Management Engine.

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers*** and then ***Intel(R) AMT 9.0 Drivers***.

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click ***Next***.

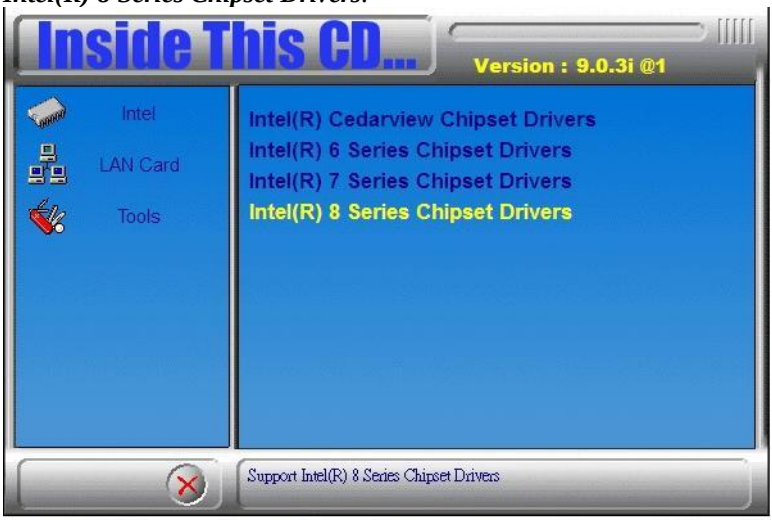
3. Click ***Yes*** to to agree with the license agreement.



4. When the Setup Progress screen appears, click ***Next***. Then, click ***Finish*** when the setup progress has been successfully installed.

Intel® USB 3.0 Drivers

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.



2. Click ***Intel(R) USB 3.0 Drivers.***

3. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click ***Next***.

4. Click ***Yes*** to to agree with the license agreement and continue the installation.

5. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

6. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
2F8h - 2FFh	Serial Port #2(COM2)
2B0h- 2DFh	Graphics adapter Controller
360h - 36Fh	Network Ports
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ8	Real Time Clock
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81866 watch dog program\n");

        SIO = Init_F81866();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81866, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime); }
        else
        {       DisableWDT();           }

        return 0;
```

```
}
//---------------------------------------------------------------------------
void EnableWDT(int interval)
{
	unsigned char bBuf;

	bBuf = Get_F81866_Reg(0x2B);
	bBuf &= (~0x20);
	Set_F81866_Reg(0x2B, bBuf);			//Enable WDTO

	Set_F81866_LD(0x07);				//switch to logic device 7
	Set_F81866_Reg(0x30, 0x01);			//enable timer

	bBuf = Get_F81866_Reg(0xF5);
	bBuf &= (~0x0F);
	bBuf |= 0x52;
	Set_F81866_Reg(0xF5, bBuf);			//count mode is second

	Set_F81866_Reg(0xF6, interval);		//set timer

	bBuf = Get_F81866_Reg(0xFA);
	bBuf |= 0x01;
	Set_F81866_Reg(0xFA, bBuf);			//enable WDTO output

	bBuf = Get_F81866_Reg(0xF5);
	bBuf |= 0x20;
	Set_F81866_Reg(0xF5, bBuf);			//start counting
}
//---------------------------------------------------------------------------
void DisableWDT(void)
{
	unsigned char bBuf;

	Set_F81866_LD(0x07);				//switch to logic device 7

	bBuf = Get_F81866_Reg(0xFA);
	bBuf &= ~0x01;
	Set_F81866_Reg(0xFA, bBuf);			//disable WDTO output

	bBuf = Get_F81866_Reg(0xF5);
	bBuf &= ~0x20;
	bBuf |= 0x40;
	Set_F81866_Reg(0xF5, bBuf);			//disable WDT
}
//---------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81866.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81866_BASE;
void Unlock_F81866 (void);
void Lock_F81866 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81866(void)
{
	unsigned int result;
	unsigned char ucDid;

	F81866_BASE = 0x4E;
	result = F81866_BASE;

	ucDid = Get_F81866_Reg(0x20);
	if (ucDid == 0x07)                                  //Fintek 81866
	{	goto Init_Finish;	}

	F81866_BASE = 0x2E;
	result = F81866_BASE;

	ucDid = Get_F81866_Reg(0x20);
	if (ucDid == 0x07)                                  //Fintek 81866
	{	goto Init_Finish;	}

	F81866_BASE = 0x00;
	result = F81866_BASE;

Init_Finish:
	return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81866 (void)
{
	outportb(F81866_INDEX_PORT, F81866_UNLOCK);
	outportb(F81866_INDEX_PORT, F81866_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81866 (void)
{
	outportb(F81866_INDEX_PORT, F81866_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81866_LD( unsigned char LD)
{
	Unlock_F81866();
	outportb(F81866_INDEX_PORT, F81866_REG_LD);
	outportb(F81866_DATA_PORT, LD);
	Lock_F81866();
}
//---------------------------------------------------------------------------
void Set_F81866_Reg( unsigned char REG, unsigned char DATA)
{
	Unlock_F81866();
	outportb(F81866_INDEX_PORT, REG);
	outportb(F81866_DATA_PORT, DATA);
	Lock_F81866();
}
//---------------------------------------------------------------------------
```

```
unsigned char Get_F81866_Reg(unsigned char REG)
{
	unsigned char Result;
	Unlock_F81866();
	outportb(F81866_INDEX_PORT, REG);
	Result = inportb(F81866_DATA_PORT);
	Lock_F81866();
	return Result;
}
//-----------------------------------------------------------------------------
```

```
//-----------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----------------------------------------------------------------------------
#ifndef __F81866_H
#define __F81866_H                     1
//-----------------------------------------------------------------------------
#define		F81866_INDEX_PORT		(F81866_BASE)
#define		F81866_DATA_PORT		(F81866_BASE+1)
//-----------------------------------------------------------------------------
#define		F81866_REG_LD			0x07
//-----------------------------------------------------------------------------
#define F81866_UNLOCK			0x87
#define		F81866_LOCK				0xAA
//-----------------------------------------------------------------------------
unsigned int Init_F81866(void);
void Set_F81866_LD( unsigned char);
void Set_F81866_Reg( unsigned char, unsigned char);
unsigned char Get_F81866_Reg( unsigned char);
//-----------------------------------------------------------------------------
#endif  //__F81866_H
```