MB961 Series

**Intel 2nd Gen. Core™ i Desktop CPU
+ H61/Q67
Sugar Bay based Micro ATX MB**

USER'S MANUAL

Version 1.0

Acknowledgments

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Introduction

Product Description

The MB961 Series Micro ATX motherboard is based on the latest Intel®
H61/Q67 Express chipset. The platform supports 2nd generation Intel®
Core™ processor family with LGA1155 packing and features an
integrated dual-channel DDR3 memory controller as well as a graphics
core.

The latest Intel processors provide advanced performance in both
computing and graphics quality. The MB961 Series board utilizes the
dramatic increase in performance provided by this Intel's latest
cutting-edge technology. This meets the requirement of customers in the
gaming, POS, digital signage and server market segment.

Measuring 244mm x 244mm, the MB961 Series offers 3Gbps/6Gbps
SATA support, USB3.0 (2 ports) and interfaces for DVI-I, HDMI and
LVDS displays.

MB961 Series FEATURES:

- Supports Intel 2nd Generation Core i7/i5/i3 QC/DC desktop
  processors
- Two DDR3 DIMM, 1066/1333MHz; supports up to 16GB memory
- One Intel PCI-Express Gigabit LAN and one Realtek PCI-Express
  Gigabit LAN
- Integrated Graphics for DVI-I and HDMI (MB961F/MB961RF only)
  displays
- Support LVDS 24 bit dual channel for MB961F/MB961RF only
- 4x SATA 2.0 for MB961/MB961F, 2x SATA 2.0 and 2x SATA 3.0
  for MB961RF, 10x USB 2.0, 2x USB 3.0 for MB961/MB961F, 12x
  USB, 2.0, 2x USB 3.0 for MB961RF
- 4x COM, Watchdog timer
- Supports LPT port for MB961 only
- 1x PCI-E (x16), 1x PCI-E (x8) Slot (MB961/MB961F only supports
  PCIE x1 lane, MB961RF supports PCIE x1 lane or PCIE x4 lanes)

Checklist

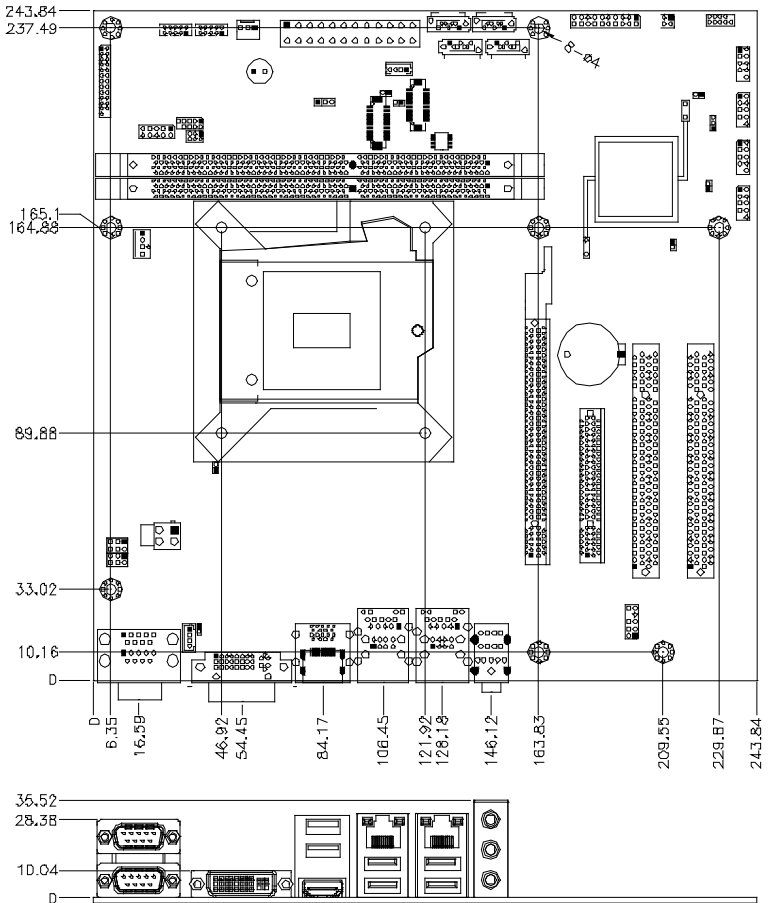Your MB961 Series package should include the items listed below.

- The MB961 Series motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Serial ATA cable

MB961 Series Specifications

Product Name	MB961RF (Q67 based) MB961F (H61 based) MB961 (H61 based)
Form Factor	Micro ATX
CPU Type	Intel® 2nd generation Core™ i7/i5/i3/Pentium®/Celeron® DT processor TDP for QC= 95W/65W/45W;DC= 65W/35W [Package = FC-LGA10, 37.5 mm x 37.5mm]
CPU Speed	Up to 3.40 GHz
Cache Size	Up to 8MB shared L2 Cache
CPU Socket	LGA1155 (Socket H2)
Chipset	Intel® BD82H61 PCH for MB961/MB961F (TDP=6.1W) or BD82Q67 PCH for MB961RF [27mm x 27mm, 942-pin FCBGA package]
BIOS	AMI BIOS, support ACPI Function
Memory	Intel® 2nd generation Core™ I7/I5/I3/Pentium®/Celeron® DT processor integrated memory controller support DDR3-1600 (Non-ECC) UDIMM x **2**, Max. 16GB
VGA	Intel® 2nd generation Core™ i7/i5/i3/Pentium® DT processor integrated Gfx(HD2000/HD3000) ● DVI-**I** x 1(thru Level shifter ASM1442) ● HDMI x 1 for MB961F/MB961RF only ● LVDS (thru CH7511 via DP) for MB961F/MB961RF only
LAN	Intel 82579V PCIe Gigabit LAN PHY x 1 Realtek RTL8111E PCIe Gigabit LAN controller x1
USB	USB 2.0 host controller, supports 10/12 ports - **4** ports in the rear panel. - **6** ports for onboard pin header (MB961/MB961F) or **8** ports for onboard pin header (MB961RF) USB 3.0 host controller (ASM1042), support 2 ports - **2** ports in the rear panel
Serial ATA	Intel® H61/Q67 PCH build-in SATA controller, Supports **4** ports x SATA 2.0 from H61 PCH (MB961/MB961F) Supports **2** ports x SATA 3.0 + **2** ports x SATA 2.0 from Q67 PCH (MB961RF)
Audio	Intel® H61/Q67 PCH built-in High Definition Audio controller: ALC892 w/ 7.1 channels
LPC I/O	Fintek F81866AD-I COM1 (RS232/422/485) [Auto flow control/ Jumper less selection]; COM2~4 (RS232 only) COM1/2 with pin-9 with power for 2 ports (500 mA each) Hardware Monitor (2 thermal inputs, 4 voltage monitor inputs & **2** Fan headers) CPU Fan = 4-pin type (PWM); SYS Fan= 3-pin type (DC) LPT port (MB961 only)
Digital IO	4 in & 4 out

Expansion Slots	PCIe (16x) x1 PCIe (8x) x1 ==**Actual signal will be PCIe(4x) for MB961RF or PCIe(1x) for MB961/MB961F**== PCI x 2 [Thru ITE8893 PCIe to PCI converter]
Edge Connector	Dual DB9 stack connector for COM #1, #2 DVI-**I** connector x1 Dual USB (3.0) stack connector x1 HDMI x1 (for MB961F/MB961RF only) RJ-45 GbE + dual USB (2.0) stack connector x2 RCA Jack 3x1 for HD Audio
Onboard Header/Connector	**-4** ports x SATA II (MB961/MB961F) **or 2 ports x SATA II + 2 ports x SATA III (MB961RF)** -2x5 pin-header x 3 for 6 ports USB 2.0 **(MB961/MB961F)** **or 2x5 pin-header x4 for 8 ports USB 2.0 (MB961RF)** -2x5 pin-header x 1 for front panel audio -DF11-10 box header x1 for COM3 -DF11-10 box header x1 for COM4 -2x5 pins pin-header x1 for Digital I/O **-2x13 pin-header x1 for LPT (MB961)** -2x5 pins male connector [for debugging purpose] -2x10 pins pin-header x 1 for front panel indicators+2x2 pins pin header for ACPI LED (For MB961) **-DF13-20pin x2 for 24-bit dual channel LVDS (MB961F/MB961RF)** **4-pin JST header [pitch=2.5] for brightness control (MB961F /MB961RF)**
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
System Voltage	+5V, +3.3V, +12V, -12V, 5VSB (2A) 24-pin ATX main power + 4-pin 12V
Other	- iSMART controller [EuP/ErP ; Auto-scheduler ; Power resume] - **ACPI LED function (MB961 only)** - **RAID function (MI961RF only)**
RoHS	Yes
Board Size	244mm x 244mm

Board Dimensions

Installations

This section provides information on how to use the jumpers and connectors on the MB961 Series in order to set up a workable system. The topics covered are:

Installing the CPU

The MB961 Series board supports an LGA1155 Socket (shown below) for Intel Sandy Bridge processors.

To install the CPU, unlock first the socket by pressing the lever sideways, then lift it up to a 90-degree. Then, position the CPU above the socket such that the CPU corner aligns with the gold triangle matching the socket corner with a small triangle. Carefully insert the CPU into the socket and push down the lever to secure the CPU. Then, install the heat sink and fan.
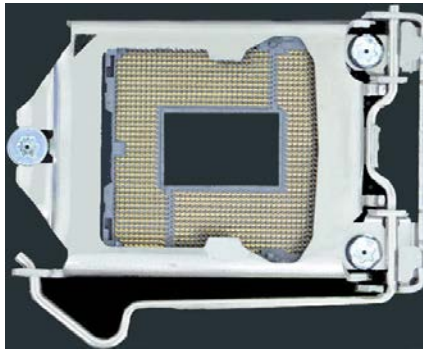
NOTE: *Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

Installing the Memory

The MB961 Series board supports four DDR3 memory socket for a maximum total memory of 16GB in DDR3 DIMM memory type.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.

2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.

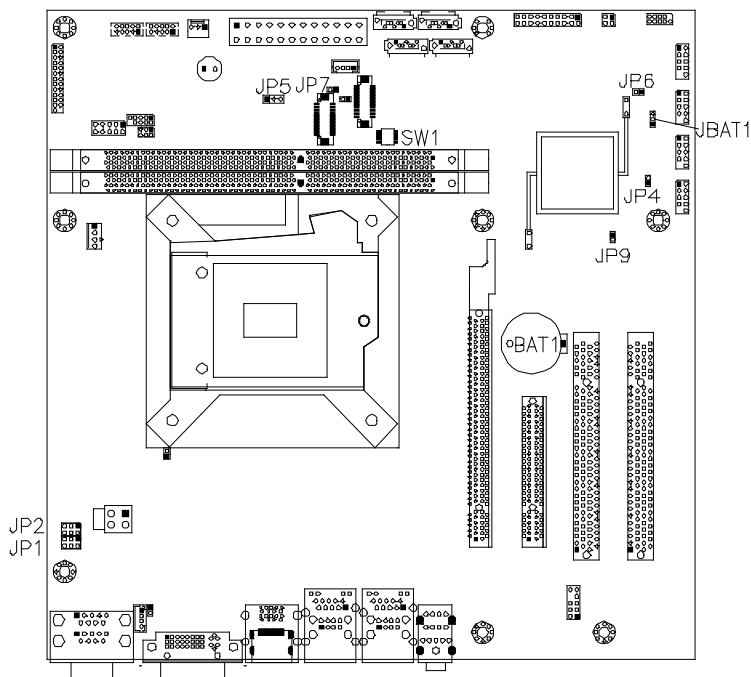3. To remove the DDR3 module, press the clips with both hands.
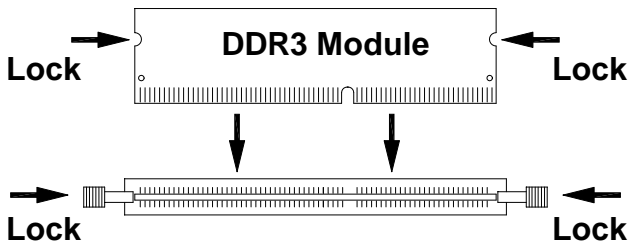
Setting the Jumpers

Jumpers are used on MB961 Series to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on MB961 Series and their respective functions.

Jumper Locations on MB961 Series

JP1: COM1 RS232 RI/+5V/+12V Power Setting
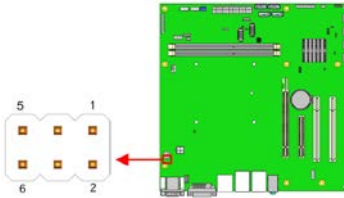
JP1	Setting	Function
	Pin 1-3 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 3-5 Short/Closed	+5V

JP2: COM2 RS232 RI/+5V/+12V Power Setting
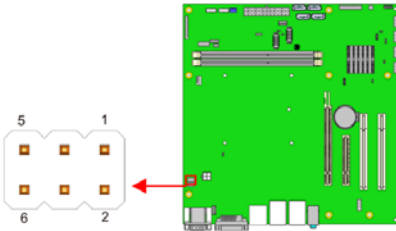
JP2	Setting	Function
	Pin 1-3 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 3-5 Short/Closed	+5V

JP4: Flash Descriptor Security Override (Factory use only)
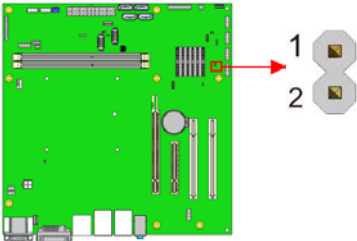
JP4	Flash Descriptor Security Override
Open	Disabled (Default)
Close	Enabled

JP5: LCD Panel Power Selection (MB961F/MB961RF only)
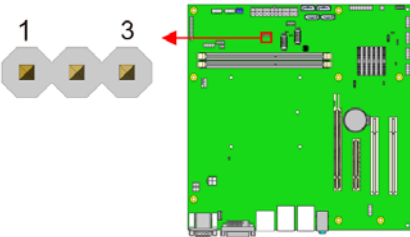
JP5	LCD Panel Power
	+3.3V*
	+5V

JP6: Factory use only (Default: open)
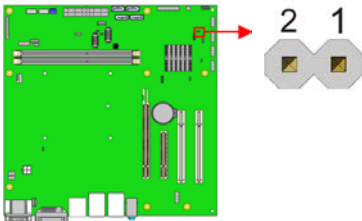
JP7: LCD Brightness +3.3V/+5V Power Setting
(MB961F/MB961RF only)
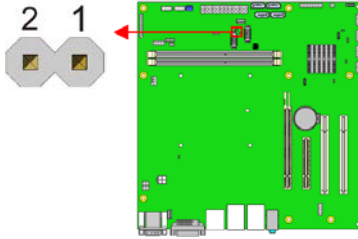
JP7	Setting
□ □ 1 2	+3.3V*
□ □ 1 2	+5V

JBAT1: Clear CMOS Contents
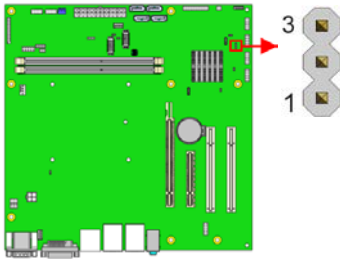
JBAT1	Setting	Function
□ □ □ 1 2 3	Pin 1-2 Short/Closed	Normal
□ □ □ 1 2 3	Pin 2-3 Short/Closed	Clear CMOS

JP9: LVDS function select
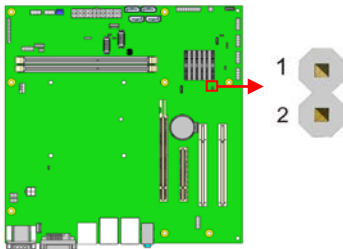
JP9	LVDS function select
Open	Disabled
Close	Enabled (Default)

SW1: Panel Type Selection
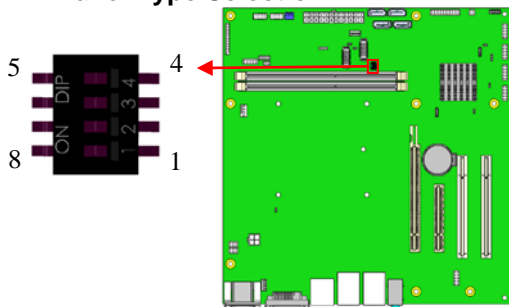
(Default: Pin 4,3,2,1 (ON ON ON OFF))
(MB961F/MB961RF only)

SW1-4	SW1-3	SW1-2	SW1-1	Panel Type
ON	ON	ON	ON	800*600 18bit 1ch
ON	ON	ON	OFF	1024*768 18bit 1ch *
ON	ON	OFF	ON	1024*768 24bit 1ch
ON	ON	OFF	OFF	1280*768 18bit 1ch
ON	OFF	ON	ON	1280*800 18bit 1ch
ON	OFF	ON	OFF	1280*960 18bit 1ch
ON	OFF	OFF	ON	1280*1024 24bit 2ch
ON	OFF	OFF	OFF	1366*768 18bit 1ch
OFF	ON	ON	ON	1366*768 24bit 1ch
OFF	ON	ON	OFF	1440*900 24bit 2ch
OFF	ON	OFF	ON	1440*1050 24bit 2ch
OFF	ON	OFF	OFF	1600*900 24bit 2ch
OFF	OFF	ON	ON	1680*1050 24bit 2ch
OFF	OFF	ON	OFF	1600*1200 24bit 2ch
OFF	OFF	OFF	ON	1920*1080 24bit 2ch
OFF	OFF	OFF	OFF	1920*1200 24bit 2ch

Connectors on MB961Series

Connector Locations on MB961 Series

CN3: COM1 and COM2 Serial Ports
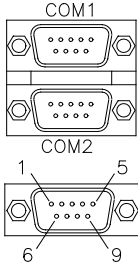
Pin #	Signal Name		
	RS-232	**R2-422**	**RS-485**
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC
10	NC	NC	NC

CN1: DVI-I Connector
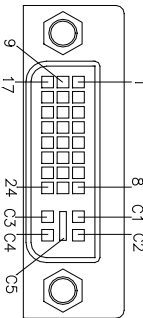
Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	Hot_ Plug_Detect
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
CRT_VSYNC	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	CRT_R
SHIELD 1/3	11	C2	CRT_G
DATA 3-	12	C3	CRT_B
DATA 3+	13	C4	CRT_HSYNC
DDC POWER	14	C5	A GROUND2
A GROUND 1	15	C6	A GROUND3
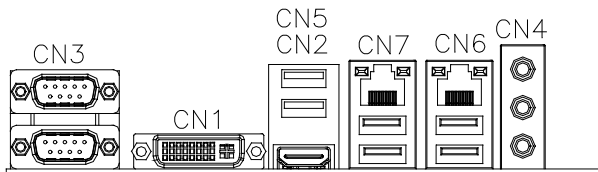
CN5: USB3.0 Connector

CN2: HDMI Connector (*MB961F/MB961RF only*)

CN7: Intel Gigabit LAN + USB 10/11

CN6: Realtek Gigabit LAN + USB 2/3

CN4: HD Audio Connector

CN8: LCD Backlight Connector (*MB961F/MB961RF only*)
1X4_2.0mm_Straight_M (JST B4B-PH-K-S)
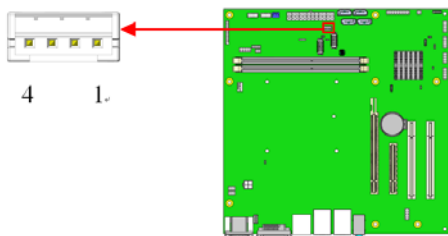
Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Brightness Control
4	Ground

CN9, CN11: SATA2 Connectors
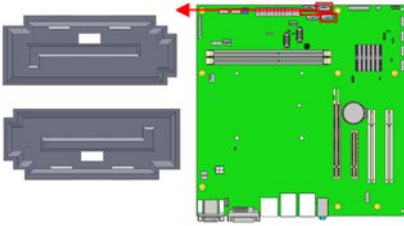
CN10, CN12: SATA2 or SATA3 Connectors
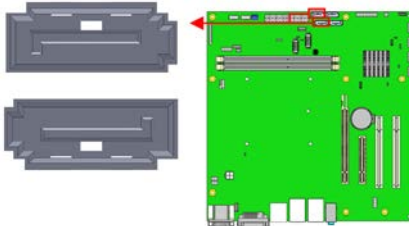
MB961 supports SATA2 (3Gbps)
MB961F supports SATA2 (3Gbps) and SATA3 (6Gbps)

CH1, CH2: LVDS Connectors (1st channel, 2nd channel)
(For *MB961F/MB961RF only*)
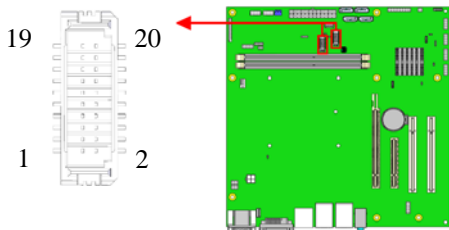
Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
+5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC-	16	15	TXC+
+5V/3.3V	18	17	ENABKL
NC	20	19	NC

J1: MCU JTAG (for debug use)
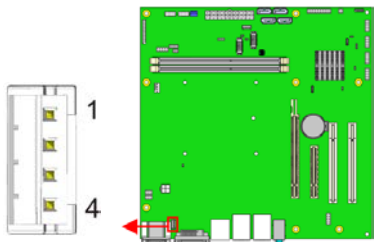
J3: Audio Pin Header for Chassis Front Panel
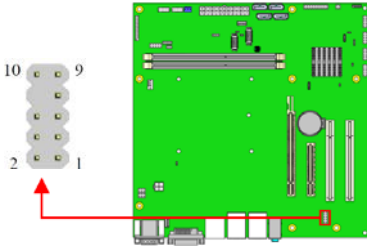
Signal Name	Pin #	Pin #	Signal Name
MIC IN_L	1	2	Ground
MIC IN_R	3	4	DET
LINE_R	5	6	Ground
Sense	7	8	KEY
LINE_L	9	10	Ground

J4: ATX 12V Power Connector
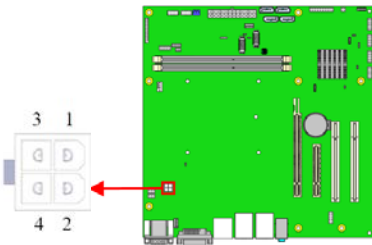
Pin #	Signal Name
1	Ground
2	Ground
3	+12V
4	+12V

J5, J9, J12, J14: USB Connectors
(*J12 is supported by MB961RF only*)
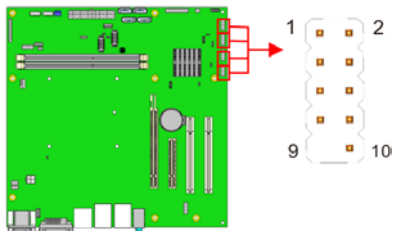
Signal Name	Pin #	Pin #	Signal Name
VCC	1	2	VCC
D0-	3	4	D1-
D0+	5	6	D1+
GND	7	8	GND
KEY	9	10	NC

J6, J8, DDR3 DIMM Sockets
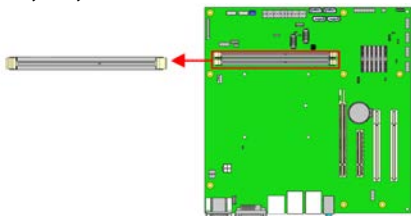
J10: Digital I/O
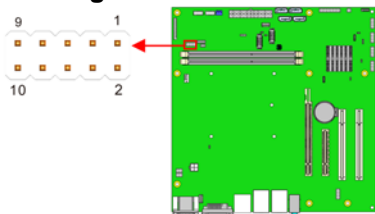
Signal Name	Pin #	Pin #	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J11: LPC Connector (for debug use)
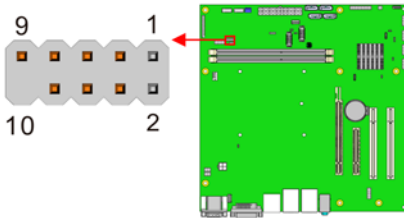
J13: Parallel Port Connector (*MB961 only*)
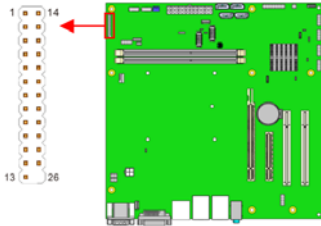
Signal Name	Pin #	Pin #	Signal Name
Line printer strobe	1	14	Auto Feed
PD0, parallel data 0	2	15	Error
PD1, parallel data 1	3	16	Initialize
PD2, parallel data 2	4	17	Select
PD3, parallel data 3	5	18	Ground
PD4, parallel data 4	6	19	Ground
PD5, parallel data 5	7	20	Ground
PD6, parallel data 6	8	21	Ground
PD7, parallel data 7	9	22	Ground
ACK, acknowledge	10	23	Ground
Busy	11	24	Ground
Paper empty	12	25	Ground
Select	13	26	N/A

J16, J17: COM3, COM4 RS232 Serial Ports
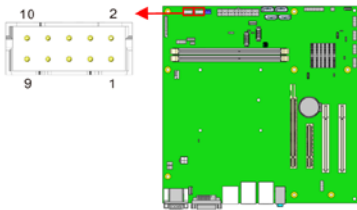
Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	2	RXD, Receive data
TXD, Transmit data	3	4	DTR, Data terminal ready
GND, ground	5	6	DSR, Data set ready
RTS, Request to send	7	8	CTS, Clear to send
RI, Ring indicator	9	10	Not Used

J15: 24-pin ATX Power Connector
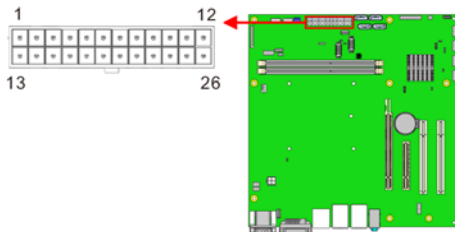
Signal Name	Pin #	Pin #	Signal Name
3.3V	13	1	3.3V
-12V	14	2	3.3V
Ground	15	3	Ground
PS-ON	16	4	+5V
Ground	17	5	Ground
Ground	18	6	+5V
Ground	19	7	Ground
-5V	20	8	Power good
+5V	21	9	5VSB
+5V	22	10	+12V
+5V	23	11	+12V
Ground	24	12	+3.3V

J18: ACPI LED Connector (*MB961 only*)
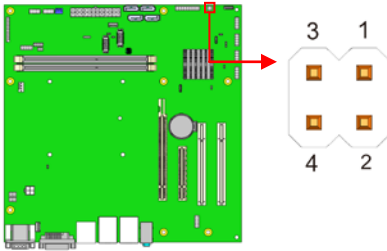
Pin #	Signal Name
1	S1/S3 LED+
2	Ground
3	S0 LED+
4	Ground

J19: Front Panel Function Connector
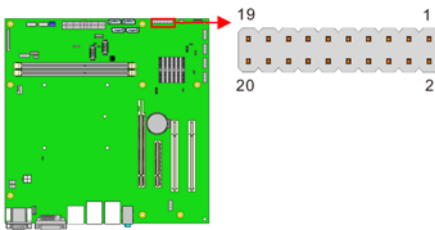
Signal Name	Pin #	Pin #	Signal Name
SPK -	1	2	PWR LED +
NC	3	4	NC
GND	5	6	PWR LED- (GND)
SPK +(+5V)	7	8	NC
NC	9	10	GND
NC	11	12	GND
PWR_SW	13	14	PWR_SW
NC	15	16	NC
RST+	17	18	RST-(GND)
HDD LED -	19	20	HDD LED +

J20: SPI Connector (For debug use)
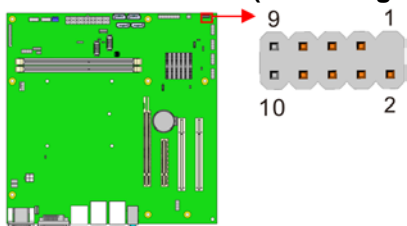
J21: LPC signal connector
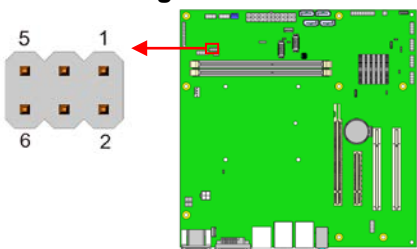
Signal Name	Pin	Pin	Signal Name
-SUSTAT	1	2	3VDUAL
SERIRQ	3	4	NC
GPIO	5	6	Ground

CPU_FAN1: CPU Fan Power Connector
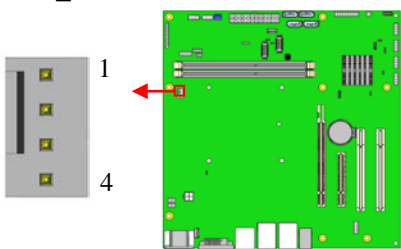
Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Control

SYS_FAN1: System Fan1 Power Connector
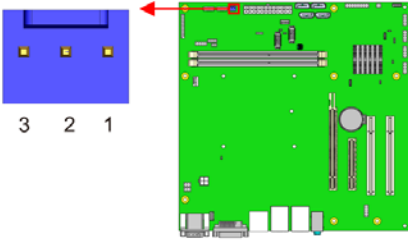
Pin #	Signal Name
1	Ground
2	+12V(MAX. 500mA)
3	Rotation detection

PCIE1: PCIE x8 Slot
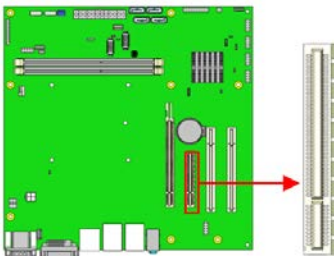
MB961/MB961F support PCIE x1 only
MB961RF supports PCIE x1 or PCIE x4

PCIE2: PCI-E X16 Slot
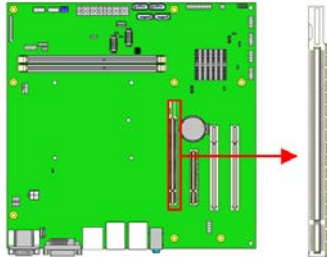
PCI3, PCI4: PCI Slot
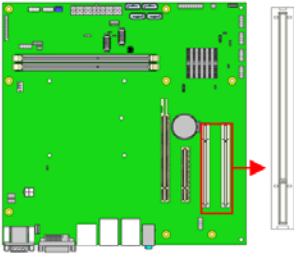
BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

```
Press <DEL> to Enter Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

Main Settings

Main	Advanced	Chipset	Boot	Security	Save & Exit

BIOS Information		Choose the system default language
System Language	[English]	→ ←**Select Screen**
System Date	[Tue 01/20/2009]	↑ ↓ **Select Item**
Access Level	Administrator	**Enter: Select**
		+- Change Field
		F1: General Help
		F2: Previous Values
		F3: Optimized Default
		F4: Save ESC: Exit

System Language
Choose the system default language.

System Date
Set the Date. Use Tab to switch between Data elements.

System Time
Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

▶ PCI Subsystem Settings
▶ ACPI Settings
▶ Wake up event setting
▶ Trusted Computing
▶ CPU Configuration
▶ SATA Configuration
▶ Shutdown Temperature Configuration
▶ iSmart Controller
▶ USB Configuration
▶ F81866 Super IO Configuration
▶ F81866 H/W Monitor
▶ CPU PPM Configuration

```
→ ←Select Screen
↑↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

PCI Subsystem Settings

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

PCI Bus Driver Version | V 2.0502

PCI 64bit Resources Handing
Above 4G Decoding | Disabled

PCI Common Settings
PCI Latency Timer | 32 PCI Bus Clocks
VGA Palette Snoop | Disabled
PERR# Generation | Disabled
SERR# Generation | Disabled

▶ PCI Express Settings

```
→ ←Select Screen
↑↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

Above 4G Decoding

Enables or Disables 64bit capable devices to be decoded in above 4G address space (only if system supports 64 bit PCI decoding).

PCI Latency Timer
Value to be programmed into PCI Latency Timer Register.

VGA Palette Snoop
Enables or disables VGA Palette Registers Snooping.

PERR# Generation
Enables or disables PCI device to generate PERR#.

SERR# Generation
Enables or disables PCI device to generate SERR#.

PCI Express Settings
Change PCI Express devices settings.

PCI Express Settings

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

PCI Express Device Register Settings	
Relaxed Ordering	Disabled
Extended Tag	Disabled
No Snoop	Enabled
Maximum Payload	Auto
Maximum Read Request	Auto
PCI Express Link Register Settings	
ASPM Support	Disabled
WARNING: Enabling ASPM may cause	Disabled
PCI-E devices to fail	
Extended Synch	Disabled
Link Training Retry	5
Link Training Timeout (uS)	100
Unpopulated Links	Keep Link ON

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-   Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

Relaxed Ordering
Enables or disables PCI Express Device Relaxed Ordering.

Extended Tag
If ENABLED allows device to use 8-bit Tag field as a requester.

No Snoop
Enables or disables PCI Express Device No Snoop option.

Maximum Payload

Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Maximum Read Request

Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support

Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

Extended Synch

If ENABLED allows generation of Extended Synchronization patterns.

Link Training Retry

Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Link Training Timeout (uS)

Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

Unpopulated Links

In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

ACPI Settings

Main	**Advanced**	**Chipset**	**Boot**	**Security**	**Save & Exit**

ACPI Settings	
	→ ←**Select Screen**
Enable Hibernation Enabled	↑↓ **Select Item**
ACPI Sleep State S1 (Suspend to R…)	**Enter: Select**
Lock Legacy Resources Disabled	**+- Change Field**
S3 Video Repost Disabled	**F1: General Help**
	F2: Previous Values
	F3: Optimized Default
	F4: Save ESC: Exit

Enable Hibernation
Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State
Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

Lock Legacy Resources
Enabled or Disabled Lock of Legacy Resources.

S3 Video Repost
Enable or disable S3 Video Repost.

Wake up event settings

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
Wake system with Fixed Time			Disabled		
Wake up hour			0		
Wake up minute			0		
Wake up second			0		
					→ ←Select Screen
Wake on Ring			Enabled		↑↓ Select Item
Wake on PCI PME			Enabled		Enter: Select
Wake on PCIE Wake Event			Enabled		+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

Wake system with Fixed Time

Enables or Disables System wake on alarm event. When enabled, System will wake on the hr::min:: sec specified.

Wake on PCIE PME Wake Event

The options are Disabled and Enabled.

CPU Configuration
This section shows the CPU configuration parameters.

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
CPU Configuration					
Intel® Core ™ i7-3770 CPU @ 3.40GHz					
Processor Stepping		306a8			
Microcode Revision		c			
Max CPU Speed		3400 MHz			
Min CPU Speed		1600 MHz			
CPU Speed		3400 MHz			
Processor Cores		4			
Intel HT Technology		Supported			
Intel VT-x Technology		Supported			
Intel SMX Technology		Supported			
64-bit		Supported			
Hyper-threading		Enabled			→ ←Select Screen
Active Processor Cores		All			↑↓ Select Item
Limit CPUID Maximum		Disabled			Enter: Select
Execute Disable Bit		Enabled			+- Change Field
Intel Virtualization Technology		Disabled			F1: General Help
Hardware Prefetcher		Disabled			F2: Previous Values
Adjacent Cache Line Prefetch		Enabled			F3: Optimized Default
					F4: Save ESC: Exit

Hyper-threading
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

Active Processor Cores
Number of cores to enable in each processor package.

Limit CPUID Maximum
Disabled for Windows XP.

Execute Disable Bit
XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Re33dHat Enterprise 3 Update 3.)

Intel Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Hardware Prefetcher

To turn on/off the Mid level Cache (L2) streamer Prefetcher.

Adjacent Cache Line Prefetch

To turn on/off prefetching of adjacent cache lines.

SATA Configuration

SATA Devices Configuration.

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

SATA Controller(s)	Enabled	
SATA Mode Selection	IDE	
SATA Port0	Empty	
Software Preserve	Unknown	
SATA Port1	Empty	→ ←Select Screen
Software Preserve	Unknown	↑↓ Select Item
SATA Port2	Empty	Enter: Select
Software Preserve	Unknown	+- Change Field
SATA Port3	Empty	F1: General Help
Software Preserve	Unknown	F2: Previous Values
SATA Port4	Empty	F3: Optimized Default
Software Preserve	Unknown	F4: Save ESC: Exit
SATA Port5	Empty	
Software Preserve	Unknown	

SATA Controller(s)

Enable / Disable Serial ATA Controller.

SATA Mode Selection

(1) IDE Mode.
(2) AHCI Mode.
(3) RAID Mode.

Shutdown Temperature Configuration

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
APCI Shutdown Temperature			Disabled		→ ←Select Screen
					↑↓ Select Item
					Enter: Select
					+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

ACPI Shutdown Temperature
The default setting is Disabled.

iSmart Controller

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
iSmart Controller					
Power-On after Power failure			Disable		→ ←Select Screen
					↑↓ Select Item
Schedule Slot 1			None		Enter: Select
Schedule Slot 2			None		+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

ISmart Controller
Setup the power on time for the system.

Schedule Slot 1 / 2
Setup the hour/minute for system power on.

USB Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit

USB Configuration

USB Devices:
  2 Hubs

Legacy USB Support	Enabled	
USB3.0 Support	Enabled	
XHCI Hand-off	Enabled	→ ←Select Screen
EHCI Hand-off	Enabled	↑↓ Select Item
Port 60/64 Emulation	Enabled	Enter: Select
		+- Change Field
USB hardware delays and time-outs:		F1: General Help
USB Transfer time-out	20 sec	F2: Previous Values
Device reset tine-out	20 sec	F3: Optimized Default
Device power-up delay	Auto	F4: Save ESC: Exit

Legacy USB Support
Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected.
DISABLE option will keep USB devices available only for EFI
applications.

USB3.0 Support
Enable/Disable USB3.0 (XHCI) Controller support.

XHCI Hand-off
This is a workaround for OSes without XHCI hand-off support. The
XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off

Enabled/Disabled. This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

Port 64/60 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

USB Transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

Device reset tine-out

USB mass Storage device start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

F81866 Super IO Configuration

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

```
Super IO Configuration

                                           →  ←Select Screen
F81866 Super IO Chip          F81866
► Serial Port 0 Configuration              ↑ ↓ Select Item
► Serial Port 1 Configuration             Enter: Select
► Serial Port 2 Configuration             +-   Change Field
► Serial Port 3 Configuration             F1: General Help
                                          F2: Previous Values
► Parallel Port Configuration             F3: Optimized Default
                                          F4: Save  ESC: Exit
```

Serial Port Configuration

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

Parallel Port Configuration

Set Parameters of Parallel Port(LPT/LPTE)

F81866 H/W Monitor

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

PC Health Status

CPU temperature	+41 C
SYS temperature	+35 C
FAN1 Speed	4021RPM
FAN2 Speed	N/A
Vcore	+0.976V
+5V	+5.213 V
+12V	+12.408 V
1.5V	+1.504 V
VSB5V	+4.992 V
VCC3V	+3.392 V

Fan1 smart fan control
Fan2 smart fan control

```
→ ←Select Screen
↑↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

Fan1/Fan2 Smart Fan Control

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

CPU PPM Configuration

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

CPU PPM Configuration

EIST   Enabled
Turbo Mode   Enabled

→ ←Select Screen

↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help

F2: Previous Values
F3: Optimized Default

F4: Save ESC: Exit

EIST
Enable/Disable Intel SpeedStep.

Chipset Settings
This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

► PCH-IO Configuration
► System Agent (SA) Configuration

→ ←Select Screen

↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

PCH-IO Configuration

This section allows you to configure the North Bridge Chipset.

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

```
Intel PCH RC Version            1.5.0.0
Intel PCH SKU Name              H61
Intel PCH Rev ID                O5/B3

► PCI Express Configuration
► USB Configuration
► PCH Azalia Configuration

PCH LAN Controller              Enabled
   Wake on LAN                  Enabled

High Precision Event Timer Configuration
High Precision Timer            Enabled                 → ←    Select Screen
                                                        ↑ ↓  Select Item
SLP_S4 Assertion Width          4-5 Seconds             Enter: Select
                                                        +-  Change Field
                                                        F1: General Help
                                                        F2: Previous Values
                                                        F3: Optimized Default
                                                        F4: Save  ESC: Exit
```

PCH LAN Controller
Enable or disable onboard NIC.

Wake on LAN
Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

SLP_S4 Assertion Width
Select a minimum assertion width of the SLP_S4# signal.

PCI Express Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
PCI Express Configuration					
PCI Express Clock Gating		Enabled			
DMI Link ASPM Control		Enabled			
DMI Link Extended Synch Control		Disabled			
PCIe-USB Glitch W/A		Disabled			
Subtractive Decode		Disabled			
► PCI Express Root Port 1					
► PCI Express Root Port 2					
► PCI Express Root Port 3				→ ←	Select Screen
PCI-E Port 4 is assigned to LAN				↑↓ Select Item	
► PCI Express Root Port 5				Enter: Select	
► PCI Express Root Port 6				+- Change Field	
► PCI Express Root Port 7				F1: General Help	
► PCI Express Root Port 8				F2: Previous Values	
				F3: Optimized Default	
				F4: Save ESC: Exit	

PCI Express Clock Gating
Enable or disable PCI Express Clock Gating for each root port.

DMI Link ASPM Control
The control of Active State Power Management on both NB side and SB side of the DMI link.

PCIe-USB Glitch W/A
PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG port.

USB Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
USB Configuration					
EHCI1			Enabled		
EHCI2			Enabled		
USB Ports Per-Port Disable Control			Disabled		

→ ←   Select Screen
↑↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

EHCI1/2
Control the USAB EHCI (USB 2.0) functions. One EHCI controller must always be enabled.

USB Ports Per-Port Disable Control
Control each of the USB ports (0~13) disabling.

PCH Azalia Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
PCH Azalia Configuration					
Azalia			Auto		
Azalia Docking Support			Disabled		
Azalia PME			Disabled		
Azalia Internal HDMI Code			Disabled		

→ ←   Select Screen
↑↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

Azalia
Control Detection of the Azalia device.
Disabled = Azalia will unconditionally disabled.
Enabled Azalia will be unconditionally enabled.
Auto = Azalia will enabled if present, disabled otherwise.

System Agent (SA) Configuration

Aptio Setup Utility

Main	Advanced	**Chipset**	Boot	Security	Save & Exit
System Agent Bridge Name			IvyBridge		
System Agent RC Version			1.1.0.0		
VT-d Capability			Supported		
VT-d			Enabled		→ ←Select Screen
CHAP Device (B0:D7:F0)			Disabled		
Thermal Device (B0:D4:F0)			Disabled		↑↓ Select Item
Enable NB CRID			Disabled		Enter: Select
BDAT ACPI Table Support			Disabled		+- Change Field
C-State Pre-Wake			Enabled		F1: General Help
					F2: Previous Values
► Graphics Configuration					F3: Optimized Default
► Memory Configuration					F4: Save ESC: Exit

VT-d
Check to enable VT-d function on MCH.

Enable NB CRID
Enable or disable NB CRID WorkAround.

C-State Pre-Wake
Controls C-State Pre-Wake feature for ARAT, in SSKPD[57].

Graphics Configuration

Aptio Setup Utility

Main	Advanced	**Chipset**	Boot	Security	Save & Exit
Graphics Configuration					
IGFX VBIOS Version			2132		
IGfx Frequency			350 MHz		
Primary Display			Auto		
Internal Graphics			Auto		→ ←Select Screen
GTT Size			2MB		↑↓ Select Item
Aperture Size			256MB		Enter: Select
DVMT Pre-Allocated			64M		+- Change Field
DVMT Total Gfx Mode			Disabled		F1: General Help
Gfx Low Power Mode			Disabled		F2: Previous Values
► LCD Control					F3: Optimized Default
					F4: Save ESC: Exit

Primary Display

Select which of IGFX/PEG/PCI graphics device should be primary display or select SG for switchable Gfx.

Internal Graphics

Keep IGD enabled based on the setup options.

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (Fixed) graphics memory size used by the internal graphics device.

DVMT Total Gfx Mem

Select DVMT 5.0 total graphics memory size used by the internal graphics device.

Gfx Low Power Mode

This option is applicable for SFF only.

Primary IGFX Boot Display (LCD Control)

Select the Video Device that will be activated during POST. This has no effect if external graphics present. Secondary booty display selection will appear based on your selection. VGA modes will be supported only on primary display.

Memory Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

Memory Information

Memory Frequency	1333 MHz
Total Memory	8192 MB (DDR3)
DIMM#0	2048 MB (DDR3)
DIMM#1	Not Present
DIMM#2	2048 MB (DDR3)
DIMM#3	Not Present
CAS Latency (tCL)	11
Minimum delay time	
CAS to RAS (tRCDmin)	11
Row Precharge (tRPmin)	11
Active to Precharge (tRASmin)	28

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-   Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

Boot Settings

This section allows you to configure the boot settings.

Aptio Setup Utility

Main	Advanced	Chipset	**Boot**	Security	Save & Exit

Boot Configuration		
Setup Prompt Timeout	1	
Bootup NumLock State	On	
Quiet Boot	Disabled	
Fast Boot	Disabled	
		→ ←**Select Screen**
CSM16 Module Version	07.68	↑↓ **Select Item**
		Enter: Select
GateA20 Active	Upon Request	**+- Change Field**
Option ROM Messages	Force BIOS	**F1: General Help**
INT19 Trap Response	Immediate	**F2: Previous Values**
		F3: Optimized Default
Boot Option Priorities		**F4: Save ESC: Exit**
► CSM parameters		

Setup Prompt Timeout

Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables/Disables Quiet Boot option.

Fast Boot

Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

GateA20 Active

UPON REQUEST – GA20 can be disabled using BIOS services.
ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages

Set display mode for Option ROM. Options are Force BIOS and Keep Current.

INT19 Trap Response
Enable: Allows Option ROMs to trap Int 19.

Boot Option Priorities
Sets the system boot order.

CSM parameters
This section allows you to configure the boot settings.

Aptio Setup Utility

Main	Advanced	Chipset	**Boot**	Security	Save & Exit

Launch CSM   Always
Boot option filter   UEFI and Legacy
Launch PXE OpROM policy   Do not launch
Launch Storage OpROM policy   Legacy only
Launch Video OpROM policy   Legacy only

Other PCI device ROM priority   Legacy OpROM

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

Boot option filter
This option controls what devices system can boot to.

Launch PXE OpROM policy
Controls the execution of UEFI and Legacy PXE OpROM.

Launch Storatge OpROM policy
Controls the execution of UEFI and Legacy Storage OpROM.

Launch Video OpROM policy
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI device ROM priority
For PCI devices other than Network, Mass storage or Video defines
which OpROM to launch.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

```
Password Description


If ONLY the Administrator's password is set, then
this only limit access to Setup and is only asked for
when entering Setup.                                       → ←Select Screen
If ONLY the User's password is set, then this is a
power on password and must be entered to boot or          ↑↓ Select Item
enter Setup. In Setup the User will have                  Enter: Select
Administrator rights                                      +-  Change Field
The password length must be                              F1: General Help
in the following range:                                  F2: Previous Values
Minimum length                            3              F3: Optimized Default
Maximum length                           20              F4: Save  ESC: Exit

Administrator Password
User Password
```

Administrator Password
Set Setup Administrator Password.

User Password
Set User Password.

Save & Exit Settings

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

Save Changes and Exit
Discard Changes and Exit
Save Changes and Reset
Discard Changes and Reset

Save Options
Save Changes
Discard Changes

Restore Defaults
Save as User Defaults
Restore User Defaults

→ ←**Select Screen**
↑↓ **Select Item**
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save   ESC: Exit

Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) 7 Series Chipset Drivers*.

2. Click *Intel(R) Chipset Software Installation Utility.*

3. When the Welcome screen to the Intel® Chipset Device Software appears, click *Next* to continue.

4. Click *Yes* to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click *Next* to continue the installation.

6. The Setup process is now complete. Click *Finish* to restart the computer and for changes to take effect.
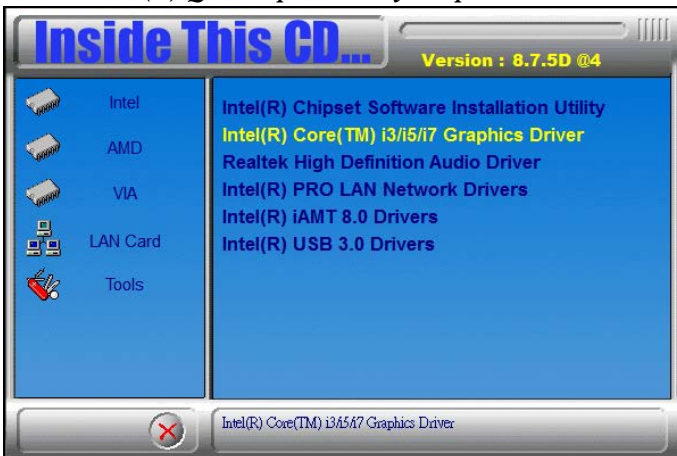
VGA Drivers Installation

NOTE: Before installing the *Intel(R) Q77 Chipset Family Graphics Driver,* the Microsoft .NET Framework 3.5 SPI should be first installed.

To install the VGA drivers, follow the steps below.

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) 7 Series Chipset Drivers*.

2. Click *Intel(R) Q77 Chipset Family Graphics Driver.*

3. When the Welcome screen appears, click *Next* to continue.

Intel® Installation Framework

Intel® HD Graphics Driver

Welcome to the Setup Program

(intel)

4. Click *Yes* to to agree with the license agreement and continue the installation.

Intel® Installation Framework

Intel® HD Graphics Driver

License Agreement

(intel)

5. On the Readme File Information screen, click *Next* to continue the installation of the Intel® Graphics Media Accelerator Driver.

Intel® Installation Framework

Intel® HD Graphics Driver

Readme File Information

(intel)

6. On Setup Progress screen, click *Next* to continue.

Intel® Installation Framework

Intel® HD Graphics Driver

Setup Progress

(intel)

7. Setup complete. Click *Finish* to restart the computer and for changes to take effect.

Realtek HD Audio Driver Installation

Follow the steps below to install the Realtek HD Audio Drivers.

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) 7 Series Chipset Drivers*.

2. Click *Realtek High Definition Audio Driver.*

3. On the Welcome to the InstallShield Wizard screen, click *Next* to proceed with and complete the installation process.

4. The InstallShield Wizard Complete. Click *Finish* to restart the computer and for changes to take effect.

LAN Drivers Installation

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) 7 Series Chipset Drivers*.

2. Click *Intel(R) PRO LAN Network Driver.*

3. Click *Install Drivers and Software.*
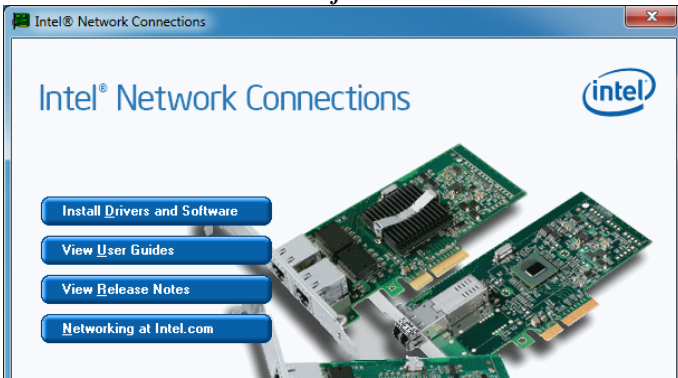
4. When the Welcome screen appears, click *Next*.
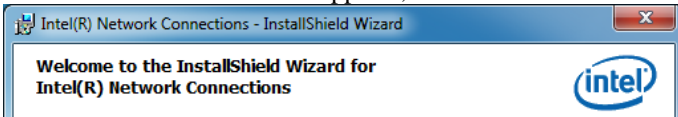
5. Click *Next* to to agree with the license agreement.
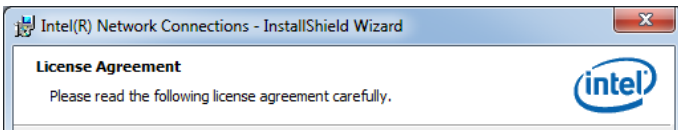
6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.
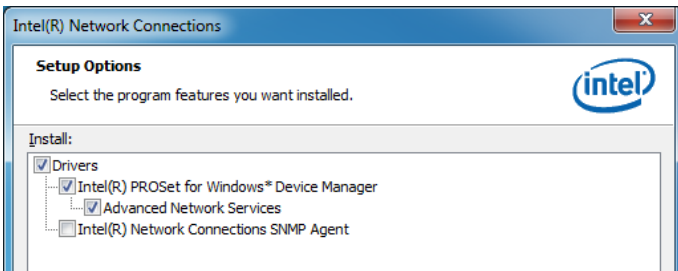
Realtek LAN Controller Drivers Installation

Follow the steps below to install the Realtek LAN Drivers.

1. Insert the CD that comes with the board. Click *Intel*, then *LAN Card,* and then *Realtek Lan Controller Drivers*.

2. Click *Realtek RTL8111E LAN Drivers.*

3. When the welcome screen to InstallShield Wizard appears, click *Next* to start the installation.
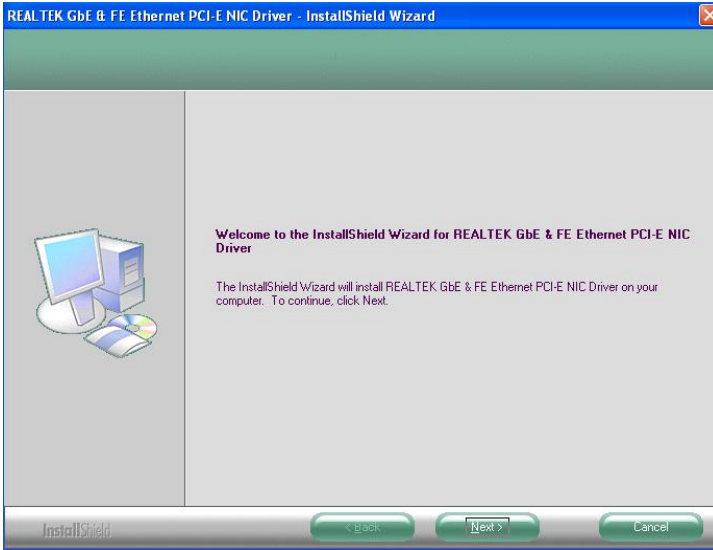
4. When the InstallShieldWizard has finished installing the Realtek LAN drivers, click *Finish*.
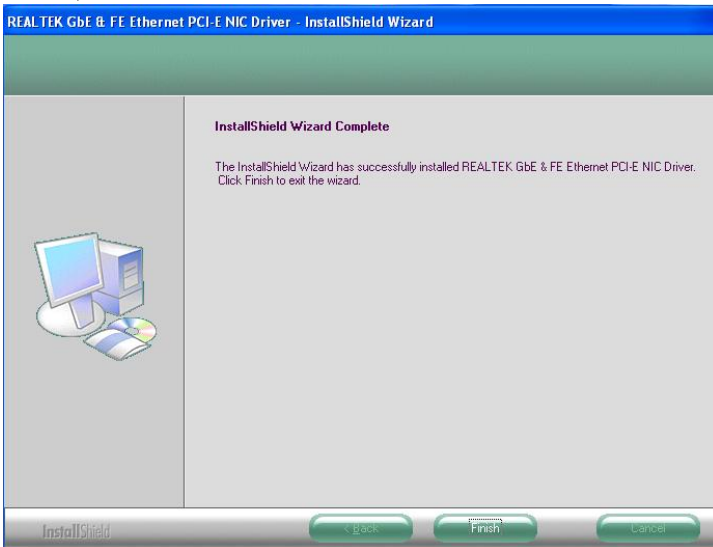
7. The wizard is ready to begin installation. Click *Install* to begin the installation.
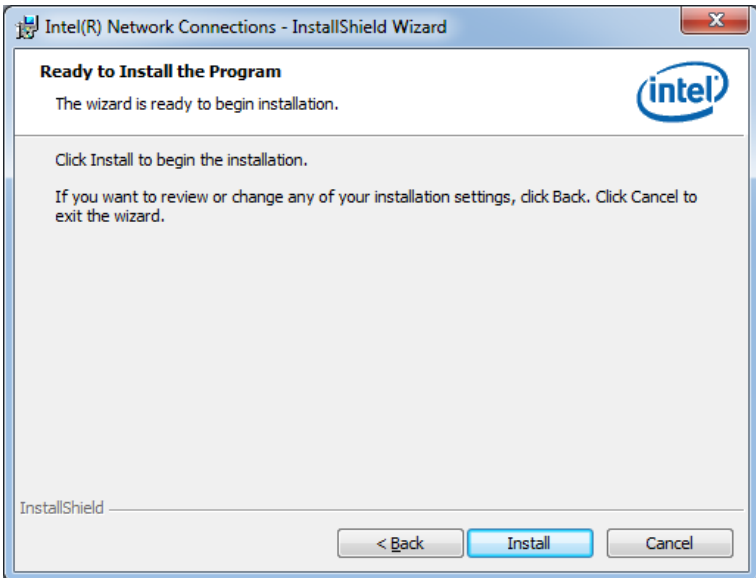
8. When InstallShield Wizard is complete, click *Finish*.
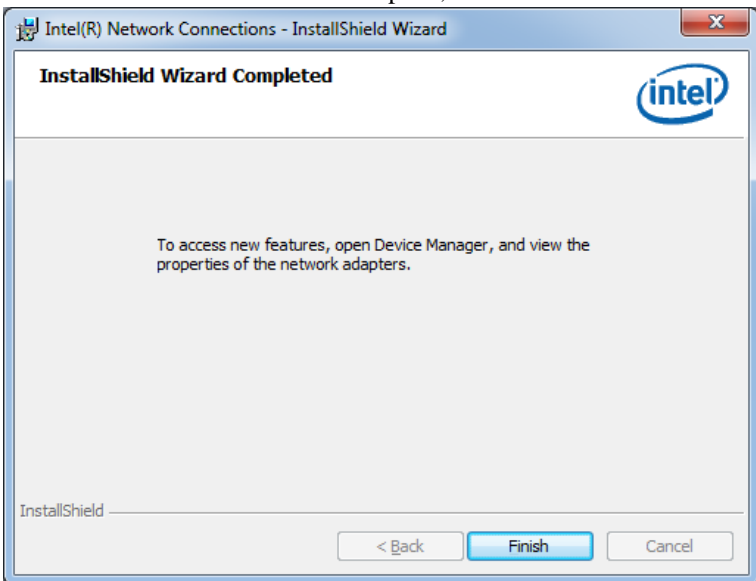
Intel® Management Engine Interface

Follow the steps below to install the Intel Management Engine.

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) AMT 8.0 Drivers*.

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click *Next*.

3. Click *Yes* to to agree with the license agreement.
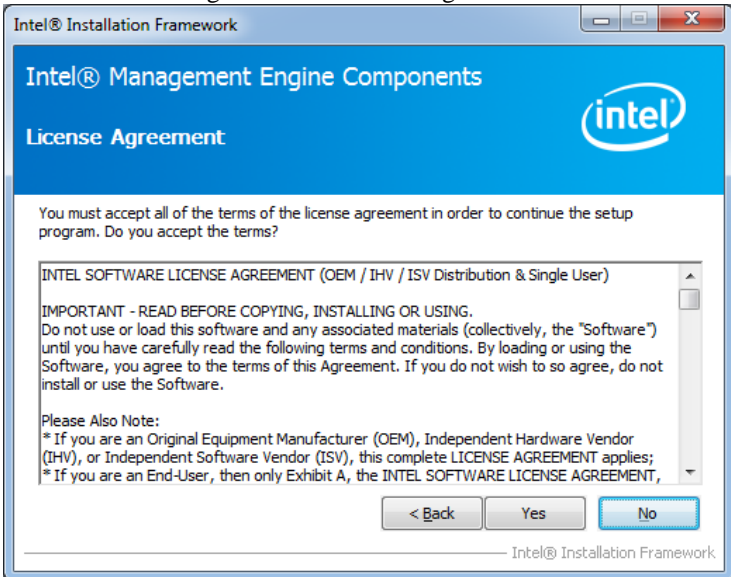
4. When the Setup Progress screen appears, click **Next**. Then, click **Finish** when the setup progress has been successfully installed.
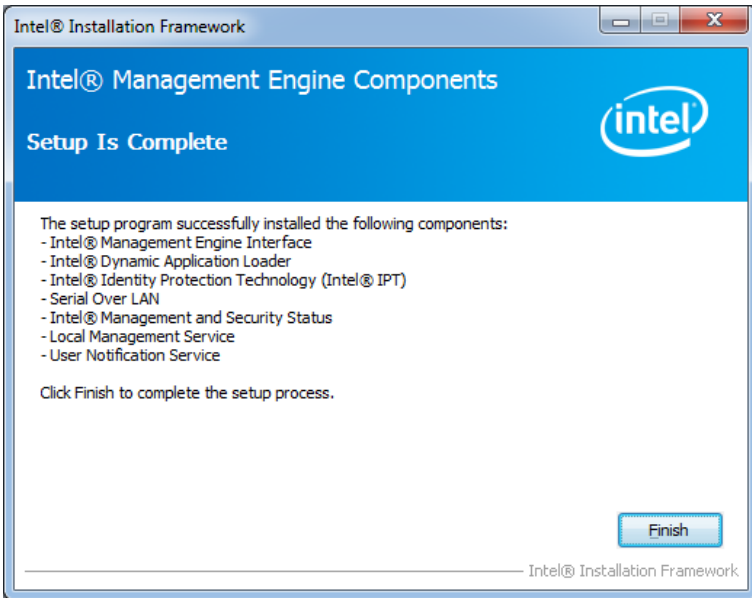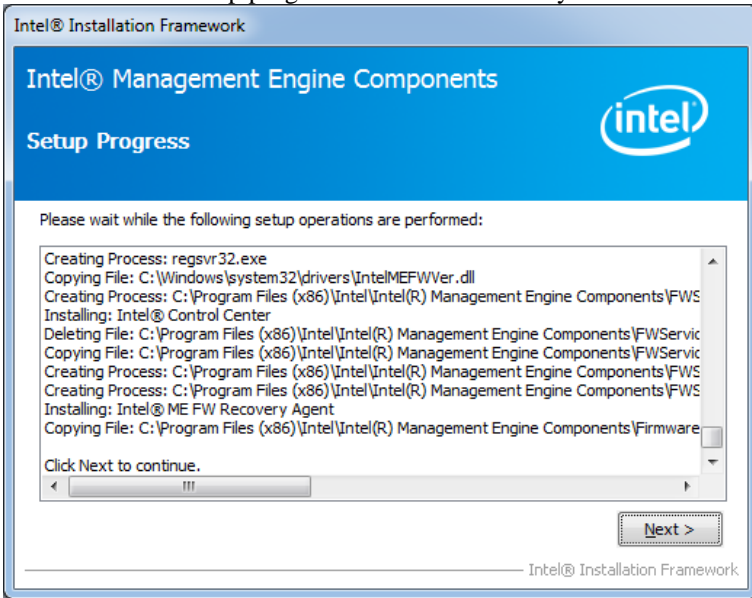
ASMedia USB 3.0 Drivers

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) 6 Series Chipset Drivers*.
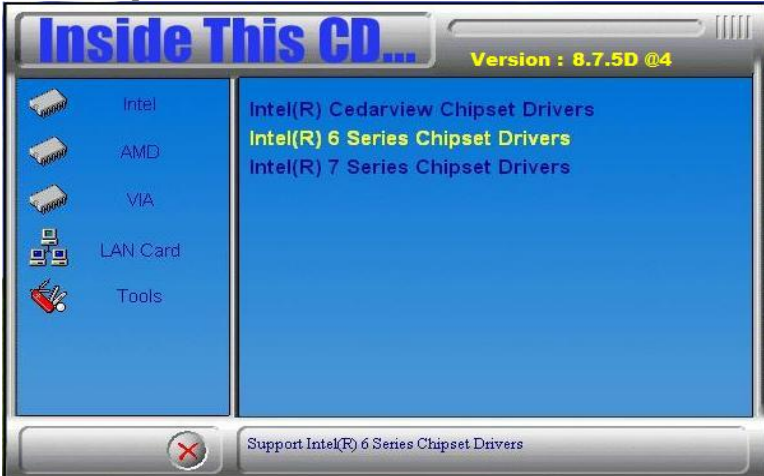
2. Click *Intel(R) PRO LAN Network Driver.*

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click *Next*.
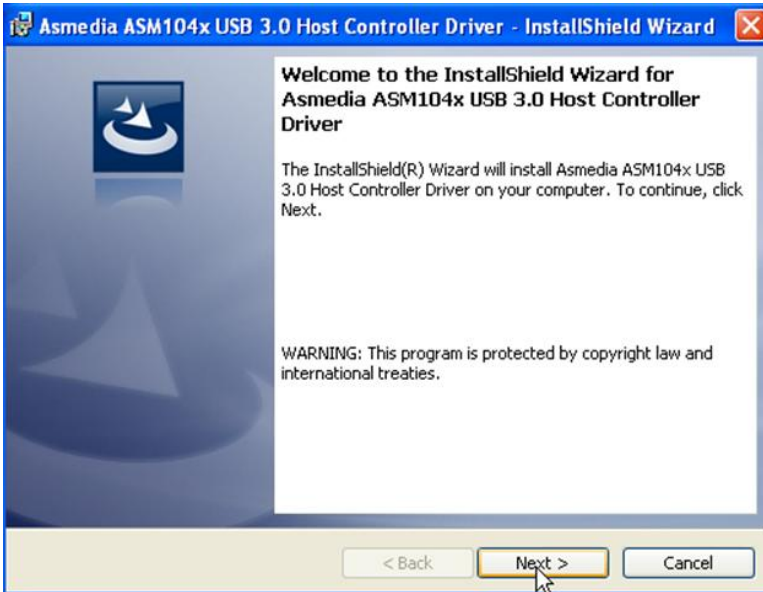
3. When InstallShield Wizard is complete, click *Finish*.
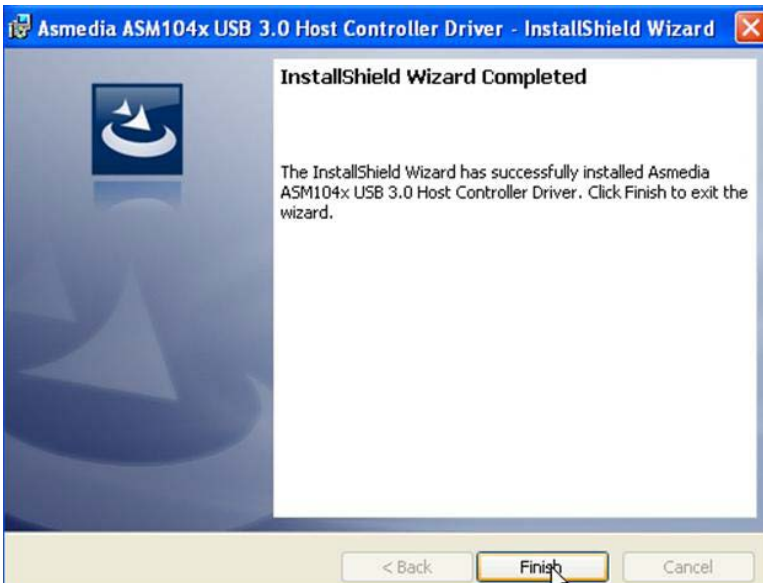
Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
2E8h – 2EFh	Serial Port #4(COM4)
2F8h - 2FFh	Serial Port #2(COM2)
2B0h - 2DFh	Graphics adapter Controller
378h - 3FFh	Parallel Port #1(LPT1)
3E8h – 3EFh	Serial Port #3(COM3)
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Serial Port #3 & Serial Port #4 & Parallel Port #1
IRQ6	Reserved
IRQ7	Reserved
IRQ8	Real Time Clock
IRQ9	Microsoft ACPI-Compliant System
IRQ10	Intel(R)6 Series /C200 Series Chipset Family SMBus Controller-1C22
IRQ12	PS/2 Mouse

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```c
//-----------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//-----------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//-----------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81866 watch dog program\n");

        SIO = Init_F81866();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81866, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime);  }
        else
        {       DisableWDT();      }

        return 0;
```

```
}
//------------------------------------------------------------------------
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_F81866_Reg(0x2B);
        bBuf &= (~0x20);
        Set_F81866_Reg(0x2B, bBuf);                    //Enable WDTO

        Set_F81866_LD(0x07);                           //switch to logic device 7
        Set_F81866_Reg(0x30, 0x01);                    //enable timer

        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= (~0x0F);
        bBuf |= 0x52;
        Set_F81866_Reg(0xF5, bBuf);                    //count mode is second

        Set_F81866_Reg(0xF6, interval);        //set timer

        bBuf = Get_F81866_Reg(0xFA);
        bBuf |= 0x01;
        Set_F81866_Reg(0xFA, bBuf);                    //enable WDTO output

        bBuf = Get_F81866_Reg(0xF5);
        bBuf |= 0x20;
        Set_F81866_Reg(0xF5, bBuf);                    //start counting
}
//------------------------------------------------------------------------
void DisableWDT(void)
{
        unsigned char bBuf;

        Set_F81866_LD(0x07);                           //switch to logic device 7

        bBuf = Get_F81866_Reg(0xFA);
        bBuf &= ~0x01;
        Set_F81866_Reg(0xFA, bBuf);                    //disable WDTO output

        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= ~0x20;
        bBuf |= 0x40;
        Set_F81866_Reg(0xF5, bBuf);                    //disable WDT
}
//------------------------------------------------------------------------
```

```
//-----------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----------------------------------------------------------------------------
#include "F81866.H"
#include <dos.h>
//-----------------------------------------------------------------------------
unsigned int F81866_BASE;
void Unlock_F81866 (void);
void Lock_F81866 (void);
//-----------------------------------------------------------------------------
unsigned int Init_F81866(void)
{
        unsigned int result;
        unsigned char ucDid;

        F81866_BASE = 0x4E;
        result = F81866_BASE;

        ucDid = Get_F81866_Reg(0x20);
        if (ucDid == 0x07)                              //Fintek 81866
        {       goto Init_Finish;       }

        F81866_BASE = 0x2E;
        result = F81866_BASE;

        ucDid = Get_F81866_Reg(0x20);
        if (ucDid == 0x07)                              //Fintek 81866
        {       goto Init_Finish;       }

        F81866_BASE = 0x00;
        result = F81866_BASE;

Init_Finish:
        return (result);
}
//-----------------------------------------------------------------------------
void Unlock_F81866 (void)
{
        outportb(F81866_INDEX_PORT, F81866_UNLOCK);
        outportb(F81866_INDEX_PORT, F81866_UNLOCK);
}
//-----------------------------------------------------------------------------
void Lock_F81866 (void)
{
        outportb(F81866_INDEX_PORT, F81866_LOCK);
}
//-----------------------------------------------------------------------------
void Set_F81866_LD( unsigned char LD)
{
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, F81866_REG_LD);
        outportb(F81866_DATA_PORT, LD);
        Lock_F81866();
}
//-----------------------------------------------------------------------------
void Set_F81866_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, REG);
        outportb(F81866_DATA_PORT, DATA);
        Lock_F81866();
}
//-----------------------------------------------------------------------------
```

```
unsigned char Get_F81866_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, REG);
        Result = inportb(F81866_DATA_PORT);
        Lock_F81866();
        return Result;
}
//-------------------------------------------------------------------------
```

```
//-------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-------------------------------------------------------------------------
#ifndef __F81866_H
#define __F81866_H                      1
//-------------------------------------------------------------------------
#define      F81866_INDEX_PORT          (F81866_BASE)
#define      F81866_DATA_PORT           (F81866_BASE+1)
//-------------------------------------------------------------------------
#define      F81866_REG_LD              0x07
//-------------------------------------------------------------------------
#define F81866_UNLOCK             0x87
#define      F81866_LOCK                      0xAA
//-------------------------------------------------------------------------
unsigned int Init_F81866(void);
void Set_F81866_LD( unsigned char);
void Set_F81866_Reg( unsigned char, unsigned char);
unsigned char Get_F81866_Reg( unsigned char);
//-------------------------------------------------------------------------
#endif //__F81866_H
```