DATA IMAGE CORPORATION

TFT Module Specification

PRELIMINARY

ITEM NO.: FG100430DNCWAG01

Table of Contents

Customer Companies	R&D Dept.	Q.C. Dept.	Eng. Dept.	Prod. Dept.
	ALEX	ERIC	PAUL	HELEN
Approved by	Version:	Issued Date:	Sheet Code:	Total Pages:
	1	2006/4/17		20

2. Record of Revision

Rev	Date	Item	Page	Comment
1	17/APR/06			Initial PRELIMINARY

3. Handing Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnection from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the interface Connector of the TFT module.
11) After installation of the TFT module into an enclosure, do not twist nor bend the TFT module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT module from outside. Otherwise the TFT module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module should be supplied by power complied with requirements of Limited Power Source, or be applied exemption.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit. Do not connect the CFL in Hazardous Voltage Circuit.

4. General Description

This specification applies to the 10.4 inch color TFT LCD module.
This module is designed for General Display.
The screen format is intended to support the SVGA (800(H) x 600(V)) screen and 262k colors (RGB 6-bits data driver).
All input signals are LVDS interface compatible.
The module does not contain an inverter card for backligh

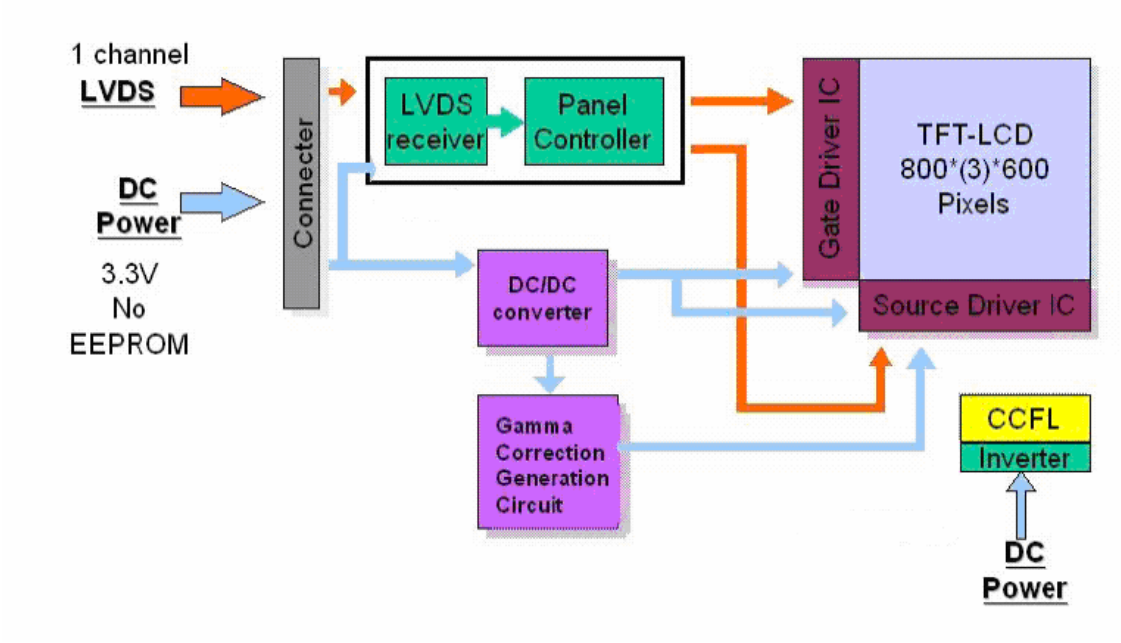
4.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition：

Items	Unit	Specifications
Screen Diagonal	[mm]	10.4”
Outline dimension	[mm]	236.0(W)x 174.3(H)x 5.6(D)
Active Area	[mm]	211.2(H) x158.4(V)
Pixel H x V		800(R,G,Bx3) x 600
Pixel Pitch	[mm]	0.264(H) x 0.264(V)
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		TN mode, Normally White
Typical White Luminance (ICFL=4.5 mA)	[cd/m2]	230 Typ. (center)
Contrast Ratio		500：1 Typ.
Optical Rise Time/Fall Time	[msec]	10/25 Typ.
Viewing angle (CR≧10)		60/60/35/65 (L/R/U/D)
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.
Typical Power Consumption (VDD line + VCFL line)	[Watt]	3.3 Typ
Weight	[Grams]	280 Typ ± 10
Surface treatment	[mm]	Anti-glare, hard coating 3H
Electrical Interface		1 channel LVDS
Support Color		Native 262K colors (RGB 6-bit driver)
Temperature Range Operating Storage(Shipping)	 [°C] [°C]	 0 to +50 -20 to +60

4.2 Functional Block Diagram

The following diagram shows the functional block of the 10.4 inches Color TFT LCD Module：



5. Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows：

(GND = 0 V,Ta=25°C)

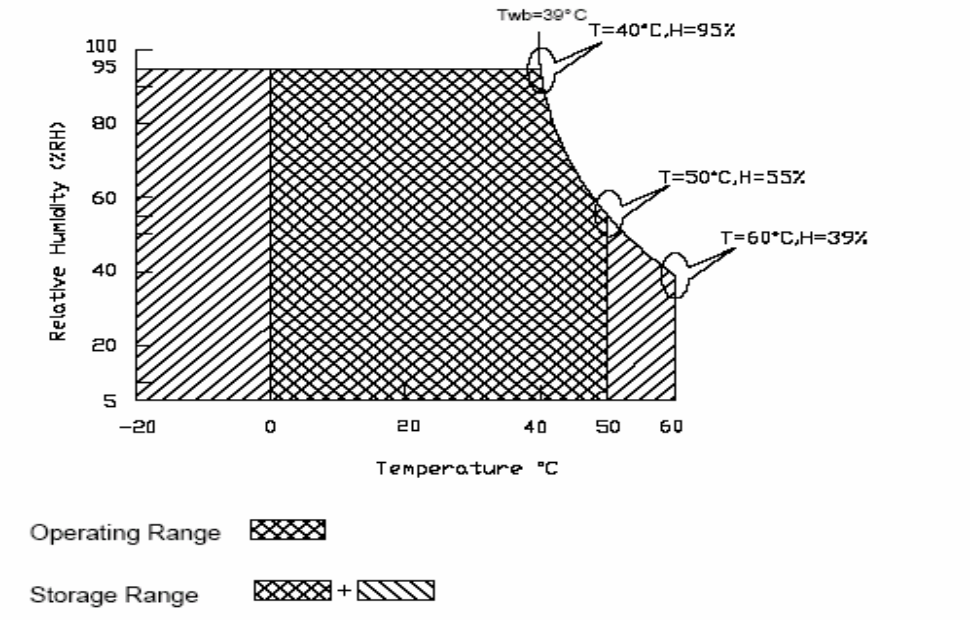
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
CCFL Current	ICFL	3.0	5.5	[mA] rms	
CCFL Ignition Voltage	Vs	--	800	Vrms	
Operating Temperature	TOP	0	+50	[°C]	Note1
Operating Humidity	HOP	8	90	[%RH]	Note1
Storage Temperature	TST	-20	+60	[°C]	Note1
Storage Humidity	HST	5	90	[%RH]	Note1

Note 1: The relative humidity must not exceed 90% non-condensing at temperatures of 40 °C or less.

At temperatures greater than 40°C, the wet bulb temperature must not exceed 39°C. When operate at low temperatures, the brightness of CCFL will drop and the life time of CCFL will be reduced.

Note2：The unit should not be exposed to corrosive chemicals.

Wet bulb temperature chart



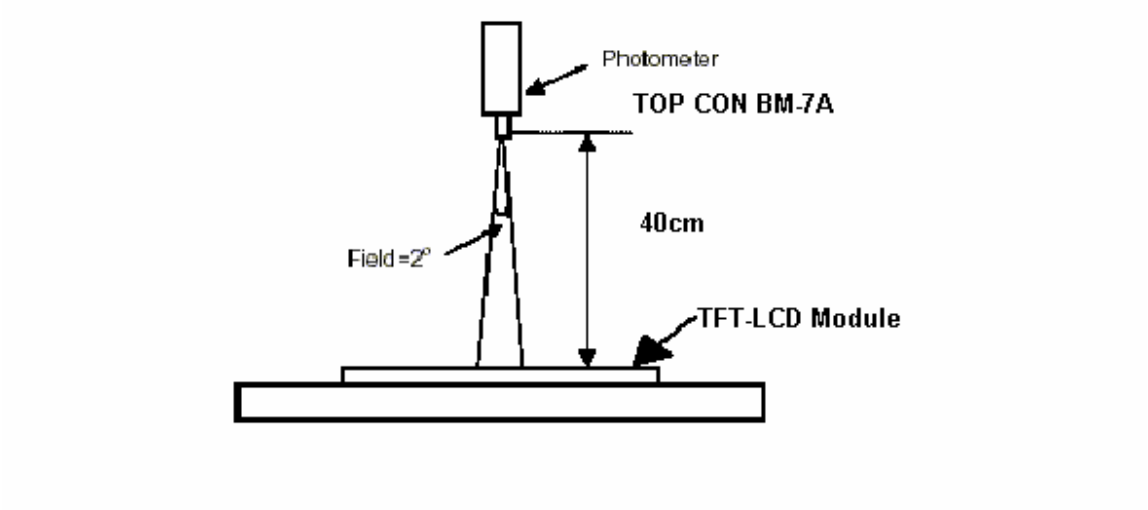
Note1：Maximum Wet-Bulb should be 39°C and no condensation.

6. Optical Characteristics

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ_X+	Center CR≥10	50	60	--	deg	Note 1,4
		θ_X-		50	60	--		
	Vertical	θ_Y+		30	35	--		
		θ_Y-		60	65	--		
Contrast Ratio		CR max.	Center	400	500	--		Note 1,3
Response time	Rise	Tr	Center	-	10	20	ms	Note 1,6
	Fall	Tf	θx=θy =0°	-	25	30	ms	
Brightness Uniformity		B-uni	θx=θy =0°	70	80	--	%	Note1,5
Central Luminance		L	I_{CFL}=4.5mA	200	230	--	cd/m^2	Note 1,2,4
Lamp Life time		--		10,000	20000	--	hours	
Chromaticity		X_W	Center θx=θy =0°	0.280	0.320	0.340		Note 1,7
		Y_W		0.300	0.330	0.360		
		X_R		0.540	0.570	0.600		
		Y_R		0.290	0.320	0.350		
		X_G		0.270	0.300	0.330		
		Y_G		0.530	0.560	0.590		
		X_B		0.115	0.145	0.175		
		Y_B		0.100	0.130	0.160		
Image sticking		tis	2 hours			2	Sec	Note 8

The following optical specifications shall be measured in a darkroom or equivalent state(ambient luminance≤1 lux, and at room temperature). The measurement must be taken after backlight warming up for 20 minutes. The operation temperature is 25°C±2°C. The measurement method is shown in Note1.

Note1: The method of optical measurement:



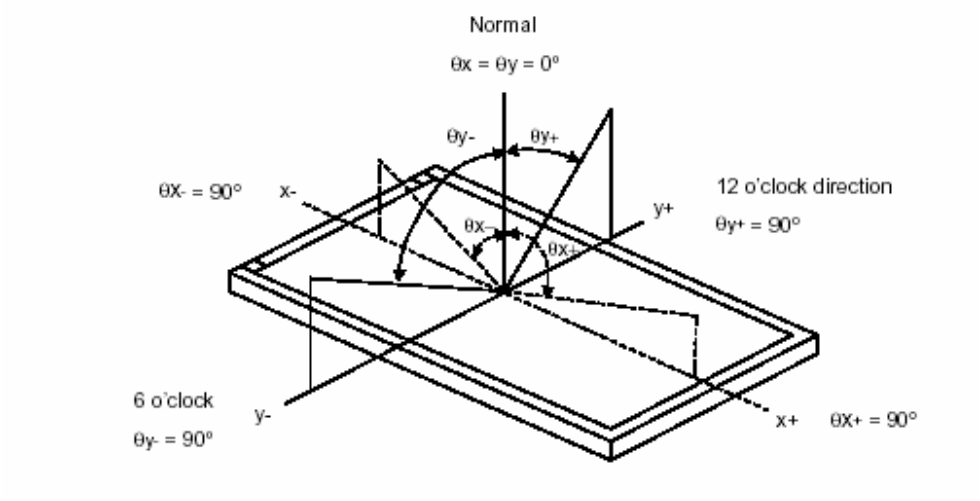
Note2: Definition of Central Luminance(L):

Central Luminance must be measured at the central point of the LCD module and at the viewing angle of the θx=θy=0°(Note 4) when all the input terminals of LCD panel are electrically opened.

Note3: Definition of Contrast Ratio (CR):

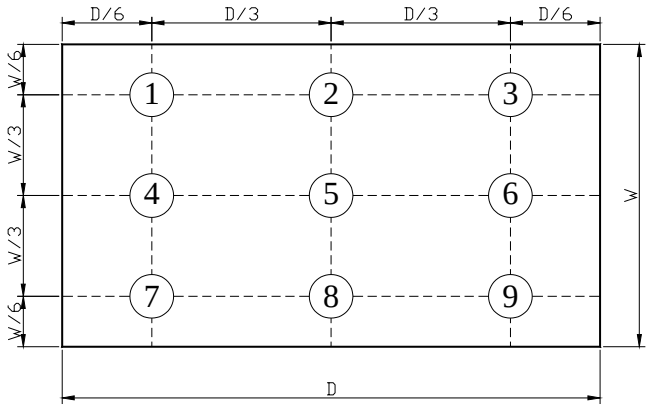
$$CR = \frac{\text{Luminance with all pixels in white state}}{\text{Luminance with all pixels in Black state}}$$

Note 4: Definition of Viewing Angle(CR≥10):



Note 5: Definition of Brightness Uniformity (Buni):

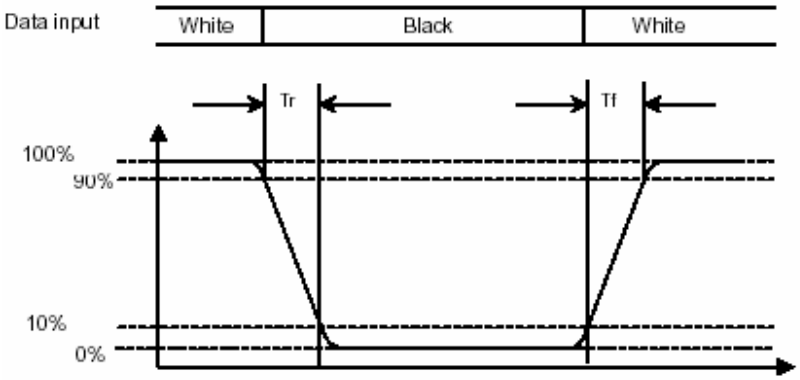
Luminance Measuring Points



$$\text{B-uni} = \frac{\text{Minimum luminance of 9 points}}{\text{Maximum luminance of 9points}}$$

Note6: Definition of Response Time:

The Response Time is set initially by defining the “Rising Time (Tr)” and the “Falling Time (Tf)” respectively. Tr and Tf are defined as following figure.



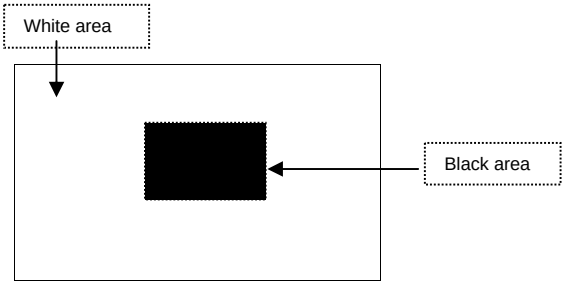
Note 7: Definition of Chromaticity:

The color coordinates (X_W,Y_W),(X_R,Y_R),(X_G,Y_G),and (X_B,Y_B) are obtained with all pixels in the viewing field at white, red, green, and blue states, respectively.

Note 8: Definition of Image sticking (tis):

Continuously display the test pattern shown in the figure below for 2 hours. Then display a completely white screen. The previous image shall not persist more than 2 sec at 25 °C

Image sticking pattern



7. Signal Interface

7.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will following components.

Connector Name / Designation	For Signal Connector
Manufacturer	HIROSE
Type / Part Number	HRS DF 19K-20P-1H
Mating Connector / Part Number	HRS DF19G-20S-1C (WIRE TYPE))
Mating Connector / Part Number	HRS DF19-20S-1F (FPC TYPE)

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Connector / Part Number	SM02B-BHSS-1-TB

7.2 Signal Pin

Pin assignment
(1)Input signal interface

Pin no	Symbol	Function	Etc.
1	V_{DD}	+3.3 V power supply	
2	V_{DD}	+3.3 V power supply	
3	GND	Ground	
4	GND	Ground	
5	RxIN0-	LVDS receiver signal channel 0	
6	RxIN0+		
7	GND	Ground	
8	RxIN1-	LVDS receiver signal channel 1	
9	RxIN1+		
10	GND	Ground	
11	RxIN2-	LVDS receiver signal channel 2	
12	RxIN2+		
13	GND	Ground	
14	CKIN-	LVDS receiver signal clock	
15	CKIN+		
16	GND	Ground	

17	NC	No Connection	
18	NC	No Connection	
19	GND	Ground	
20	GND	Ground	

(2)LVDS transmitter/receiver signal mapping

	Symbol	**Function**	
TxIN0	R0	Red data (LSB)	6 bit red display data
TxIN1	R1	Red data	
TxIN2	R2	Red data	
TxIN3	R3	Red data	
TxIN4	R4	Red data	
TxIN5	R5	Red data (MSB)	
TxIN6	G0	Green data (LSB)	6 bit green display data
TxIN7	G1	Green data	
TxIN8	G2	Green data	
TxIN9	G3	Green data	
TxIN10	G4	Green data	
TxIN11	G5	Green data (MSB)	
TxIN12	B0	Blue data (LSB)	6 bits blue display data
TxIN13	B1	Blue data	
TxIN14	B2	Blue data	
TxIN15	B3	Blue data	
TxIN16	B4	Blue data	
TxIN17	B5	Blue data (MSB)	
TxIN18	Hs	Horizontal sync.	
TxIN19	Vs	Vertical sync.	
TxIN20	DE	Data enable	
TxCLKIN	CLK	Clock	Dot clock

7.3 Signal Description

The module using a LVDS receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Note：Input signals shall be low or Hi-Z state when VDD is off.

Signal Name	Description
RxIN0-, RxIN0+	LVDS differential data input (Red0-Red5, Green0)
RxIN1-, RxIN1+	LVDS differential data input (Green1-Green5, Blue0-Blue1)
RxIN2-, RxIN2+	LVDS differential data input (Blue2-Blue5, Hsync, Vsync, DE)
CKIN-, CKIN+	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground
NC	No Connection

Signal Name	Description	
+RED5	Red Data 5 (MSB)	Red-pixel Data
+RED4	Red Data 4	Each red pixel's brightness data consists of these
+RED3	Red Data 3	6 bits pixel data.
+RED2	Red Data 2	
+RED1	Red Data 1	
+RED0	Red Data 0 (LSB)	
	Red-pixel Data	
+GREEN5	Green Data 5 (MSB)	Green-pixel Data
+GREEN4	Green Data 4	Each green pixel's brightness data consists of these
+GREEN3	Green Data 3	6 bits pixel data.
+GREEN2	Green Data 2	
+GREEN1	Green Data 1	
+GREEN0	Green Data 0 (LSB)	
	Green-pixel Data	
+BLUE5	Blue Data 5 (MSB)	Blue-pixel Data
+BLUE4	Blue Data 4	Each blue pixel's brightness data consists of these
+BLUE3	Blue Data 3	6 bits pixel data.
+BLUE2	Blue Data 2	
+BLUE1	Blue Data 1	
+BLUE0	Blue Data 0 (LSB)	
	Blue-pixel Data	

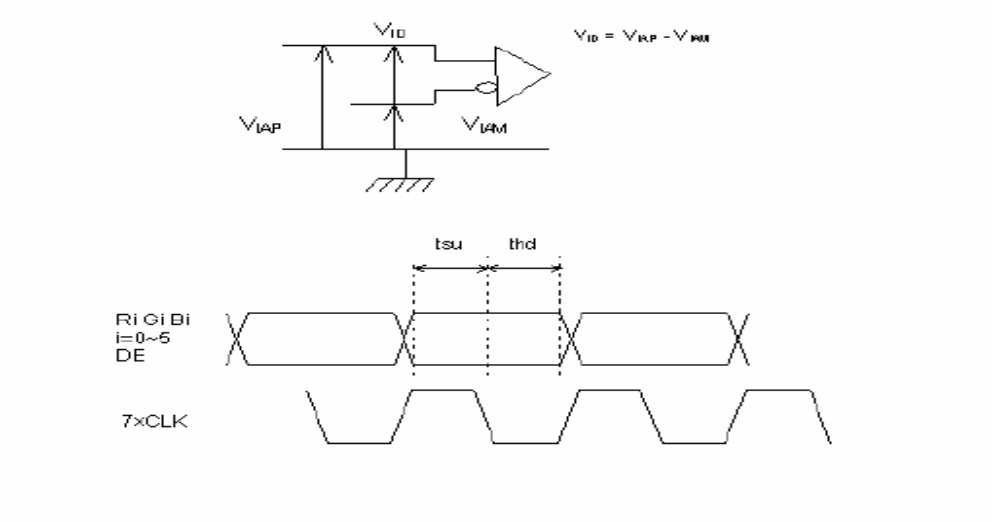
Signal Name	Description	
CLK	Data Clock	The typical frequency is 40MHz. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of CLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to CLK.
HSYNC	Horizontal Sync	The signal is synchronized to CLK.

Note：Output signals from any system shall be low or Hi-Z state when VDD is off.

7.4 Signal Electrical Characteristics

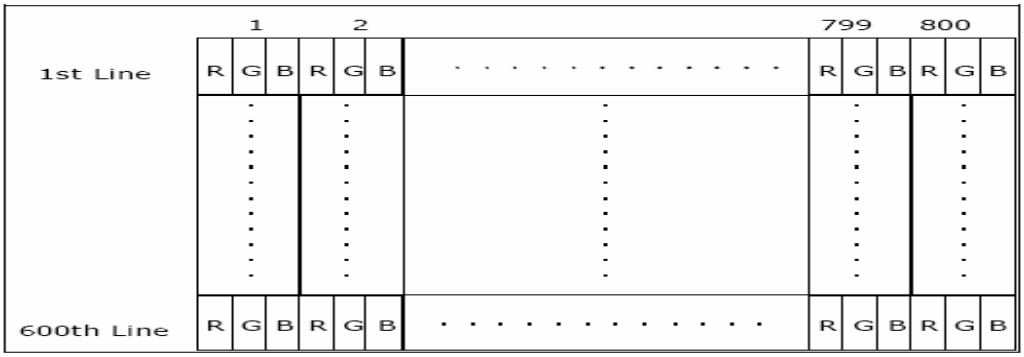
Input signals shall be low or Hi-Z state when VDD is off.
It is recommended to refer the specifications of SN75LVDS86(Texas Instruments) in detail.
Signal electrical characteristics are as follows：

Item	Symbol	Min.	Typ.	Max.	Unit
The differential level	| VID |	0.1	-	0.6	V
The common mode input voltage	VIC	$\frac{\lvert VID \rvert}{2}$	-	$2.4-\frac{\lvert VID \rvert}{2}$	V
The input setup time	tsu	0.5	-	-	ns
The input hold time	thd	0.5	-	-	ns
High-level input voltage	V IAP	2.0			V
Low-level input voltage	VIAM			0.8	V
Clock frequency	CLK	31		68	MHz



8.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format：



9. Parameter guide line for CFL inverter

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	510	560	610	Vrms	Note 1
Lamp current	I_L	3.0	4.5	5.5	mArms	Note 1
Power consumption	P_L	-	2.52	-	W	Note 2
Lamp starting voltage	V_S	-	-	1050	Vrms	T=0°C
		-	-	800		T=25°C
Frequency	F_L	-	60	-	KHz	Note 3
Lamp life time	L_L	10000	20000	-	Hr	Note 1, 4

Note1：T=25°C,I_L=4.5 mArms

Note 2: Inverter should be designed with the characteristic of lamp. When you are designing the inverter, the output voltage of the inverter should comply with the following conditions.

(1). The area under the positive and negative cycles of the waveform of the lamp current and lamp voltage should be area symmetric(the symmetric ratio should be larger than 90%).

(2). There should not be any spikes in the waveform.

(3). The waveform should be sine wave as possible.

(4). Lamp current should not exceed the maximum value within the operating Temperature (It is prohibited to over the maximum lamp current even if operated in The non-guaranteed temperature). When lamp current over the maximum value for a long time, it may cause fire. Therefore, it is recommend that the inverter should have the current limited circuit.

Note 3: Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency shall be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.

Note 4: Brightness (IL=4.5mA) to be decrease to the 50% of the initial value.

Signal for Lamp connector

Pin no.	Symbol	Function	Remark
1	H	CCFL power supply(H.V.)	Cable color: Pink
2	L	CCFL power supply(GND)	Cable color: White

10. Interface Timings

10.1 Display color v.s. input data signals:

		Data Signal																	
		Red						Green						Blue					
Color		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Green(0)/ Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Blue(0)/ Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note : Each basic color can be displayed in 64 gray scales using the 6 bit data signals. By combining the 18-bit data signals(R, G, B), the 262, 144 colors can be achieved on the display.

10.1 Timing Characteristics

(a) DE mode

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock frequency	Fck	36	40	50	MHz	
Horizontal blanking	Thb1	18	256	624	Clk	
Vertical blanking	Tvb1	3	28	184	Th	

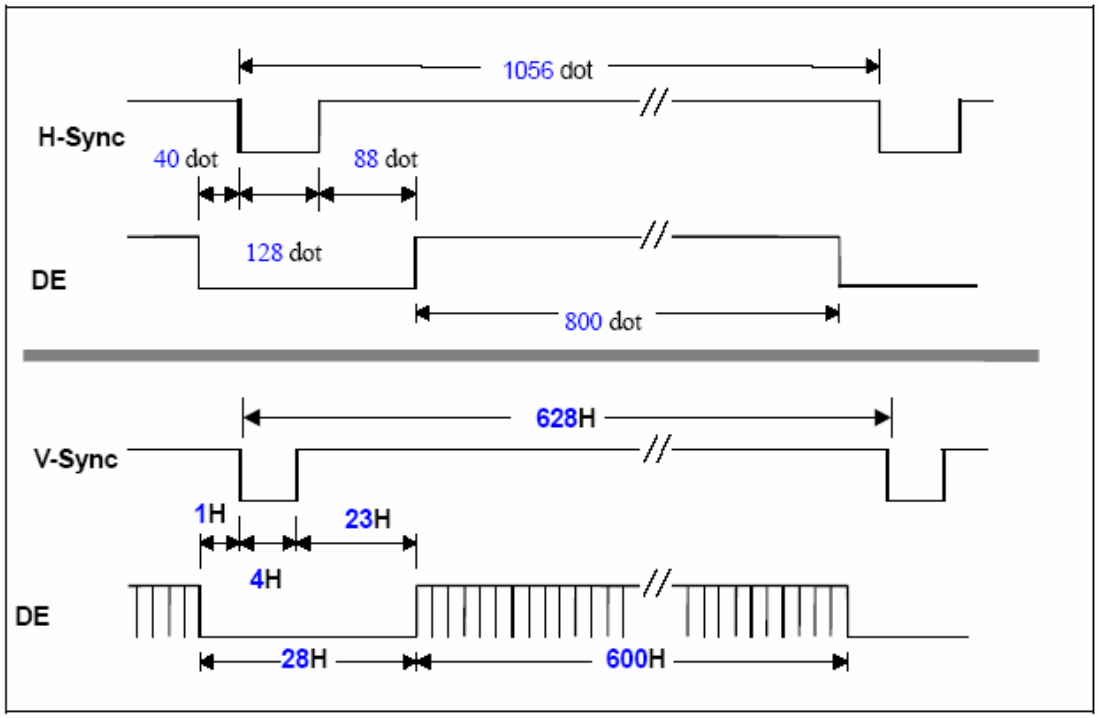
(b) HV mode

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock frequency	Fck	36	40	50	MHz	
Hsync period	Th	818	1056	1424	Clk	
Hsync pulse width	Thw	2	128	--	Clk	
Hsync front porch	Thf	8	40	--	Clk	
Hsync back porch	Thb	4	88	--	Clk	
Hsync blanking	Thb1	18	256	624	Clk	
Vsync period	Tv	603	628	784	Th	
Vsync pulse width	Tvw	1	4	--	Th	
Vsync front porch	Tvf	0	1	--	Th	
Vsync blanking	Tvb1	3	28	184	Th	
Hsync/Vsync phase shift	Tvpd	2	320	--	Clk	

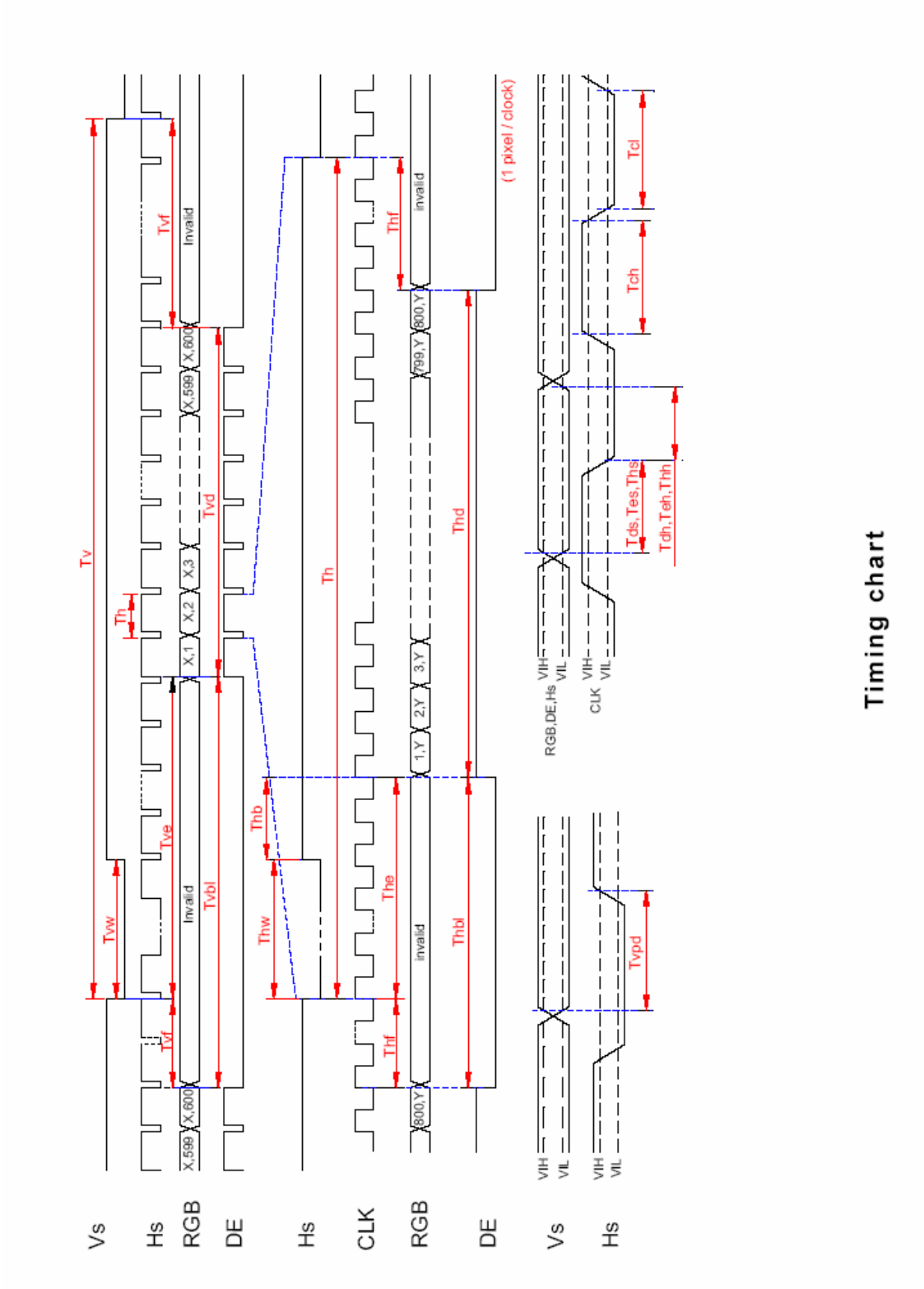
10.2Display position

D(1,1)	D(2,1)	……	D(X,1)	……	D(799,1)	D(800,1)
D(1,2)	D(2,2)	……	D(X,2)	……	D(799,2)	D(800,2)
. . .		……	. . .	……	. . .	. . .
D(1,Y)	D(2,Y)	……	D(X,Y)	……	D(799,Y)	D(800,Y)
. . .		……	. . .	……	. . .	. . .
D(1,599)	D(2,599)	……	D(X,599)	……	D(799,599)	D(800,599)
D(1,600)	D(2,600)	……	D(X,600)	……	D(799,600)	D(800,600)

10.3 Timing Definition



10.4 Timing Chart



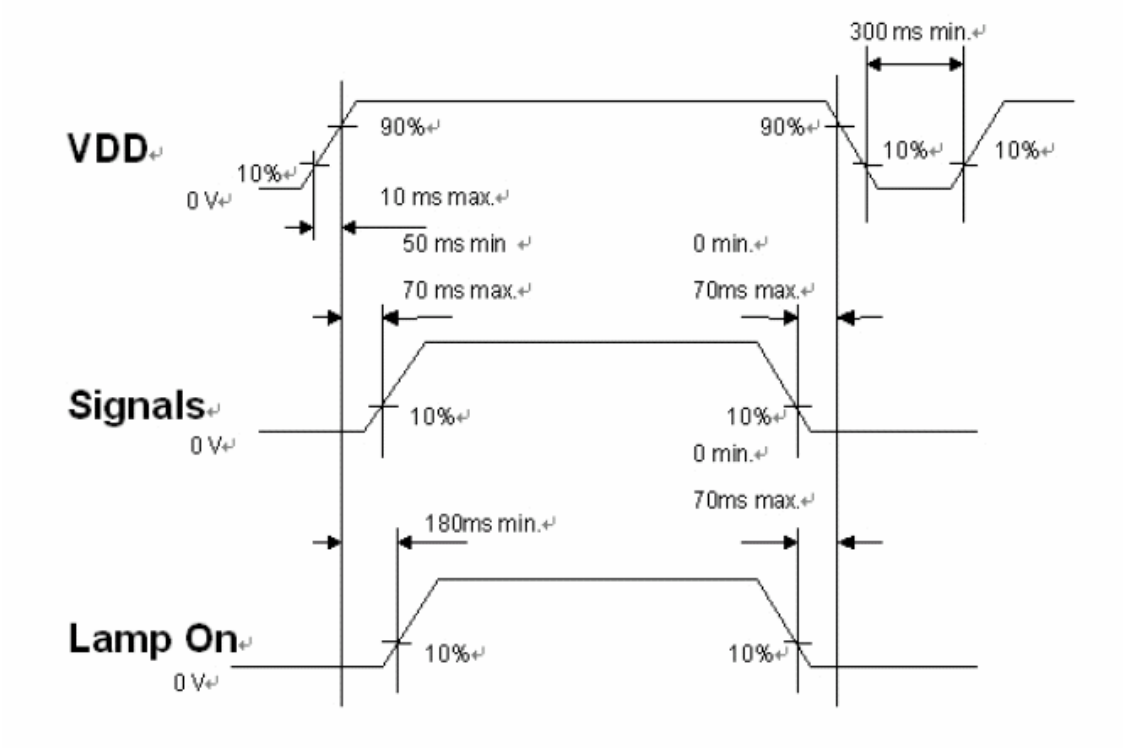
11. Power Consumption

Input power specifications are as follows：

(GND = 0 V,Ta=25°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply voltage	Input voltage	V_{DD}	3.0	3.3	3.6	V	
	Current consumption	I_{DD}		230	310	mA	
	Inrush current	I_{RUSH}	-	-	1500	mApeak	
Internal logic	Low voltage	V_{IL}	0	-	0.3 V_{DD}		
	High voltage	V_{IH}	0.7V_{DD}	-	V_{DD}		
Power ripple voltage		V_{RP}	-	-	100	mVp-p	
LCD Drive power consumption		P_{DD}		0.76		[Watt]	

12.Power ON/OFF Sequence



VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.
Note: Refer to the following power-on condition.

13. QUALITY ASSURANCE

13.1 Test Condition

13.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 25 ± 5°C
Humidity : 65 ± 5%

13.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

13.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

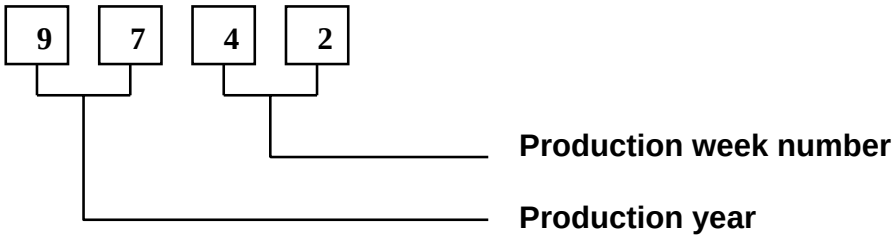
13.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

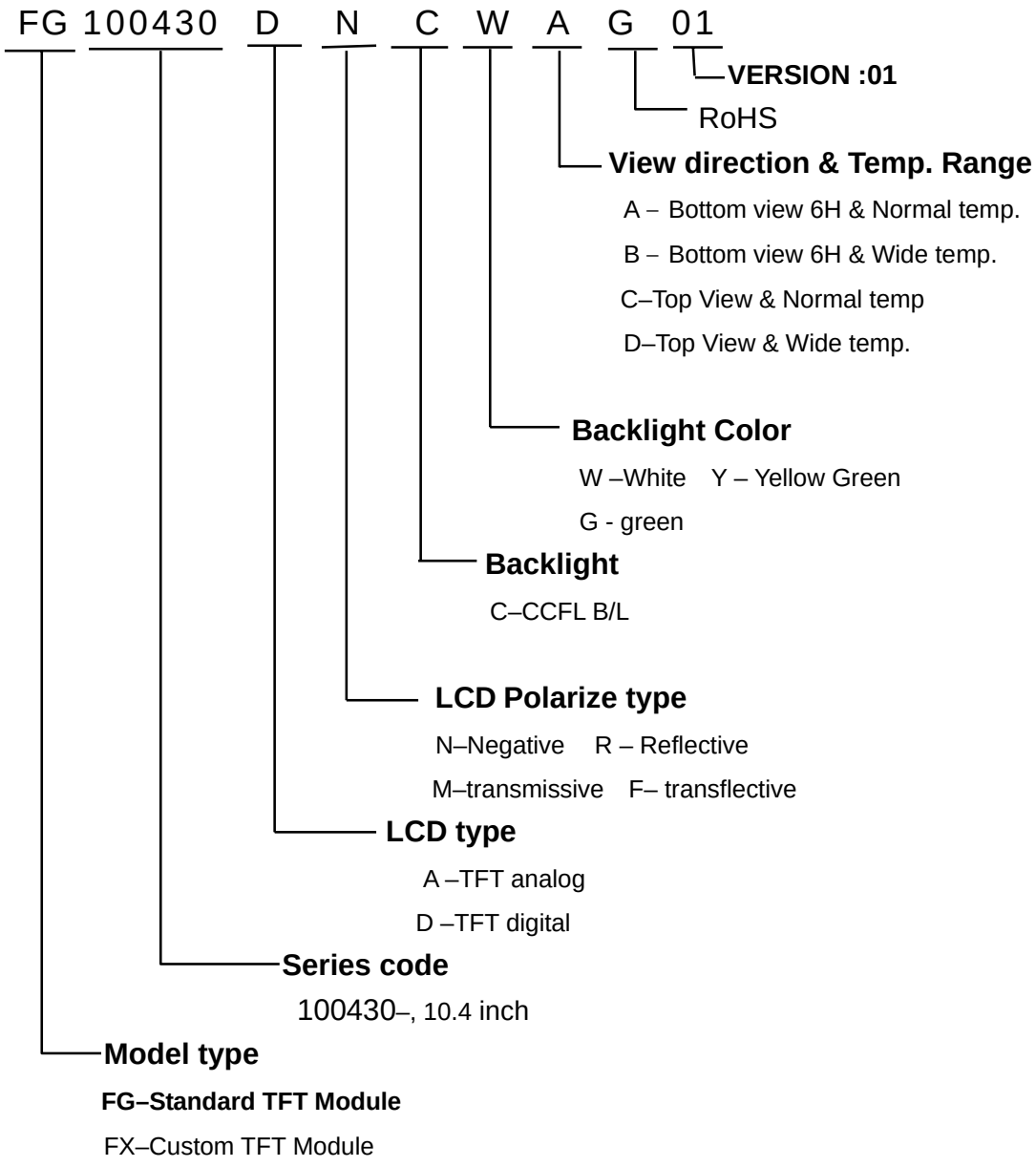
13.1.5 Test Method

Reliability Test Item & Level		Test Level
No.	Test Item	
1	High Temperature Storage Test	T=60℃,240hrs
2	Low Temperature Storage Test	T=-20℃,240hrs
3	High Temperature Operation Test	T=-50℃,240hrs
4	Low Temperature Operation Test	T=0℃,240hrs
5	High Temperature and High Humidity Operation Test	40℃,90%RH,240hrs
6	Thermal Cycling Test (No operation)	-20℃ → +25℃ → +60℃,5 Cycles 60 min 10 min 60 min
7	Vibration Test (No operation)	Frequency：10 ~ 57 Hz Amplitude：1.0 mm 58 ~ 500 Hz, 1G Sweep Time：11min Test Period：3hrs (1hrs for each Direction of X,Y,Z)
8	Shock Test (No operation)	80G, 6ms Direction：± X,± Y,± Z Cycle：1 times

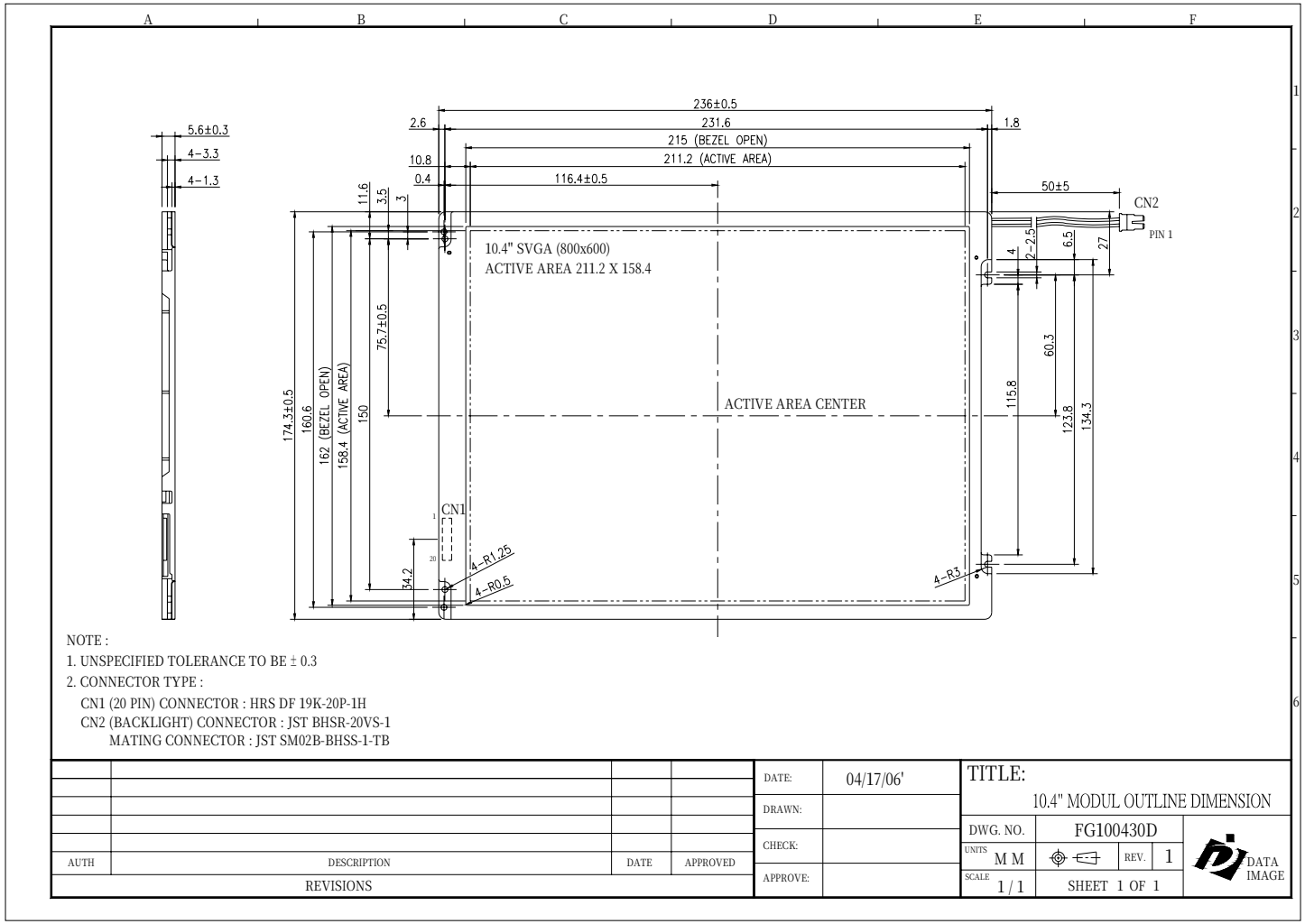
14. LOT NUMBERING SYSTEM



15. LCM NUMBERING SYSTEM



16. Mechanical Characteristics



NOTE :
1. UNSPECIFIED TOLERANCE TO BE ± 0.3
2. CONNECTOR TYPE :
   CN1 (20 PIN) CONNECTOR : HRS DF 19K-20P-1H
   CN2 (BACKLIGHT) CONNECTOR : JST BHSR-20VS-1
   MATING CONNECTOR : JST SM02B-BHSS-1-TB

AUTH	DESCRIPTION	DATE	APPROVED
REVISIONS			

DATE:	04/17/06'
DRAWN:	
CHECK:	
APPROVE:	

TITLE: 10.4" MODUL OUTLINE DIMENSION

DWG. NO.	FG100430D		
UNITS M M		REV.	1
SCALE 1 / 1	SHEET 1 OF 1		

DATA IMAGE