DATA IMAGE CORPORATION

TFT Module Specification

ITEM NO.: FG030565DSSWBG03

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	A	2010/6/3		39

2.RECORD OF REVISION

Rev	Date	Item	Page	Comment
1	31/OCT/07			Initial preliminary
2	19/DEC/07	8 8 10 10 10 18	7 8 17 21 26 38	Modify: DC Electrical Characteristics Modify: LED Dice Life Time Modify: Command Table Modify: Function Control (R05H) Modify: SPI Setting Code (R05H) Modify: OUTLINE DRAWING
3	21/May/08	8 9 10	8~13 14 24	Modify: AC Characteristics Modify: SERIAL INTERFACE Modify: Vertical Porch (R17h)
A	3/Jun/10’			Release Rev A for production

3.FEATURES

- Support CCIR656/CCIR601 8 bit format or 8 bit serial RGB or 24 bit parallel RGB.
- Support the SPI commands setting, the operation parameters setting internally.
- Our components and processes are compliant to RoHS standard
- Programmable gamma correction curve.
- Non-Volatile Memory (OTP) for VCOM calibration

4.GENERAL SPECIFICATIONS

Parameter		Specifications	Unit
Screen Size		3.5 (diagonal)	inch
Surface Treatment		Anti-Glare	
Display Format		320 X RGB X 240	dots
Active Area		70.08 (W) x 52.56 (H)	mm
Dot Pitch		0.073(W) x 0.219 (H)	mm
Pixel Configuration		Stripe	
Outline Dimension		77.8 (W) x 64.5 (H) x 2.9(T)	mm
Weight		42	g
View Angle direction		6 o'clock	
Temperature Range	Operation	-20~70	℃
	Storage	-30~80	℃

5.ABSOLUTE MAXIMUM RATINGS

(GND= 0V)

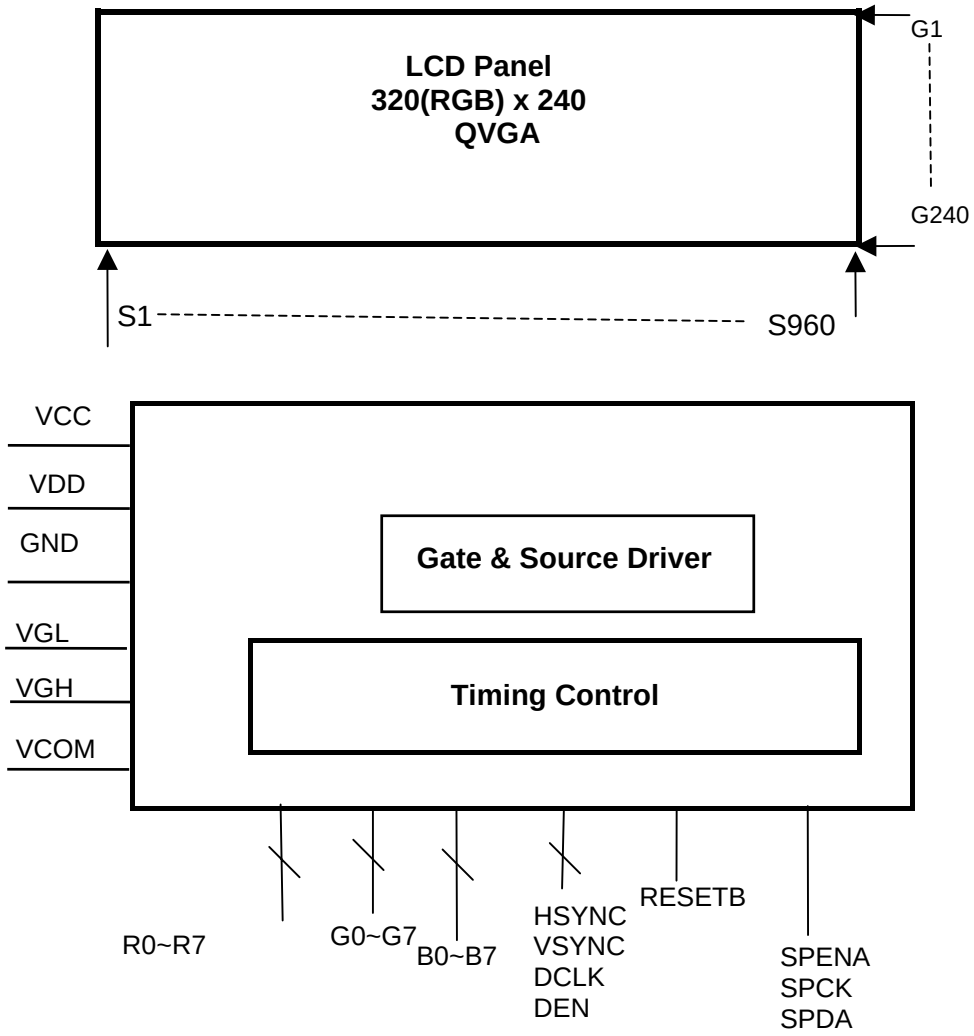
Parameter	Symbol	MIN.	MAX.	Unit
Power supply voltage	VCC	-0.3	+4.0	V
Power supply voltage	VDD	-0.3	+5.5	V
Power supply voltage	VGH	-0.3	+32	V
Power supply voltage	VGL	-22	+0.3	V
Input voltage	Vin	-0.3	VCC+0.3	V

Note:

*All of the voltages listed above are with respective to GND= 0V.

*Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

6.BLOCK DIAGRAM



7.INPUT / OUTPUT TERMINALS

Pin	Symbol	I/O	Description	Remark
1	VGL	VI	Gate output low voltage	
2	VGH	VI	Gate output high voltage	
3	VCOM	VI	VCOM input signal	
4	GND	VI	Ground	
5	RESETB	I	Hardware global reset. Low active. Normally pull high.	
6	UD	I	UP/Down scan setting. When UD="L", down to up. When UD="H", up to down.	
7	LRC	I	The shift direction of device internal shift register is controlled by this Pin as shown below: LRC="H", left to right LRC="L", right to left	
8	NC		NO Connection	
9	NC		NO Connection	
10	SPENA	I	Serial port Data Enable Signal. Internal pull high, leave it OPEN when not used.	
11	SPCK	I	Serial port Clock. Internal pull high, leave it OPEN when not used.	
12	SPDA	I	Serial port Data input. Internal pull high, leave it OPEN when not used.	
13	POL	O	Polarity signal to monitor VCOM signal.	
14	B7	I	Digital data input. B0 is LSB and B7 is MSB 1. If parallel RGB input mode is used, BX, GX, and RX indicate B, G, and R data in turn. 2. If serial RGB or CCIR601/656 input mode is select, only R0 – R7 are used, and others (BX,GX) short to GND.	
15	B6	I		
16	B5	I		
17	B4	I		
18	B3	I		
19	B2	I		
20	B1	I		
21	B0	I		
22	VLED1	VI	Power supply of LED1 back light.	
23	VLED2	VI	Power supply of LED2 back light.	
24	GLED2	VI	Ground of LED2 back light.	
25	GLED1	VI	Ground of LED1 back light.	

Pin No	Symbol	I/O	Description	Remark
26	G7	I	Digital data input. G0 is LSB and G7 is MSB 1. If parallel RGB input mode is used, BX, GX, and RX indicate B, G, and R data in turn. 2. If serial RGB or CCIR601/656 input mode is select, only R0 – R7 are used, and others (BX,GX) short to GND.	
27	G6	I		
28	G5	I		
29	G4	I		
30	G3	I		
31	G2	I		
32	G1	I		
33	G0	I		
34	VDD	VI	Power supply input. +5.0V	
35	GND	VI	Ground	
36	R7	VI	Digital data input. R0 is LSB and R7 is MSB 1. If parallel RGB input mode is used, BX, GX, and RX indicate B, G, and R data in turn. 2. If serial RGB or CCIR601/656 input mode is select, only R0 – R7 are used, and others (BX,GX) short to GND.	
37	R6	I		
38	R5	I		
39	R4	I		
40	R3	I		
41	R2	I		
42	R1	I		
43	R0	I		
44	DCLK (DOTCLK)	I	Clock signal. Latching data at the rising edge.	
45	HSYNC	I	Horizontal sync in digital RGB mode.	
46	VSYNC	I	Vertical sync in digital RGB mode.	
47	DEN	I	Input data enable control.	
48	NC		NO Connection	
49	VCC	I	Power supply input. +3.3V	
50	VCC	I	Power supply input. +3.3V	

8. ELECTRICAL CHARACTERISTICS

8.1 DC Electrical Characteristics

(GND= 0V, TA=25℃)

Parameter	Symbol	MIN.	TYP	MAX.	Unit	Remark
Power supply voltage (1)	VCC	3	3.3	3.6	V	
Power supply voltage (2)	VDD	-	5	-	V	
Low level input voltage	VIL	0	-	0.2x VCC	V	
High level input voltage	VIH	0.8x VCC	-	VCC	V	
Output high voltage	VOH	0.9x VCC	-	VCC	V	IOH=-100uA
Input leakage current	I_{IN}	-1	-	+1	μA	No pull up or pull down.
Gate on voltage	VGH	14	15	16	V	
Gate off voltage	VGL	-11	-10	-9	V	
Digital operating current	ICC	-	2	-	mA	VCC=3.3V
Analog operating current	IDD	-	1.5	-	mA	VDD=5V
Power consumption	I_{VGH}	-	25	-	μA	VGH=15V
Power consumption	I_{VGL}	-	35	-	μA	VGL=-10V
VCOM	$V_{com\ AC}$	-	5.1	-	Vp-p	
	$V_{com\ DC}$	-	1.3	-	V	

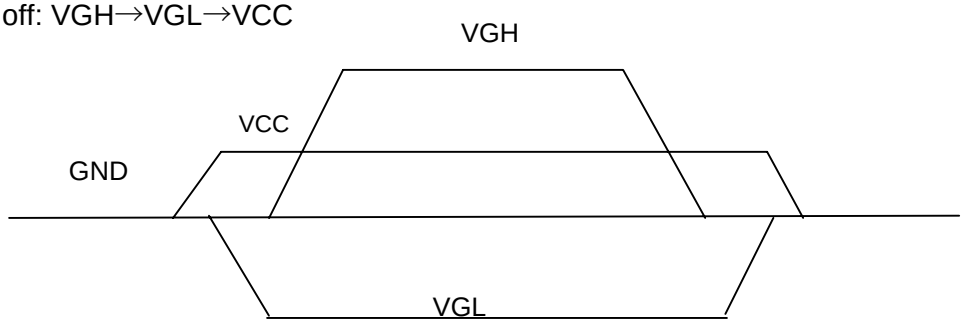
8.2 Hardware reset timing

Parameter	Symbol	Min.	Typ.	Max.	Unit.
RESETB low pulse width	T_{RSB}	10	-	-	μs

8.3 Power ON/OFF sequence

To prevent the device from damage due to latch up, the power ON/OFF sequence shown below must be followed.

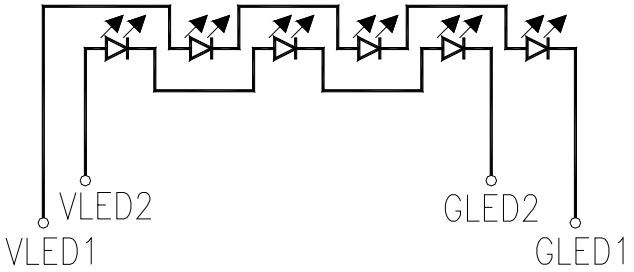
When power on: VCC→VGL→VGH
When power off: VGH→VGL→VCC



8.4 BACKLIGHT DRIVING FOR POWER CONSUMPTION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
VLED1\VLED2 voltage	V_L	9.0	10.2	11.4	V	I_L=40 mA Ta= 25 ℃
LED(1+2) current	I_L	--	20+20	--	mA	Ta= 25 ℃
LED Dice Life Time		--	40000		Hours	Note:1

Note 1: The “LED dice life time” is defined as the LED dice brightness decrease to 50% original brightness that the ambient temperature is 22℃and LED dice current 20mA.



8.5 AC Characteristics

(Unless otherwise specified, Voltage Referenced to GND, VCC = 3.3V, Ta = 25℃)

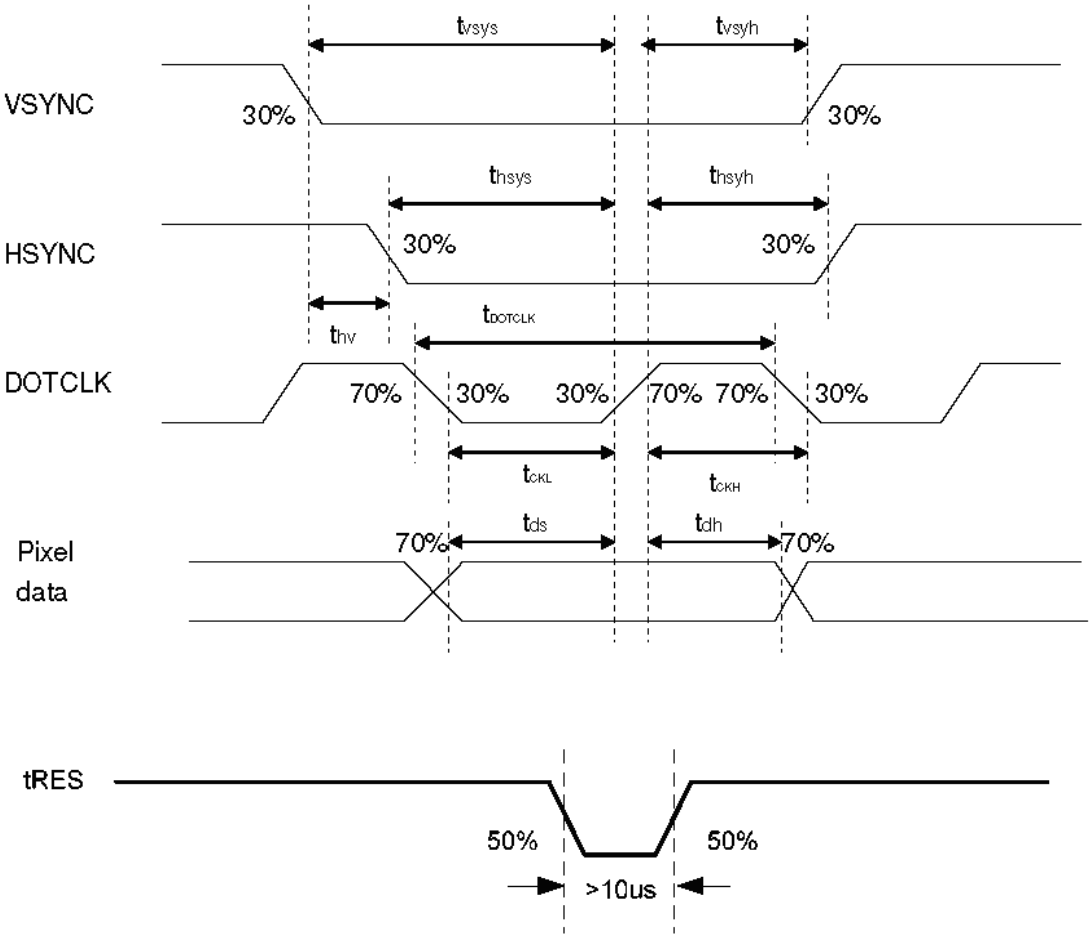
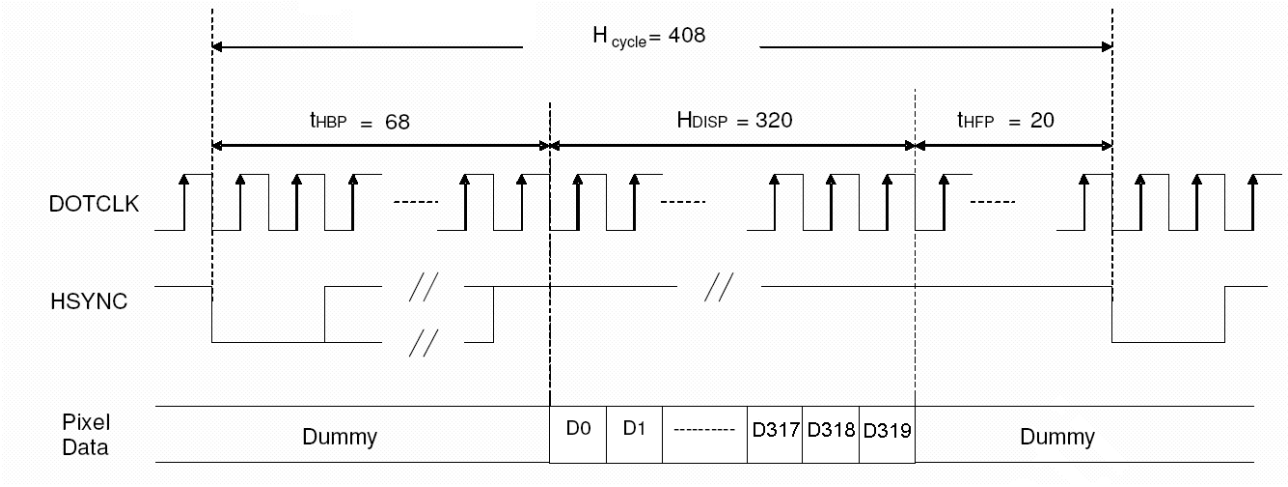


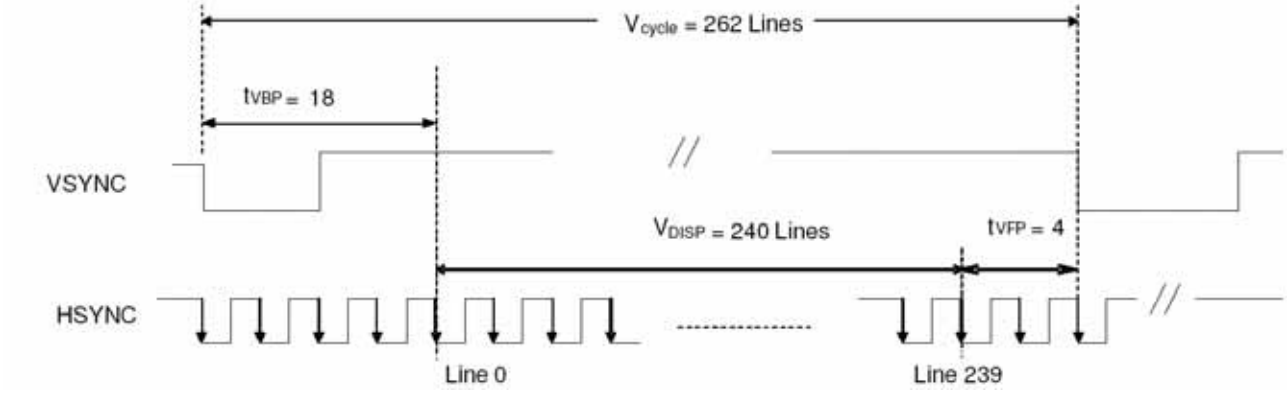
Figure 1 Pixel & tRES timing

Characteristics	Symbol	Min		Typ		Max		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	fDOTCLK	-		6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-		ns
Vertical Sync Setup Time	tvsys	20	10	-		-		ns
Vertical Sync Hold Time	tvsyh	20	10	-		-		ns
Horizontal Sync Setup Time	thsys	20	10	-		-		ns
Horizontal Sync Hold Time	thsyh	20	10	-		-		ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-		-		ns
DOTCLK High Period	tCKH	50	15	-		-		ns
Data Setup Time	tds	12	8	-		-		ns
Data hold Time	tdh	12	8	-		-		ns
Reset pulse width	tRES	10		-		-		us

Table 1 Pixel & tRES timing



a) Horizontal Data Transaction Timing



b) Vertical Data Transaction Timing

Figure 2 Data transaction timing in parallel RGB (24 bit) interface (SYNC mode)

Characteristics		Symbol	Min		Typ		Max		Unit
			24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency		fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period		tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)		fH	-		15.72		22.35		KHz
Vertical Frequency (Refresh)		fV	-		60		90		Hz
Horizontal Back Porch		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Front Porch		tHFP	-	-	20	60	-	-	tDOTCLK
Horizontal Data Start Point		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Blanking Period		tHBP + tHFP	-	-	88	264	-	-	tDOTCLK
Horizontal Display Area		HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle		Hcycle	-	-	408	1224	450	1350	tDOTCLK
Vertical Back Porch		tVBP	-		18		-		Lines
Vertical Front Porch		tVFP	-		4		-		Lines
Vertical Data Start Point		tVBP	-		18		-		Lines
Vertical Blanking Period		tVBP + tVFP	-		22		-		Lines
VS Pulse width		tWV	-		4		-		Lines
Vertical Display Area	NTSC	VDISP	-		240		-		Lines
	PAL				280(PALM=0)				
					288(PALM=1)				
Vertical Cycle	NTSC	Vcycle	-		262		350		Lines
	PAL				313				

Table 2 Data transaction timing in normal operating mode

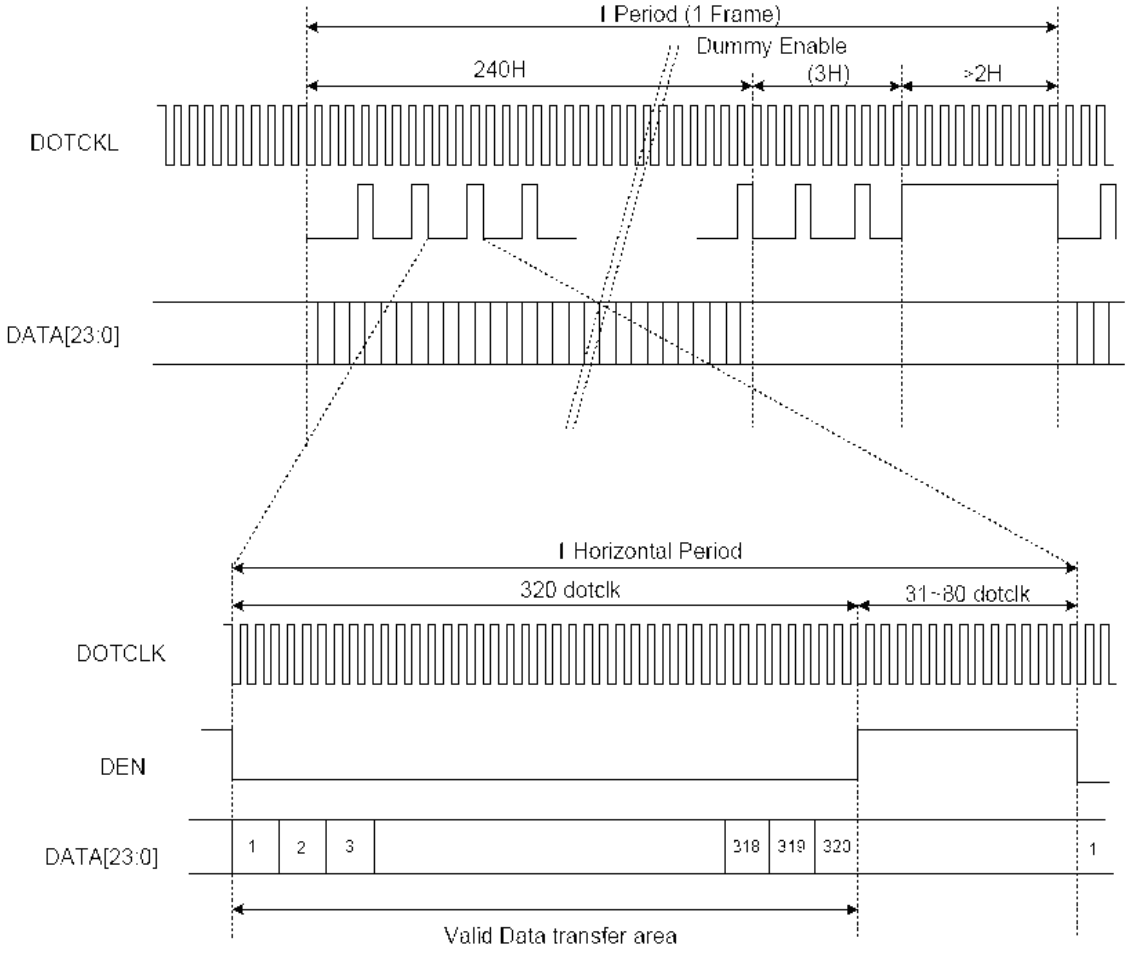


Figure 3 Signal timing in DE mode

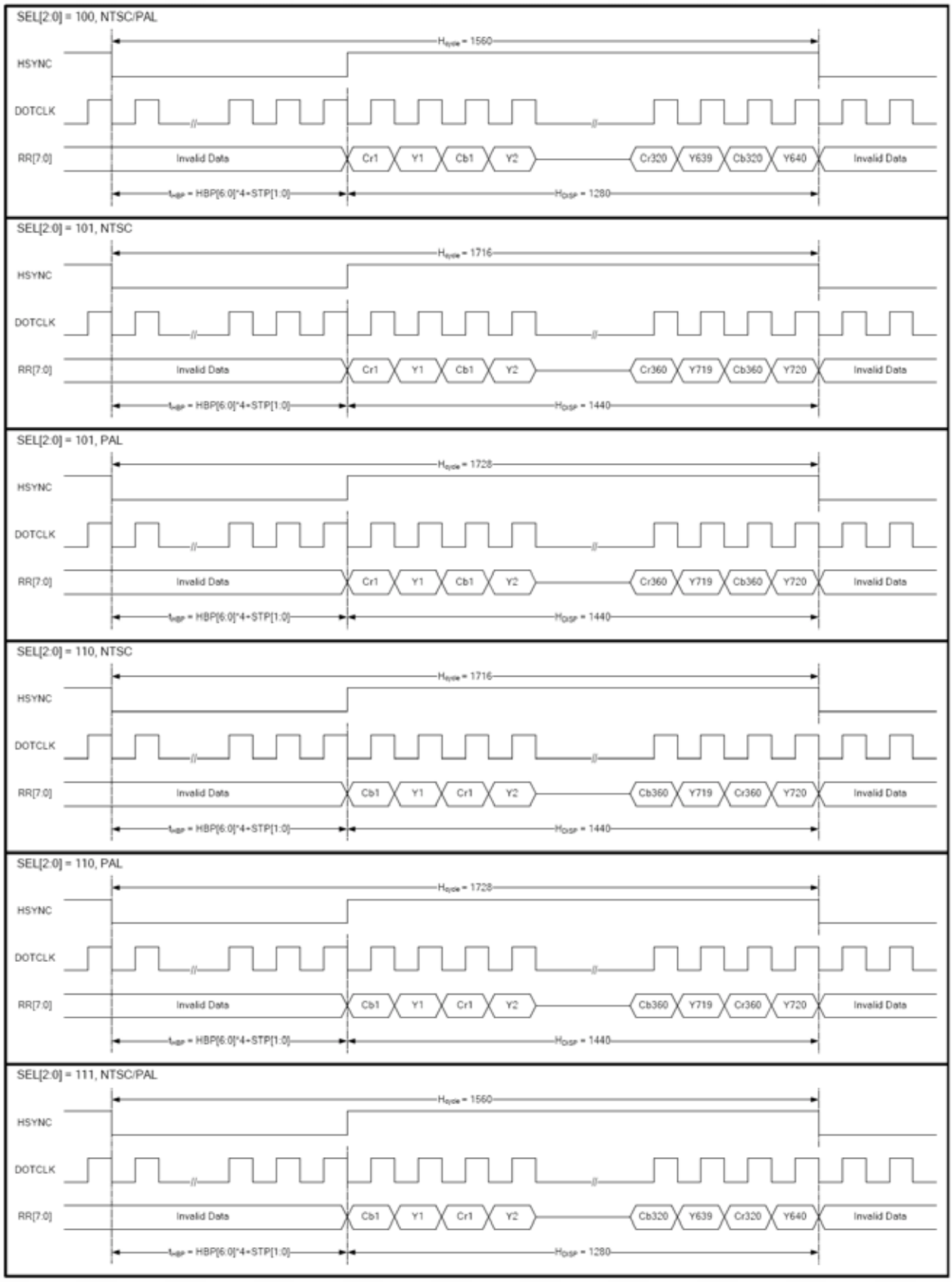


Figure 4 CCIR601 horizontal timing

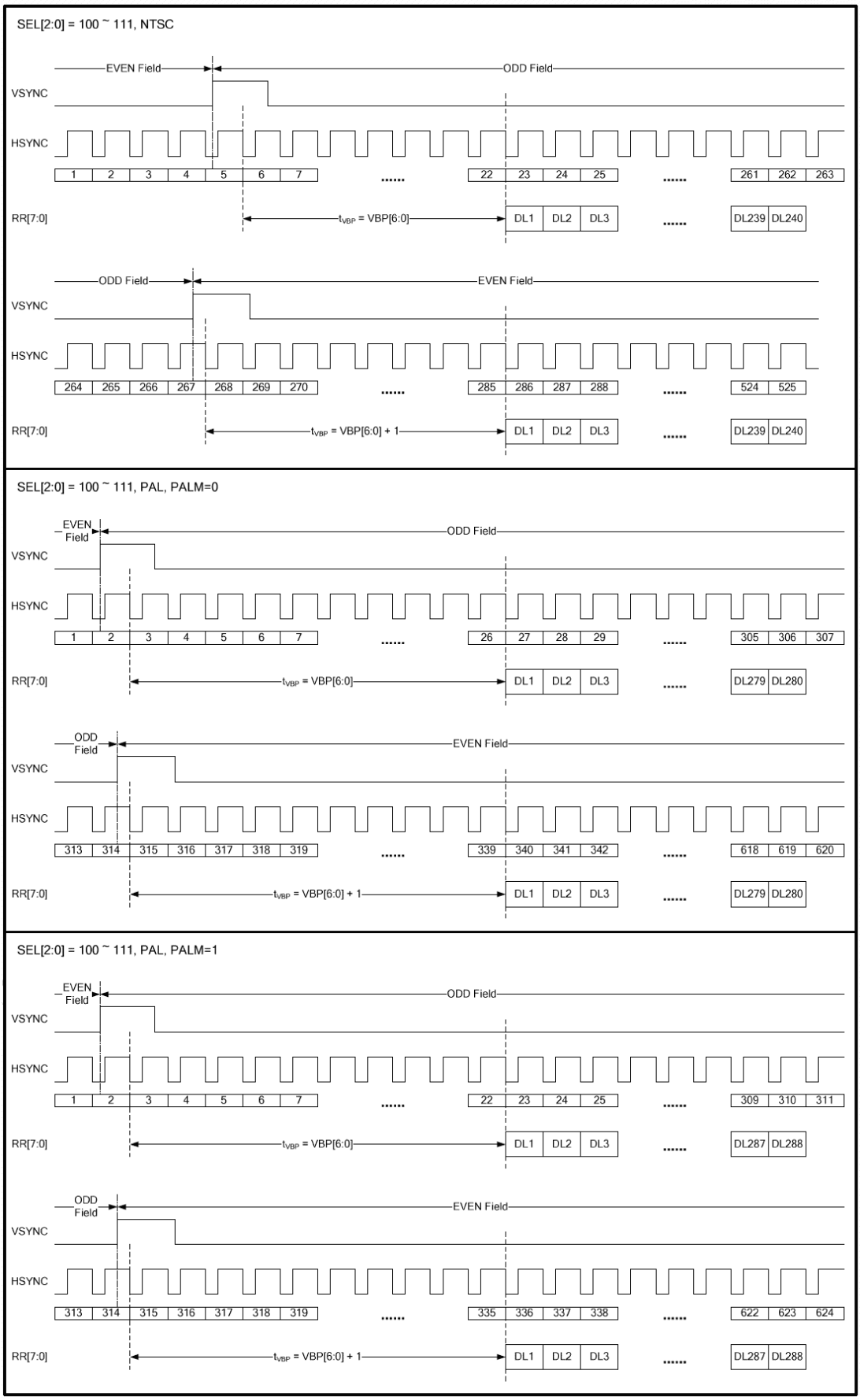


Figure 5 CCIR601 vertical timing

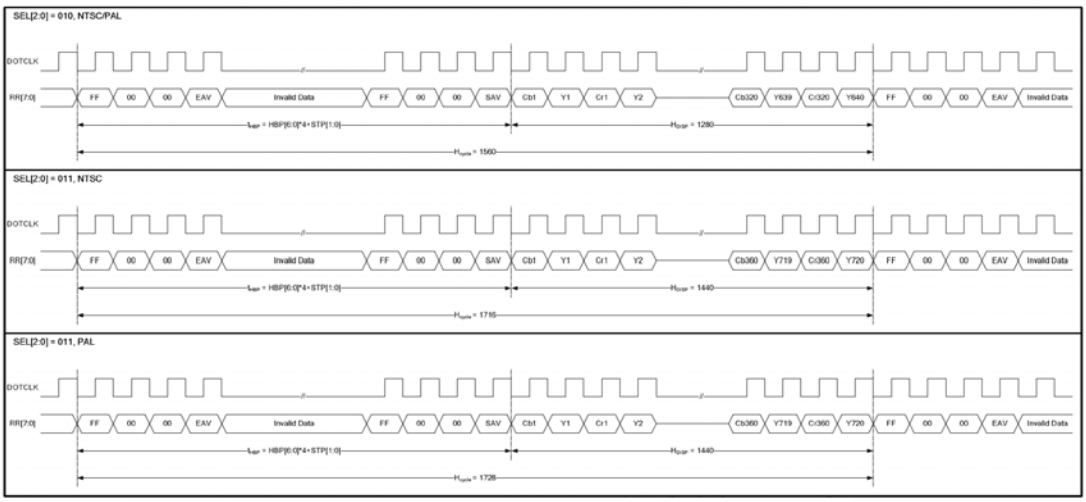


Figure 6 CCIR656 horizontal timing

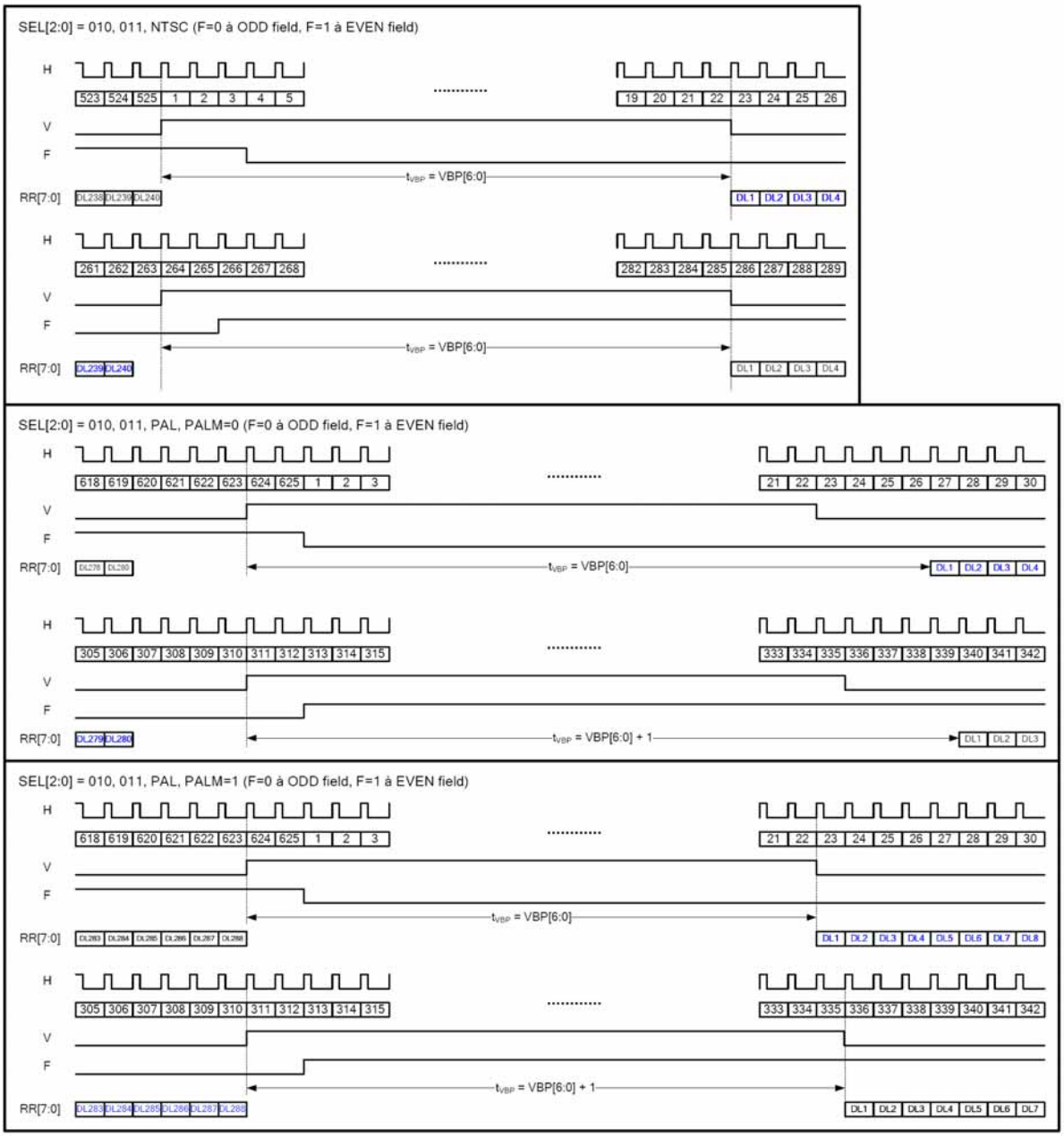


Figure 7 CCIR656 vertical timing

9.SERIAL INTERFACE

The SPI is available through the chip select line (SPENA), serial transfer clock line (SPCK), serial data input (SPDA).

The Driver IC recognizes the start of data transfer at the falling edge of SPENA input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of SPENA input. The Driver IC is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the Driver IC are compared and both 6-bit data correspond. The identification code must be 011100. Two different chip addresses must be assigned to the Driver IC because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When the RS = 1, instruction write. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

After receiving the start byte, the Driver IC starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted (9th SPCK started). All Driver IC instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (IB15 to 0---9th ~24th SPCK).

RS	RW	status
0	0	Write SPI address
0	1	Read gate line number(Note)
1	0	Write SPI data
1	1	Read SPI data

Table 1 RS & RW setting

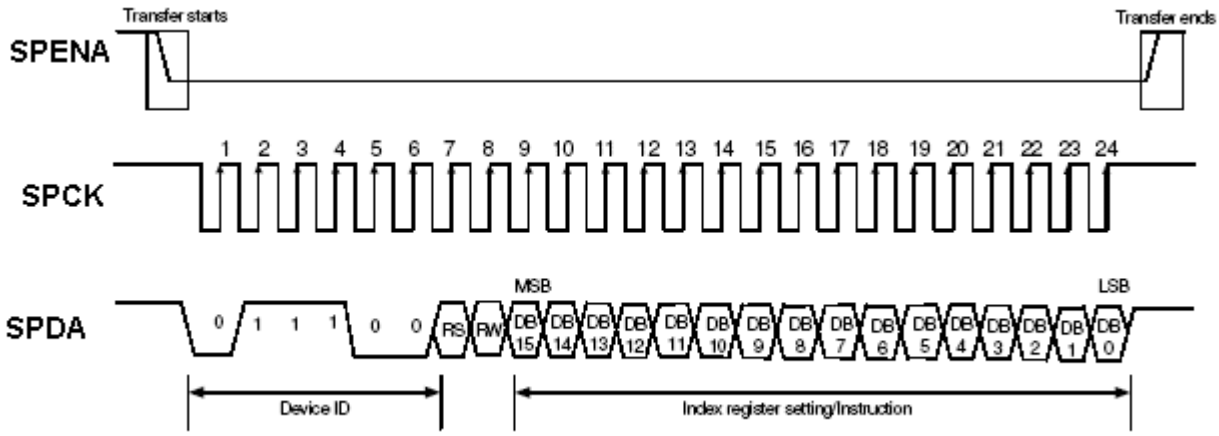
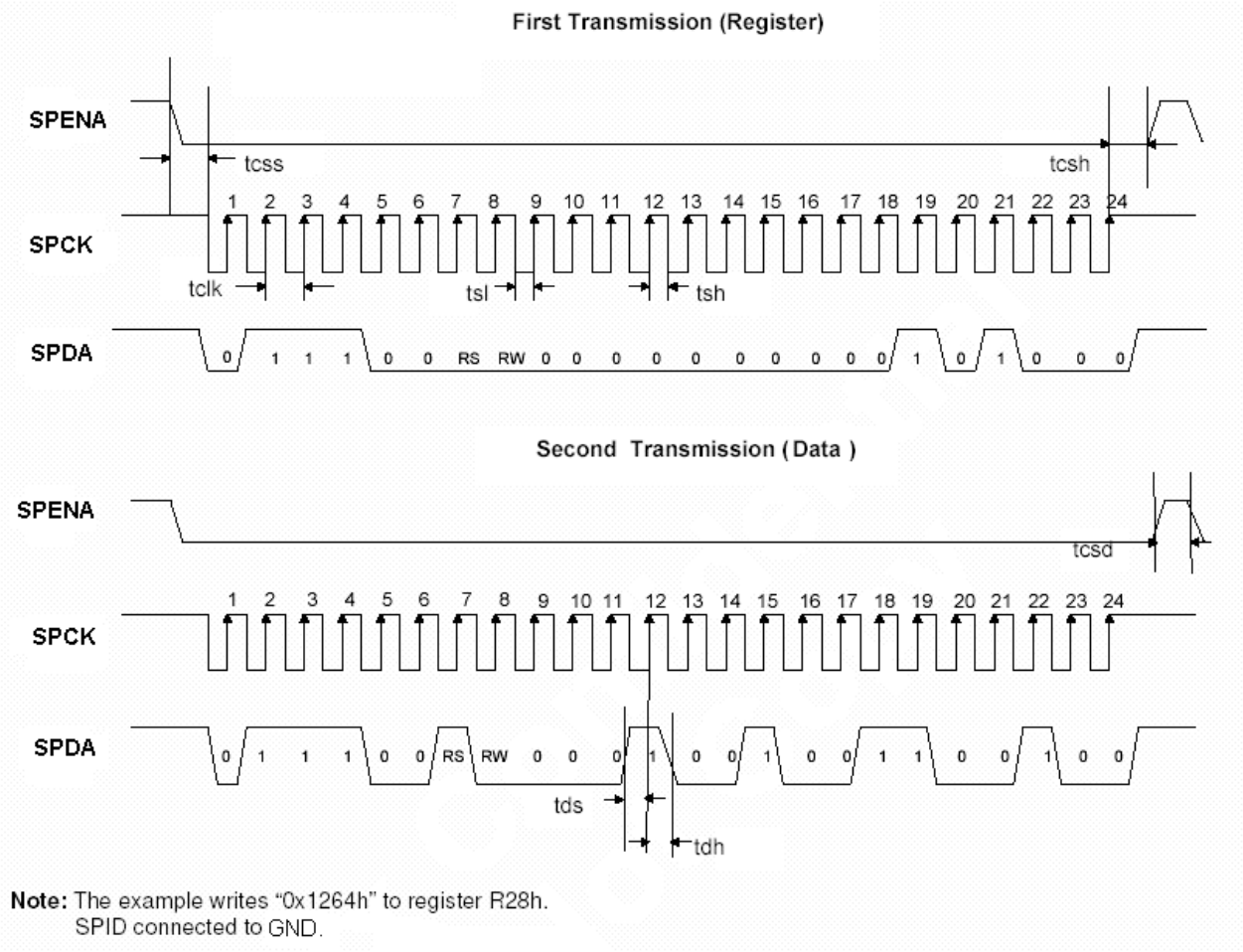


Figure 1 SPI Timing

Under the standard condition, the number of CLK is twenty-four units. After SPENA has transmitted twenty-four units of CLK, it has to change into High. When the number of CLK is less than 24 units, the data of SPI can't be downloaded. When the number of CLK is more than 25 units, the data of SPI will download the former data of the 24 units of CLK.

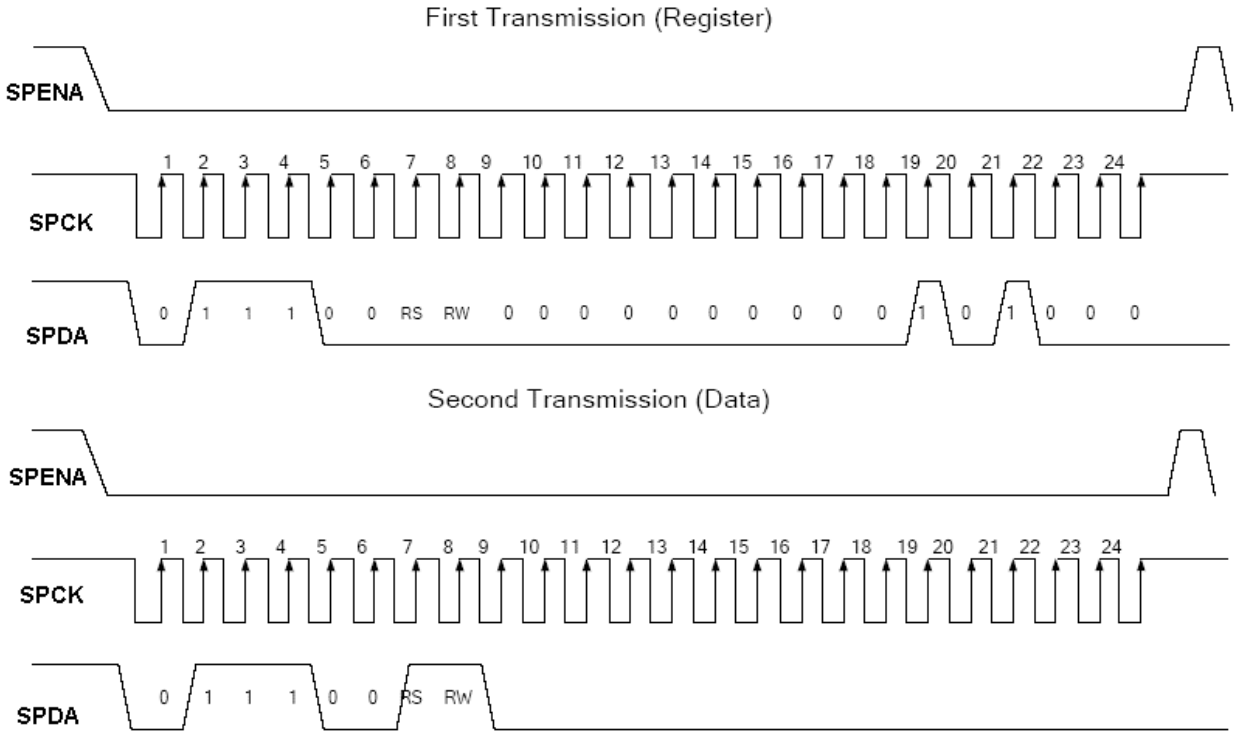
- **Write SPI**



Note: The example writes "0x1264h" to register R28h.
SPID connected to GND.

Figure 2 SPI interface Timing Diagram & W rite SPI Example

- **Read SPI**



Note: The example Read "0x1264h" from register R28h.

Figure 3 SPI interface Timing Diagram & Read SPI Example

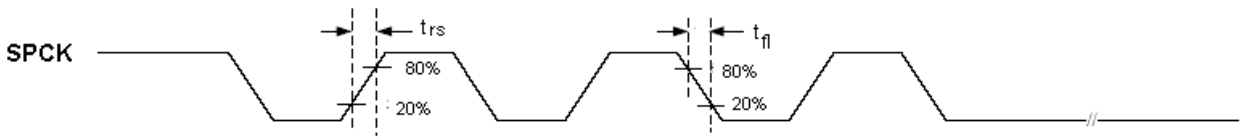


Figure 4 Rising/Falling time

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Clock Rising Time	trs	-	-	30	ns
Clock Falling Time	tfl	-	-	30	ns
Chip Select Setup Time	tcss	0	-	-	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

Table 2 SPI timing

10. COMMAND

10.1 Command Table

Reg#	Register	R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	PINV	BGR	SM	TB	CPE	0	0	0	0	0	0	0	0
R02h	LCD driver AC control	0	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	Do not setting																	
R04h	Data and color filter control	0	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	1	1	1
R05h	Function control	0	1	GHN	0	1	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	0	0	0	0	0
R06h	Reserved	Reserved																	
R07h	Reserved	Reserved																	
R0Ah	Contrast/ Brightness control	0	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0
R0Dh	Power control (3)	Do not setting																	
R0Eh	Power control (4)	Do not setting																	
R0Fh	Gate scan starting Position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R16h	Horizontal Porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0
R17h	Vertical Porch	0	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R1Eh	Power control (5)	Do not setting																	
R27h	Reserved	Reserved																	
R28h	Reserved	Reserved																	
R29h	Reserved	Reserved																	
R2Bh	Reserved	Reserved																	
R30h	γ control (1)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	γ control (9)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	γ control (10)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Software settings will override hardware pin (eg, BGR bits override BGR pin definition)

Table 1 Command table

10.2 Command description

Status Read

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 1 Status read

The status read instruction reads the internal status of the T–con IC.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RL	REV	PINV	BGR	SM	TB	0	0	0	0	0	0	0	0	0

Figure 2 Driver output control

REV: Displays all character and graphics display sections with reversal when REV = “0”. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below**.**

REV	RGB data	Source output level	
		VCOM = “H”	VCOM = “L”
0	00000H : 3FFFFH	V0 : V63	V63 : V0
1	00000H : 3FFFFH	V63 : V0	V0 : V63

Table 1 Source output level

PINV: When PINV=0, POL output is same phase with internal VCOM signal. When PINV=1, POL output phase is reversed with VCOM signal.

BGR: Selects the <R><G><B> arrangement. When BGR = “0” <R><G><B> color is assigned from S0.When BGR = “1” <B><G><R> color is assigned from S0.

SM: Change the division of gate driver. When SM = “0”, odd/even division (interlace mode) is selected. When SM = “1”, upper/lower division is selected. Select the division mode according to the mounting method.

TB: Selects the output shift direction of the gate driver. When TB = “1”, G0 shifts to G239. When TB = “0”, G239 shifts to G0.

RL: Selects the output shift direction of the source driver. When RL = “1”, S0 shifts to S959 and <R><G><B> color is assigned from S0. When RL = “0”, S959 shifts to S0 and <R><G><B> color is assigned from S959. Set RL bit and BGR bit when changing the dot order of R, G and B.

Note: The default setting of register bits **REV**, **BGR**, **TB** and **RL** are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.

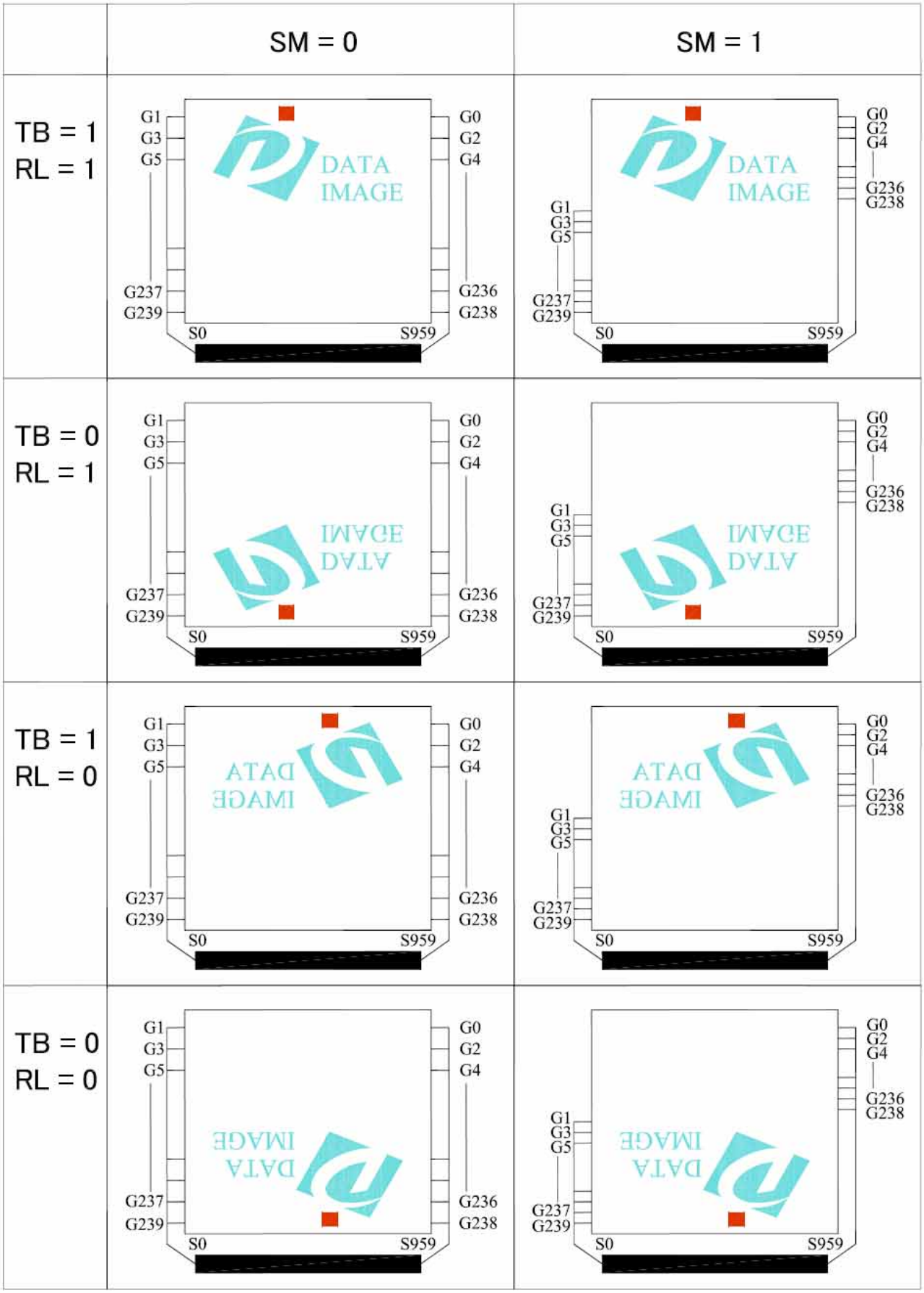


Figure 3 Scan direction & Display

LCD-Driving-Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B / C	0	0	0	0	0	0	0	0	0

Figure 4 LCD-driving-waveform control

B/C: When B/C = 0, frame inversion of the LCD driving signal is enabled. When B/C = 1, line inversion waveform is generated

Input Data and Color Filter Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	1	1	1

Figure 5 Input data and color filter control

SEL2-0: Define the input interface mode.

SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	Parallel-RGB data format	6.5MHz
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Table 2 Interface type

OEA1-0: Odd/Even filed advanced function.

OEA1	OEA0	
0	0	Display Start @ VBP delay for Odd field and @ ***VBP-1*** for Even field.
0	1	Display Start @ VBP delay for Odd field and @ ***VBP*** for Even field.
1	0	Display Start @ VBP delay for Odd field and @ ***VBP+1*** for Even field.
1	1	No use

Table 3 Odd/Even filed advanced function.

BLT[1:0]: Set the initial power on black image insertion time.

00: 10 fields
01: 20 fields
10: 40 fields
11: 80 fields

PALM: Set the input data line number in PAL mode

0: 280 lines
1: 288 lines

Function Control (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GHN	0	1	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	0	0	0	0	0

Figure 6 Function control

DIT: When DIT=0, dithering function is turned off. When DIT=1, dithering function is enabled.
DEO: When DEO=0, VSYNC/HSYNC are also needed in DE mode. Under this condition, vertical back porch is defined by VBP[6:0] and the horizontal first valid data is defined by DE signal. When DEO=1, only DEN signal is needed in DE mode.
HSP: When HSP=0, HSYNC is negative polarity. When HSP=1, HSYNC is positive polarity.
VSP: When VSP=0, VSYNC is negative polarity. When VSP=1, VSYNC is positive polarity.
CKP: When CKP=0, data is latched in DCLK falling edge. When CKP=1, data is latched by DCLK rising edge.
DEP: When DEP=0, DEN is negative polarity active. When DEP=1, DEN is positive polarity active.
LPF: When LPF=0, the low pass filter function in YUV mode is disabled. When LPF=1, the low pass filter function is YUV mode is enabled.
GHN: When GHN=0, all gate outputs are forced to VGH. When GHN=1, gate driver is normal operation.

Contrast/Brightness Control (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0

Figure 7Contrast/Brightness control

CON4-0: Display Contrast level adjustment. (0.125/step) Adjust range from 00h (level = 0) to 1Fh (level = 3.875). Default value is 08h (level = 1).
BR6-0: Display Brightness level adjustment. (2/step) Adjust range from 00h (level = -128) to 7Fh (level = +126). Default value is 40h (level = 0).

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0

Figure 8 Frame cycle control

NO1-0: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	1.5 us
0	1	3 us
1	0	4.5 us
1	1	6 us

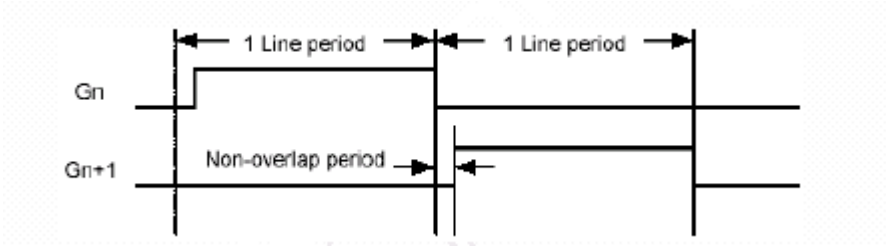


Figure 9 NO timing diagram

SDT1-0: Set delay amount from the gate output signal falling edge to the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	1 us
0	1	3 us
1	0	5 us
1	1	7 us

Table 4 Delay amount of the source output

EQ2-0: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	3 us
0	1	0	4 us
0	1	1	5 us
1	0	0	6 us
1	0	1	7 us
1	1	0	8 us
1	1	1	9 us

Table 5 EQ period

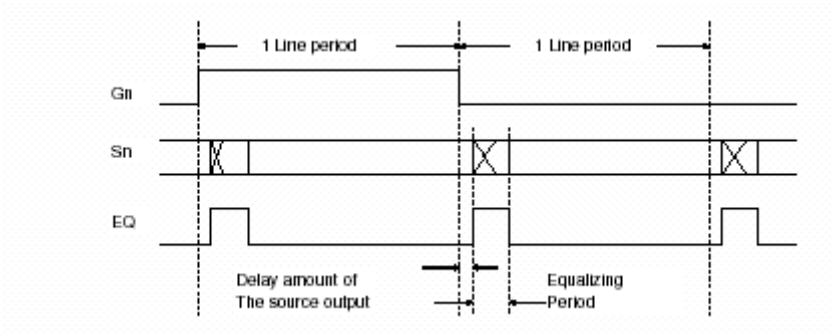


Figure 10 EQ timing diagram

Gate Scan Position (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 11 Gate scan position

SCN8-0: Set the scanning starting position of the gate driver.

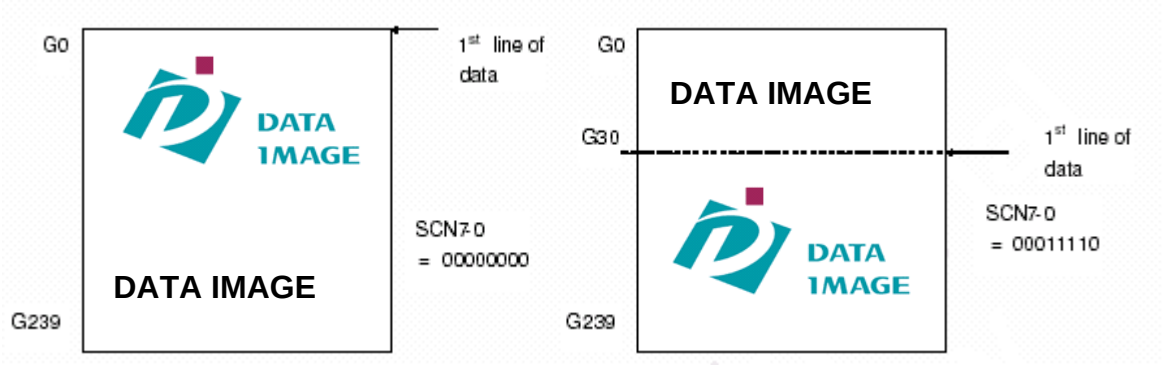


Figure 12 Gate scan display position

Horizontal Porch (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0

Figure 13 Horizontal Porch

XLIM8-0: Set the number of valid pixel per line.

XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				:					:
				:					Step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

Table 6 No. of pixel per line

Vertical Porch (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 14 Vertical porch

HBP6-0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XLIM8-0 and before the first valid data will be treated as dummy data. The setting is only effective in SYNC mode timing.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle		
							Parallel	Serial	YUV
0	0	0	0	0	0	0	Can't set		
0	0	0	0	0	0	1	Can't set		
0	0	0	0	0	1	0	Can't set		
0	0	0	0	0	1	1	Can't set		
0	0	0	0	1	0	0	Can't set		
0	0	0	0	1	0	1	Can't set		
0	0	0	0	1	1	0	Can't set		
0	0	0	0	1	1	1	Can't set		
0	0	0	1	0	0	0	Can't set		
0	0	0	1	0	0	1	9	27	36
0	0	0	1	0	1	0	10	30	40
							: Step = 1 :	: Step = 3 :	: Step = 4 :
1	1	1	1	1	1	0	126	378	504
1	1	1	1	1	1	1	127	381	508

Table 7 No. of clock cycle of clock

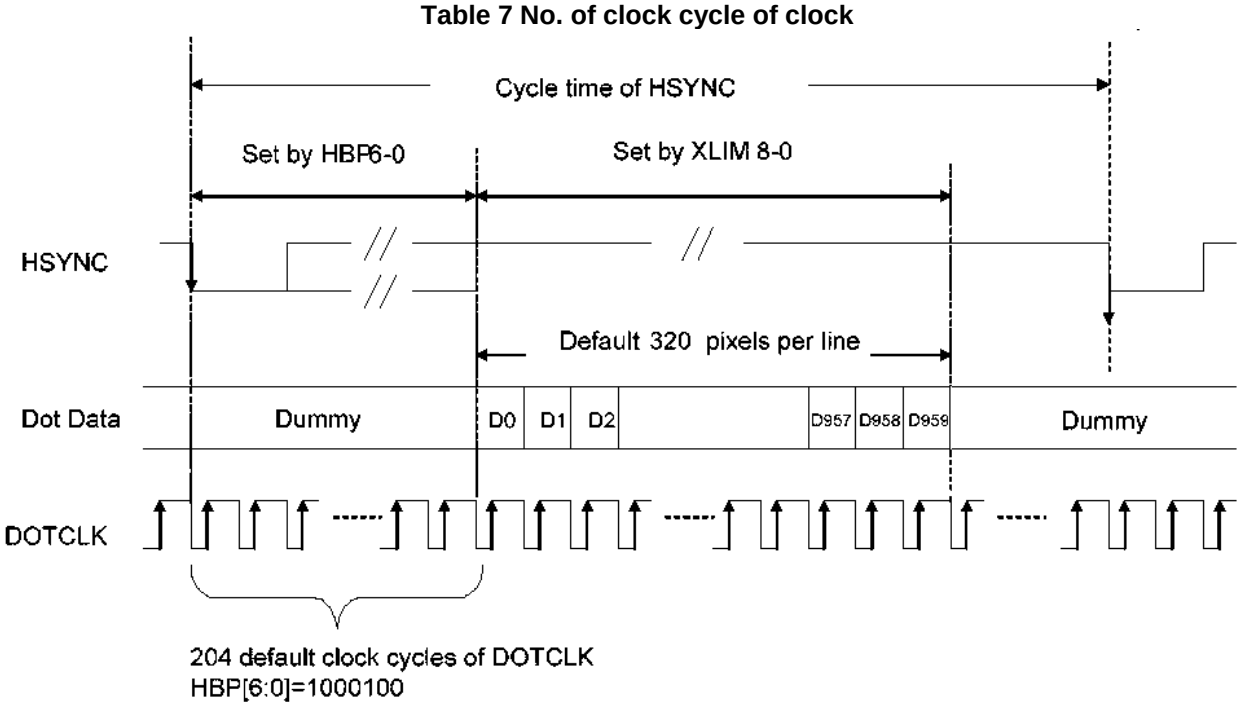


Figure 15 No. of clock cycle of clock

STH1-0: Adjust the first valid data by dot clock. This setting is not valid in parallel RGB input interface.
STH = 00: +0 dot clock
STH = 01: +1 dot clock
STH = 10: +2 dot clock
STH = 11: +3 dot clock

VBP6-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line. The setting is only effective in SYNC mode timing.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
			:				: Step = 1 :
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 8 No. of clock cycle of HSYNC

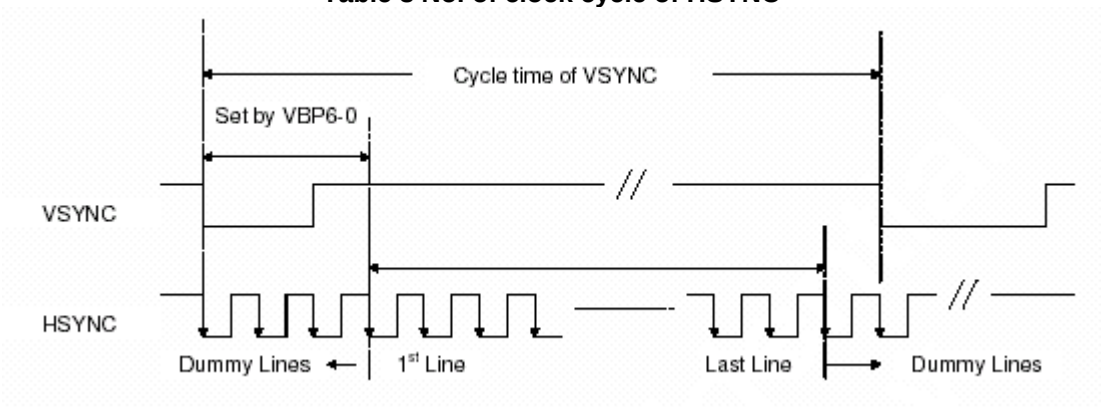


Figure 16 No. of clock cycle of HSYNC

Gamma Control 1 (R30h to R37h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1	PKP1	PKP1	0	0	0	0	0	PKP0	PKP0	PKP0
W	1	0	0	0	0	0	PKP3	PKP3	PKP3	0	0	0	0	0	PKP2	PKP2	PKP2
W	1	0	0	0	0	0	PKP5	PKP5	PKP5	0	0	0	0	0	PKP4	PKP4	PKP4
W	1	0	0	0	0	0	PRP1	PRP1	PRP1	0	0	0	0	0	PRP0	PRP0	PRP0
W	1	0	0	0	0	0	PKN1	PKN1	PKN1	0	0	0	0	0	PKN0	PKN0	PKN0
W	1	0	0	0	0	0	PKN3	PKN3	PKN3	0	0	0	0	0	PKN2	PKN2	PKN2
W	1	0	0	0	0	0	PKN5	PKN5	PKN5	0	0	0	0	0	PKN4	PKN4	PKN4
W	1	0	0	0	0	0	PRN1	PRN1	PRN1	0	0	0	0	0	PRN0	PRN0	PRN0

Figure 17 Gamma control 1

PKP52–00: Gamma micro adjustment registers for the positive polarity output.
PRP12-00: Gradient adjustment registers for the positive polarity output.
PKN52-00: Gamma micro adjustment registers for the negative polarity output.
PRN12-00: Gradient adjustment registers for the negative polarity output.

Gamma Control 2 (R3Ah to R3Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

Figure 18 Gamma control 2

VRP14-00: Adjustment registers for amplification adjustment of the positive polarity output.
VRN14-00: Adjustment registers for the amplification adjustment of the negative polarity output.
(Refer to Gamma Adjustment Function for details)

10.3 SPI Setting Code

Reg#	Hex Code	Register Bit Value
R01h	XX00	RL = X REV = X PINV = X BGR = X SM = “0” TB = X
R02h	0200	B/C = “1”
R03h		Do not setting
R04h	04XX	PALM = “1” BLT = ”00” OEA = **Note(2)** SEL = X
R05h		GHN=”1” LPF=”1” DEP=”0” CKP=”1” VSP= **Note(2)** HSP=”0” DEO=”1” DIT=”1”
R0Ah	4008	BR = “1000000” CON = “01000”
R0Bh	D400	NO = “11” SDT = “01” EQ = “100”
R0Dh		Do not setting
R0Eh		Do not setting
R0Fh	0000	SCN = “00000000”
R16h	9F80	XLIM = “100111111”
R17h		STH = “00” HBP = **Note(2)** VBP = **Note(2)**
R1Eh		Do not setting
R30h	0000	PKP1 = “000” PKP0 = “000”
R31h	0407	PKP3 = “100” PKP2 = “111”
R32h	0202	PKP5 = “010” PKP4 = “010”
R33h	0000	PRP1 = “000” PRP0 = “000”
R34h	0505	PKN1 = “101” PKN0 = “101”
R35h	0003	PKN3 = “000” PKN2 = “011”
R36h	0707	PKN5 = “111” PKN4 = “111”
R37h	0000	PRN1 = “000” PRN0 = “000”
R3Ah	0904	VRP1 = “01001” VRP0 = “0100”
R3Bh	0904	VRN1 = “01001” VRN0 = “0100”

Note: (1) X means the bit is refer to the logic stage of the corresponding hardware pin.
(2) The default values of the VSP 、OEA、HBP、VBP are automatically set by SEL.

Default Value auto setting			VSP	OEA[1:0]	HBP[6:0]	VBP[6:0]
SEL[2:0] = 000	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 001	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 010	NTSC		0	01	1000101	0010110
	PAL	PALM=0	0	10	1000101	0011100
		PALM=1				0011000
SEL[2:0] = 011	NTSC		0	01	1000100	0010110
	PAL	PALM=0	0	10	1000111	0011100
		PALM=1				0011000
SEL[2:0] = 100	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100
SEL[2:0] = 101	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 110	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 111	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100

Table 1 Registers Default Value

11.GAMMA ADJUSTMENT FUNCTION

The IC incorporates gamma adjustment function for the 262K-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

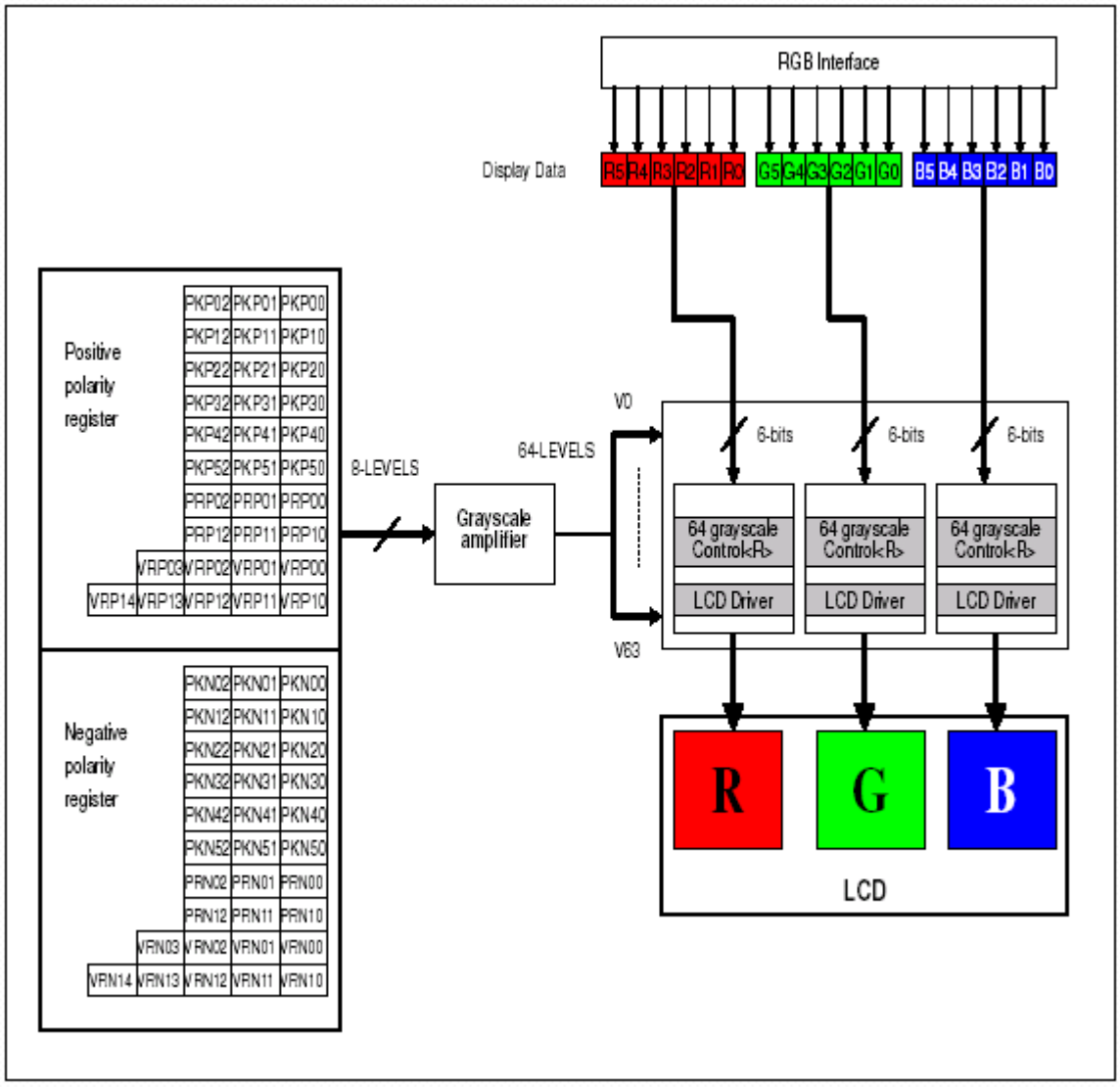


Figure 1 Grayscale control block

11.1 Structure of Grayscale Amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.

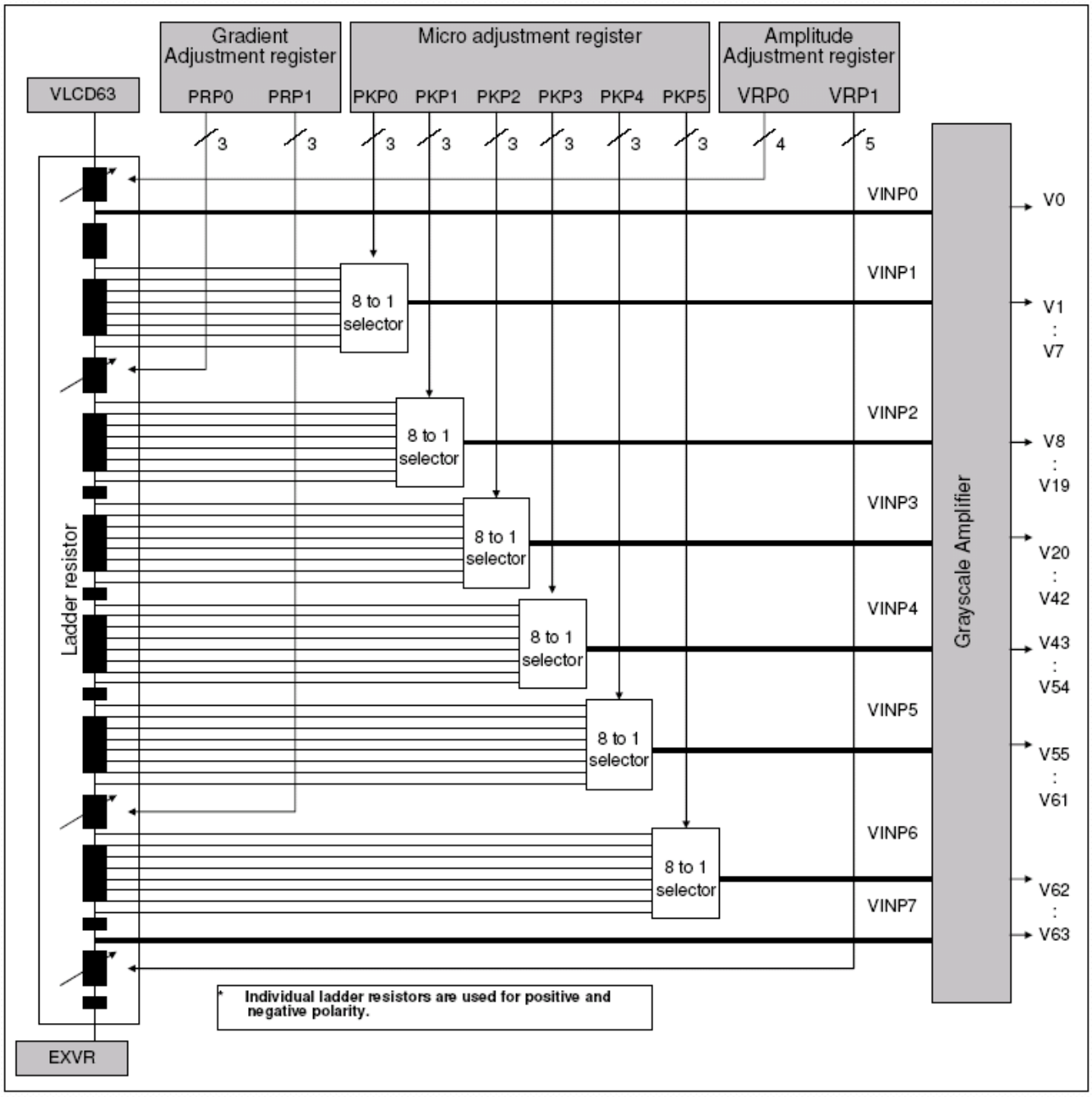


Figure 1 Grayscale amplifier

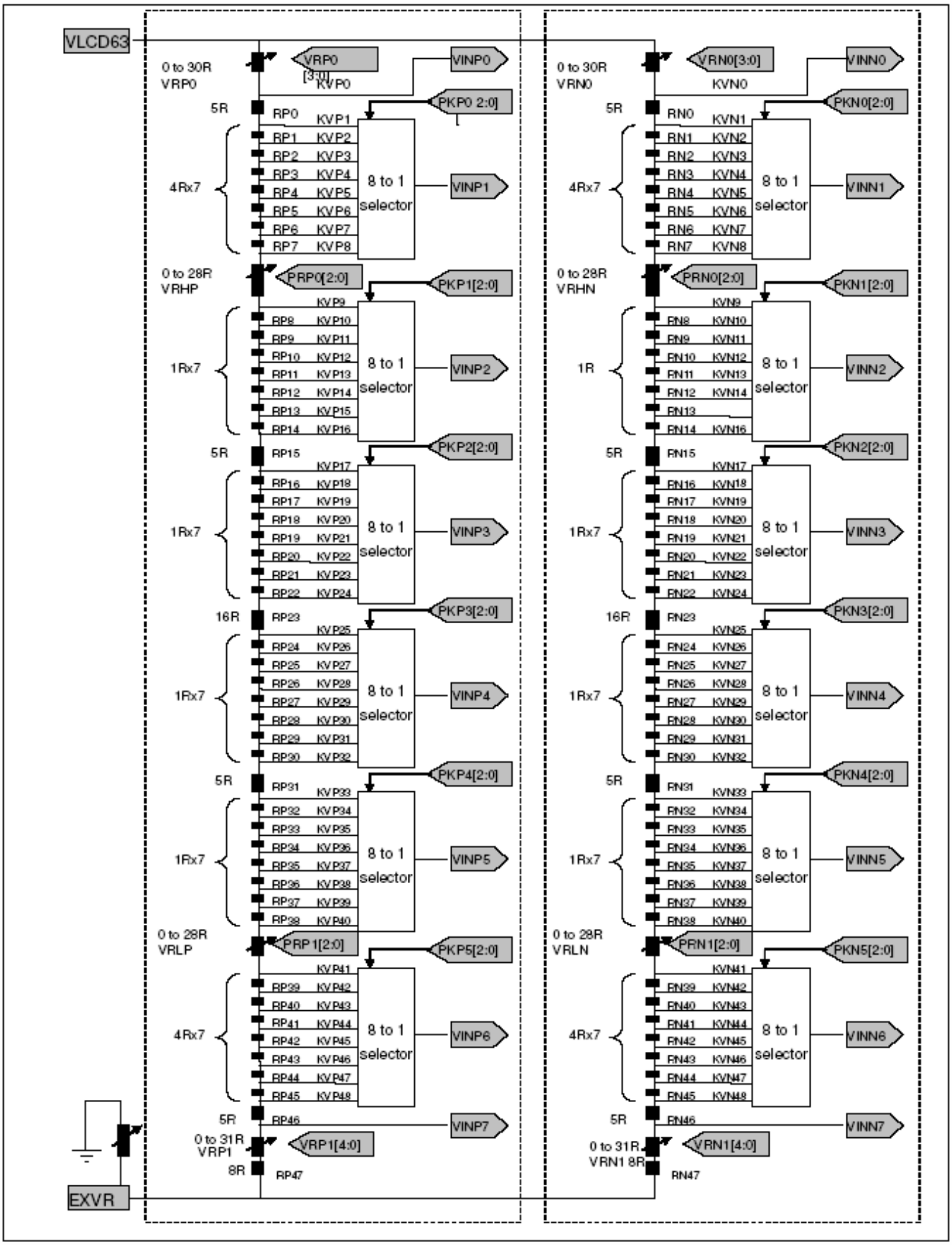


Figure 2 Resistor Ladder for Gamma Voltages Generation

11.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) following graphics indicates the operation of each adjusting register.

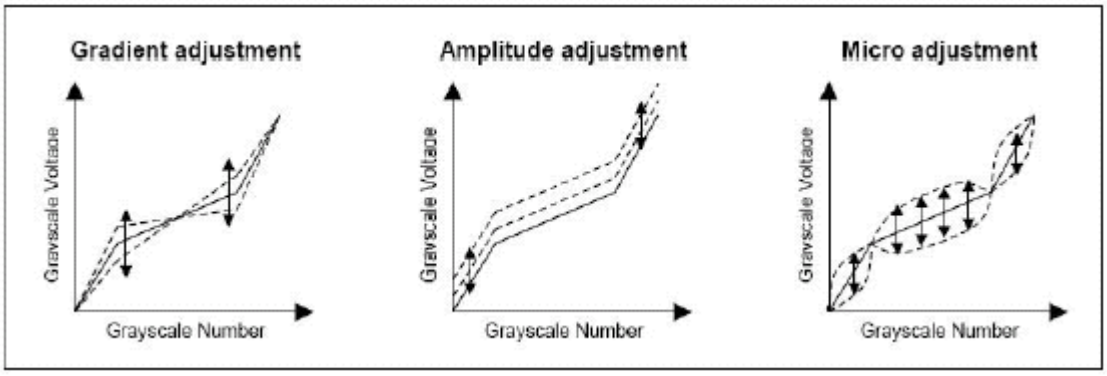


Figure 1 Gamma adjustment function

11.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

11.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

11.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

11.3 Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors. Also, there has pin (EXVR) that can be connected to GND or an external variable resistor for compensating the dispersion of length between one panel to another.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 1 PRP(N)

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
: Step=2R :	
1110	28R
1111	30R

Table 2 VRP(N)0

VRP(N)1	Resistance
0000	0R
0001	1R
0010	2R
: Step=1R :	
1110	28R
1111	30R

Table 3 VRP(N)1

8 to 1 Selector

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor.

Following figure explains the relationship between the micro adjusting register and the selecting voltage.

Positive polarity							**Negative polarity**						
Register	**Selected voltage**						**Register**	**Selected voltage**					
PKP[2:0]	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6	**PKN[2:0]**	VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Table4 PKP and PKN

12.OPTICAL CHARACTERISTIC

12.1. Specification:

Ta = 25°C

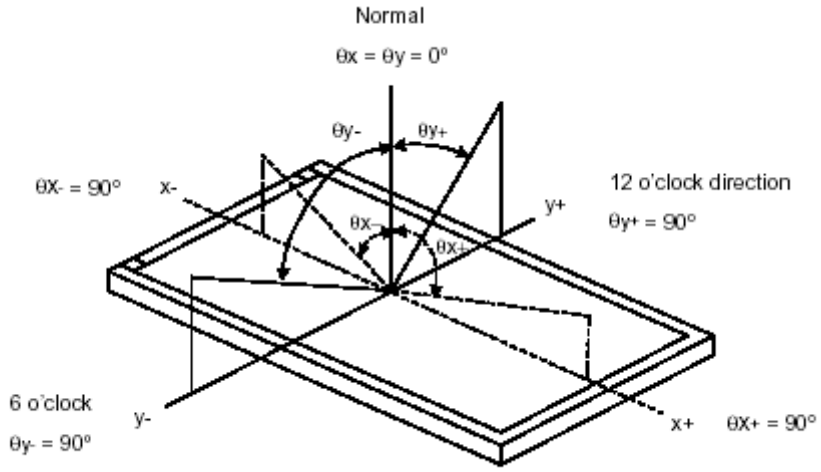
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ_x+	Center CR≥10		(70)		deg	Note 12-2
		θ_x-			(70)		deg	
	Vertical	θ_Y+			(50)		deg	
		θ_Y-			(70)		deg	
Contrast Ratio		CR		200				Note 12-1
Response time	Rise	Tr	Center θx=θy =0°		15	30	ms	Note 12-4
	Fall	Tf			35	50	ms	
Uniformity		U		70	--		%	
Brightness			Center θx=θy =0°	200	250	--	cd/m^2	Note 12-2
Chromaticity	White	x		0.28	0.31	0.36		Note 12-2
		y		0.27	0.32	0.37		

Note 12-1:CR = $\frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

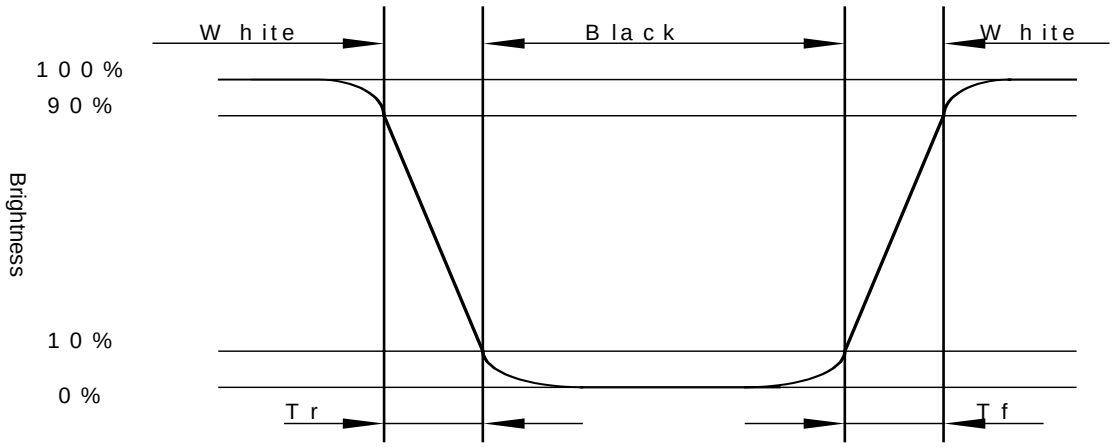
Contrast Ratio is measured in optimum common electrode voltage.
The test configurations of contrast ratio see section 12-2 .

Note 12-2: 1.Topcon BM-7A luminance meter 1.0° field of view is used in the testing (after 2 minutes operation).
2. LED current =40mA.

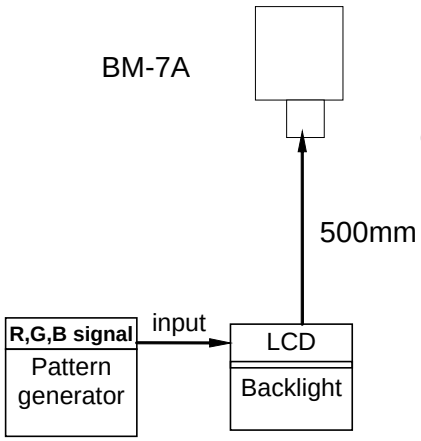
Note 12-3 : The definitions of viewing angles diagrams:



Note 12-4: The definition of response time:

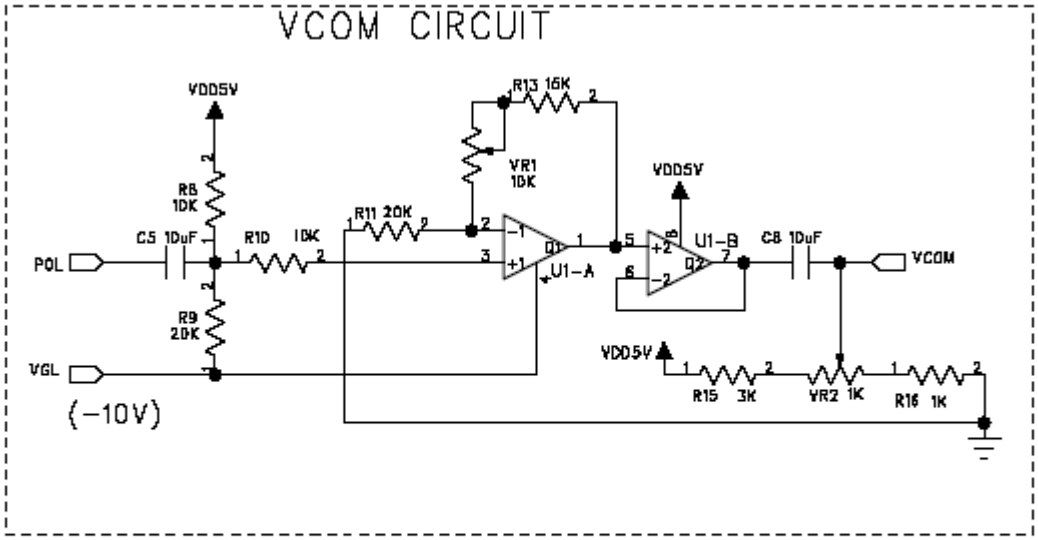


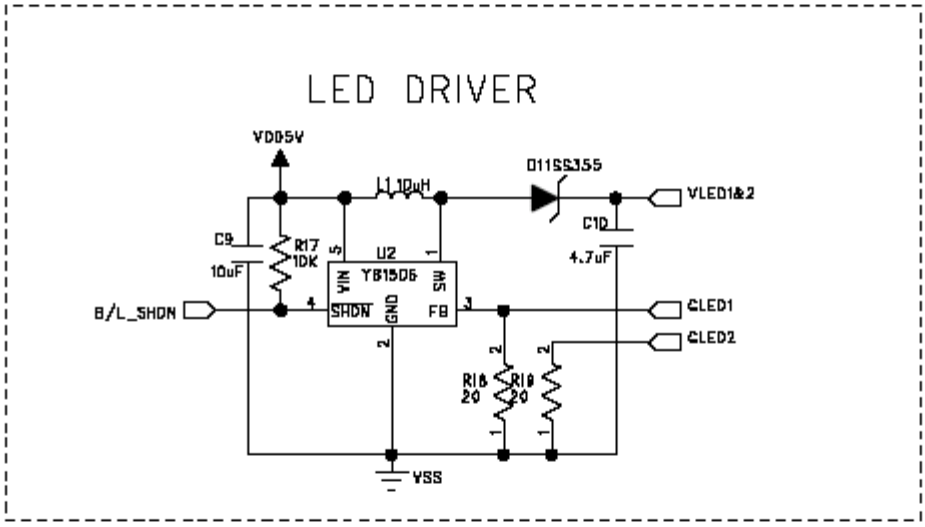
12.2. Testing configuration

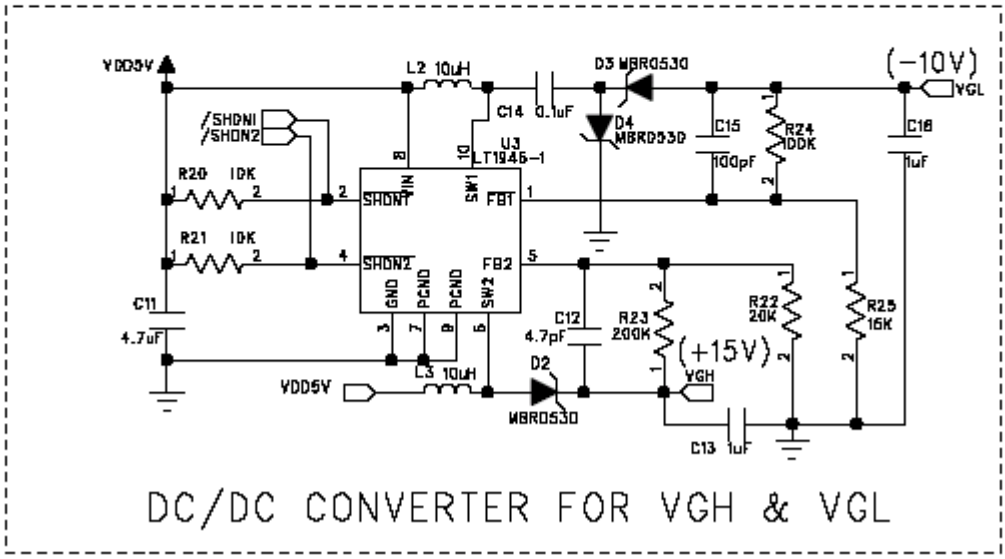


Caution: 1. Environmental illumination≦1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

13.APPLICATION CIRCUIT







14.QUALITY ASSURANCE

14.1 Test Condition

14.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 20 ± 5°C
Humidity : 65 ± 5%

14.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

14.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

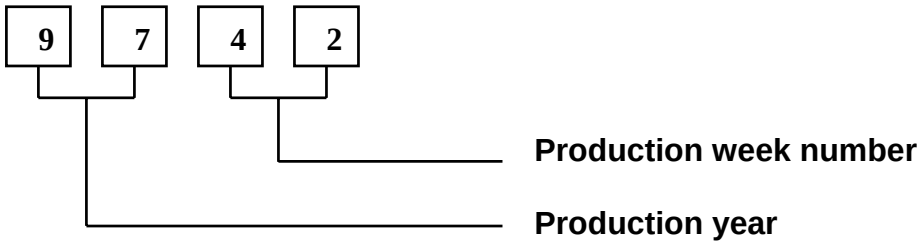
14.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

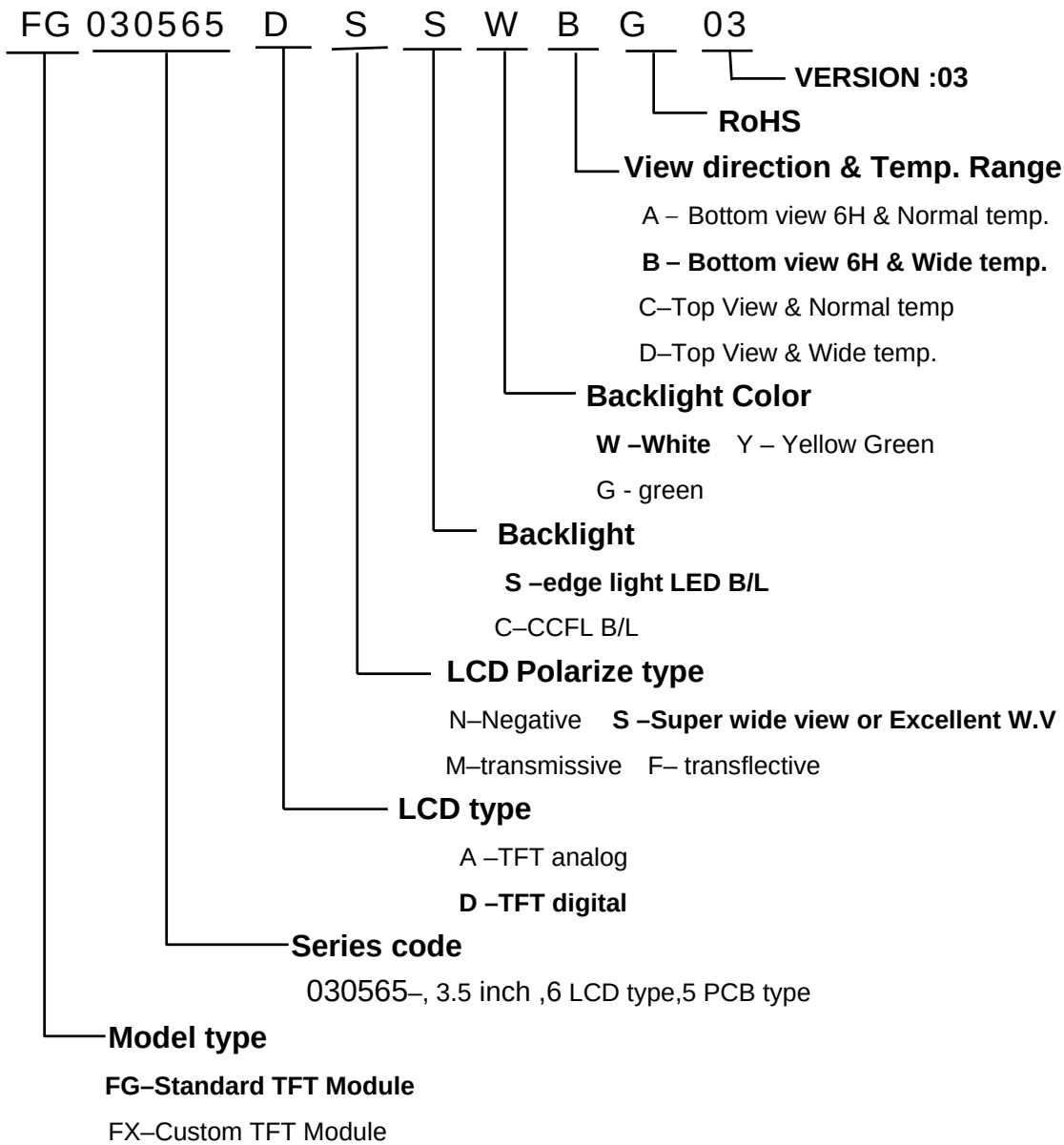
14.1.5 Test Method

No.	Reliability Test Item & Level	Test Level
1	High Temperature Storage Test	T=80°C,240hrs
2	Low Temperature Storage Test	T=-30°C,240hrs
3	High Temperature Operation Test	T=70°C,240hrs
4	Low Temperature Operation Test	T=-20°C,240hrs
5	High Temperature and High Humidity Operation Test	T=60°C,90% RH,240hrs
6	Temperature Cycle Test (No operation)	-30°C → +25°C → +80°C,50 Cycles 30 min 5min 30 min
7	Vibration Test (No operation)	Frequency:10 ~ 55 Hz Amplitude:1.0 mm Sweep Time:11min Test Period:6 Cycles for each Direction of X,Y,Z
8	Shock Test (No operation)	100G, 6ms Direction：± X,± Y,± Z Cycle：3 times

15.LOT NUMBERING SYSTEM



16.LCM NUMBERING SYSTEM



17.PRECAUTIONS IN USE LCM

1. LIQUID CRYSTAL DISPLAY (LCD)

LCD is made up of glass, organic sealant, organic fluid, and polymer based polarizers. The following precautions should be taken when handing,

(1). Keep the temperature within range of use and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel off or bubble.

(2). Do not contact the exposed polarizers with anything harder than an HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin.

(3). Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.

(4). Glass can be easily chipped or cracked from rough handling, especially at corners and edges.

(5). Do not drive LCD with DC voltage.

2. Liquid Crystal Display Modules

2.1 Mechanical Considerations

LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.

(1). Do not tamper in any way with the tabs on the metal frame.

(2). Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.

(3). Do not touch the elastomer connector, especially insert an backlight panel (for example, EL).

(4). When mounting a LCM make sure that the PCB is not under any stress such as bending or twisting . Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.

(5). Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.

2.2. Static Electricity

LCM contains CMOS LSI's and the same precaution for such devices should apply, namely

(1). The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.

(2). The modules should be kept in antistatic bags or other containers resistant to static for storage.

(3). Only properly grounded soldering irons should be used.

(4). If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.

(5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.

(6). Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.

2.3 Soldering

(1). Solder only to the I/O terminals.

(2). Use only soldering irons with proper grounding and no leakage.

(3). Soldering temperature : 280°C ± 10°C

(4). Soldering time: 3 to 4 sec.

(5). Use eutectic solder with resin flux fill.

(6). If flux is used, the LCD surface should be covered to avoid flux spatters. Flux residue should be removed after wards.

2.4 Operation

(1). The viewing angle can be adjusted by varying the LCD driving voltage V0.

(2). Driving voltage should be kept within specified range; excess voltage shortens display life.

(3). Response time increases with decrease in temperature.

(4). Display may turn black or dark blue at temperatures above its operational range; this is (however not pressing on the viewing area) may cause the segments to appear "fractured".

(5). Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured".

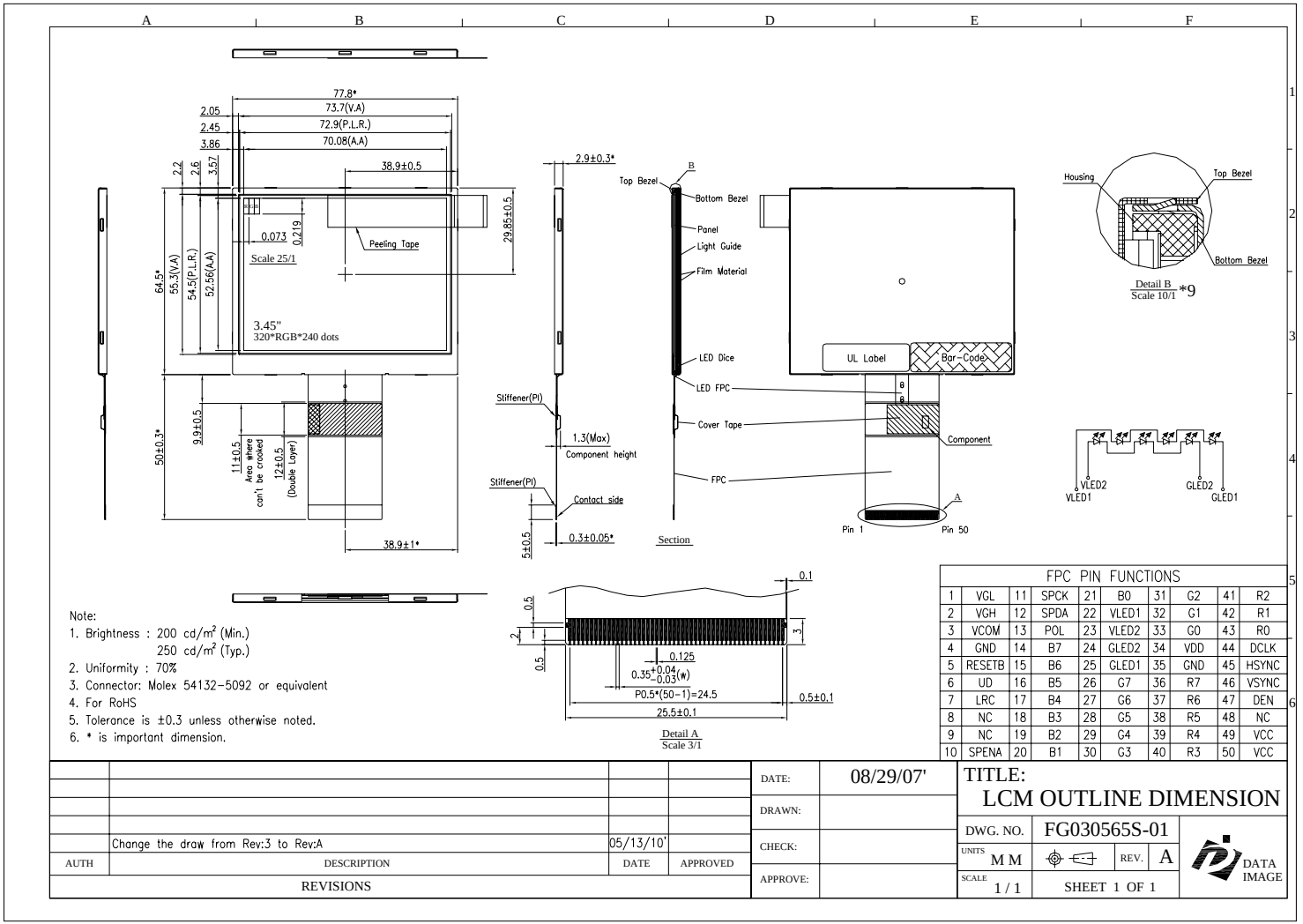
2.5 Storage

If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all the time.

2.6 Limited Warranty

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events.

18.OUTLINE DRAWING



Note:
1. Brightness : 200 cd/m² (Min.)
   250 cd/m² (Typ.)
2. Uniformity : 70%
3. Connector: Molex 54132-5092 or equivalent
4. For RoHS
5. Tolerance is ±0.3 unless otherwise noted.
6. * is important dimension.

FPC PIN FUNCTIONS

1	VGL	11	SPCK	21	B0	31	G2	41	R2
2	VGH	12	SPDA	22	VLED1	32	G1	42	R1
3	VCOM	13	POL	23	VLED2	33	G0	43	R0
4	GND	14	B7	24	GLED2	34	VDD	44	DCLK
5	RESETB	15	B6	25	GLED1	35	GND	45	HSYNC
6	UD	16	B5	26	G7	36	R7	46	VSYNC
7	LRC	17	B4	27	G6	37	R6	47	DEN
8	NC	18	B3	28	G5	38	R5	48	NC
9	NC	19	B2	29	G4	39	R4	49	VCC
10	SPENA	20	B1	30	G3	40	R3	50	VCC

AUTH	DESCRIPTION	DATE	APPROVED
	Change the draw from Rev:3 to Rev:A	05/13/10'	

REVISIONS

DATE: 08/29/07'
DRAWN:
CHECK:
APPROVE:

TITLE: LCM OUTLINE DIMENSION

DWG. NO. FG030565S-01
UNITS M M
REV. A
SCALE 1 / 1
SHEET 1 OF 1

DATA IMAGE

19.PACKAGE INFORMATION

Material

1 Carton + 2 Anti-static bag + 2 Form(15mm) + 1 Form(35mm)
+ 20 Anti-static tray + 2 Drier + 2 Antirust

Total pcs

1 Antistatic tray = 8 panel pcs
1 Anti-static bag = 9 Anti-static tray + cover tray = 9*8 +1*0 = 72 pcs
1 Carton = 2 Anti-static bag = 2*72 = 144 pcs
1 Carton = 144 pcs
Carton size : 485L x 282W x 279H (mm)
Total Weight ±8.5 kgw

FG030565 TFT LCM PACKING