DATA IMAGE CORPORATION

TFT Module Specification

Preliminary

ITEM NO.: FG030561DSSWBG04

Table of Contents

Customer Companies	QA Approval	QA Check	R&D Approval	R&D Check
	pretty	Seven	Gomer	Levi
Approved by	Version:	Issued Date:	Sheet Code:	Total Pages:
	7	14/DEC/15'		55

2. RECORD OF REVISION

Rev	Date	Item	Page	Comment	Source
1	25/SEP/07			Initial PRELIMINARY	ESR9609016
2	9/JAN/08	6 6 6 6 12 10	4 4 4 4 41,42 20,25,35	1. Change VCOM Voltage. VCOMH, VCOML, VCOM-AC, VCOM-DC. 2. Add I_{VDDIO} , I_{VCI} , and I_{VCIP} operating current 3. Change LED voltage. 4. Add LED Dice Life Time 40000 Hours typ. 5. Change APPLICATION CIRCUIT 6.Modify: COMMAND DESCRIPTION	11S-7C0042
3	19/MAY/08	9 10 6	8~19 31~32 4	Modify: AC CHARACTERISTICS Modify: Vertical Porch (R17h) Change VCOM-AC, VCOM-DC, VCOMH, VCOML	11S-850011
4	26/MAR/09	8 12	6 41	Modify: SDO Pin terminals Modify: Application circuit	11S-930024
5	29/MAR/11’	16 18	48 50	1. Modify: LCM PRODUCT LABEL DEFINE; 2. Update the OUTLINE DRAWING.	11S-990032
6	02/OCT/13’	13 15.1.5 15.2 15.3	43 47 47 48	1. Modify Viewing Angle. 2. Add Test Method Remark. 3. Add Judgment standard. 4. Add Inspection condition.	110-DA0005
7	14/DEC/15’	6.2 13 15.1.5 15.4 18	4 43 47 50 44	Modify LED Back-light Driving Section Modify OPTICAL CHARACTERISTIC Update Test Method Update Sampling table Modify OUTLINE DRAWING from Rev 2 to 3.	11S-FB0001

3. FEATURES

- Support CCIR656/CCIR601 8 bit format or 8 bit serial RGB.
- Support the SPI commands setting, the operation parameters setting internally.
- Our components and processes are compliant to RoHS standard
- Support Contrast/Brightness control.
- On-chip voltage generator.
- On-chip DC-DC converter up to 6x / -6x.
- Programmable gamma correction curve.
- Non-Volatile Memory (OTP) for VCOM calibration

4. GENERAL SPECIFICATIONS

Parameter		Specifications	Unit
Screen Size		3.45” (diagonal)	inch
Surface Treatment		Anti-Glare	
Display Format		320 X RGB X 240	dots
Active Area		70.08 (W) x 52.56 (H)	mm
Pixel Pitch		0.219(W) x 0.219 (H)	mm
Pixel Configuration		Stripe	
Outline Dimension		77.8 (W) x 64.5 (H) x 4(T)	mm
Weight		42	g
View Angle direction		6 o’clock	
Temperature Range	Operation	-20~60	°C
	Storage	-30~70	°C

5. ABSOLUTE MAXIMUM RATINGS

(VSS=0V)

Parameter	Symbol	MIN.	MAX.	Unit
Power supply voltage (1)	VDDIO	-0.3	+4.0	V
Power supply voltage (2)	VDD	-0.3	+2.7	V
Input voltage	VCI	-0.3	+5.0	V

Note:

*All of the voltages listed above are with respective to VSS= 0V.

*Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

6. ELECTRICAL CHARACTERISTICS

6.1 DC Electrical Characteristics

(Unless otherwise specified, Voltage Referenced to $V_{SS=0V}$, V_{DDIO} = 3.3V, Ta = 25℃)

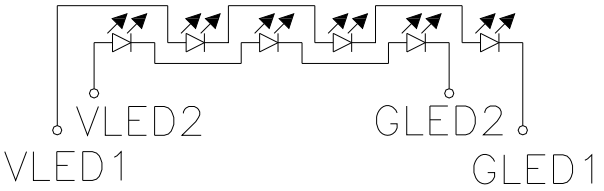
Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{DDIO}	Power supply pin of the logic block	Recommend Operating Voltage Possible Operating Voltage	2.5	3.3	3.6	V
I_{VDDIO}	I_{VDDIO} operating current	VDDIO = 3.3 V	--	0.18	0.25	mA
V_{CI}	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	VDDIO	3.3	3.6	V
I_{VCI}	I_{VCI} operating current	VCI = 3.3 V	--	9.5	12	mA
V_{CIP}	Voltage supply pin for analog circuit		V_{CI}	V_{CI}	V_{CI}	V
I_{VCIP}	I_{VCIP} operating current	VCIP = 3.3 V	--	20	22	uA
V_{COMH}	VCOM High Output Voltage		3.5	3.9	4.3	V
V_{COML}	VCOM Low Output Voltage		-1.7	-1.3	-0.9	V
VCOM	VCOM-AC		-	5.1	-	V_{P-P}
	VCOM-DC		-	1.3	-	V
V_{OH1}	Logic High Output Voltage	I out = -100μA	0.9*V_{DDIO}	-	V_{DDIO}	V
V_{OL1}	Logic Low Output Voltage	I out = 100μA	0	-	0.1*V_{DDIO}	V
V_{IH1}	Logic High Input voltage		0.8*V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*V_{DDIO}	V
VGH	Gate driver High Output Voltage		-	+15	-	V
VGL	Gate driver Low Output Voltage		-	-10	-	V

6.2 LED Back-light Driving Section

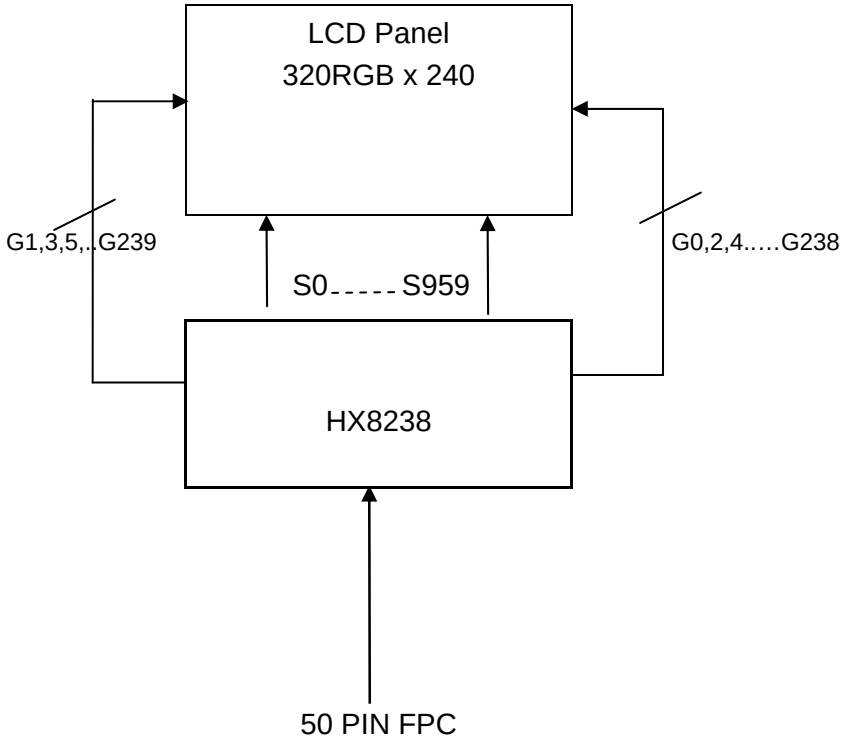
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V_L	7.8	8.7	10.2	V	I_L=40 mA Ta= 25 °C
LED current	I_L	--	40	--	mA	Ta= 25 °C
LED Dice Life Time		--	50,000		Hours	Note:1

VL=LEDA-LEDK

Note 1: The “LED dice life time” is defined as the LED dice brightness decrease to 50% original brightness that the ambient temperature is 22℃and LED dice current 20mA.



7. BLOCK DIAGRAM



Correspondence between Data and Display Position

	S0000	S0001	S0002	S0003	S0004	S0005	S0006	S0007	----------	S958	S959
G000	R001	G001	B001	R002	G002	B002	R003	G003		G320	B320
G239	R001	G001	B001	R002	G002	B002	R003	G003		G320	B320

8. INPUT / OUTPUT TERMINALS

Pin No	Symbol	I/O	Description
1	SDO	O	Data output pin in serial mode. Leave it OPEN when not used. Note1
2	RESET	I	Hardware global reset. Low active. Normally pull high.
3	CSB	I	Serial port Data Enable Signal. Internal pull high, leave it OPEN when not used.
4	SCK	I	Serial port Clock. Internal pull high, leave it OPEN when not used.
5	SDI	I	Serial port Data input. Internal pull high, leave it OPEN when not used.
6	VSS	VI	Ground
7	DB0	I	Graphic Display Data.
8	DB1	I	
9	DB2	I	
10	DB3	I	
11	DB4	I	
12	DB5	I	
13	DB6	I	
14	DB7	I	
15	LEDA	VI	Power supply of LED backlight.
16	LEDK	VI	Ground of LED backlight.
17	DEN	I	Data Enable pin, connect to VDDIO or floating if not used.
18	HSYNC	I	Line synchronization signal, connect to VDDIO or floating if not used.
19	VSYNC	I	Frame synchronization signal, connect to VDDIO or floating if not used.
20	VSS	VI	Ground
21	DCLK (DOTCLK)	I	Dot-Clock signal.
22	VSS	VI	Ground
23	SHUT	I	Display shut down pin to put the driver into sleep mode. Internal pull low.
24	VCIM	O	Negative voltage of VCI. Please connect a capacitor for stabilization.
25	C1P	I	Connect a capacitor to C1N
26	C1N	I	Connect a capacitor to C1P
27	VLCD63	O	Internal generated power for source driver. Please connect a capacitor for stabilization.
28	VCIX2	I	Equals to 2xVCI. Please connect a capacitor for stabilization.
29	CYN	I	Connect a capacitor to CYP
30	CYP	I	Connect a capacitor to CYN
31	CXN	I	Connect a capacitor to CXP

Pin No	Symbol	I/O	Description
32	CXP	I	Connect a capacitor to CXN
33	VDDIO	VI	Voltage input pin for I/O logic
34	VCIP	VI	Voltage supply pin for analog circuit. Connect to same source of VCI.
35	VCI	VI	Booster input voltage pin. 2.5V~3.6V
36	VDD	VO	VDD is connecting with internal regulator. Please connect a capacitor for stabilization.
37	VDD	VO	
38	CN	I	Connect a capacitor to CP.
39	CP	I	Connect a capacitor to CN.
40	VGL	O	A negative voltage output pin for gate driver, Please connect a capacitor for stabilization.
41	C2N	I	Connect a capacitor to C2P.
42	C2P	I	Connect a capacitor to C2N.
43	C3N	I	Connect a capacitor to C3P.
44	C3P	I	Connect a capacitor to C3N.
45	VGH	O	A positive voltage output pin for gate driver, Please connect a capacitor for stabilization.
46	VCOML	O	This pin indicates a LOW level of VCOM generated in driving the VCOM alternation.
47	VCOMH	O	This pin indicates a HIGH level of VCOM generated in driving the VCOM alternation.
48	VSS	VI	Ground.
49	VFB	I	Main boost regulator feedback input. Connect feedback resistive divider to GND.
50	DRV	O	Power transistor gate signal for the boost converter.

Note1:SDO is not a tri-state output pin. Please don't connect to the other devices.

T/P Pin define:

No	Symbol
1	Top(X2)
2	Left(Y1)
3	Bottom(X1)
4	Right(Y2)

9. AC CHARACTERISTICS

9.1 AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 3.3V, Ta = 25℃)

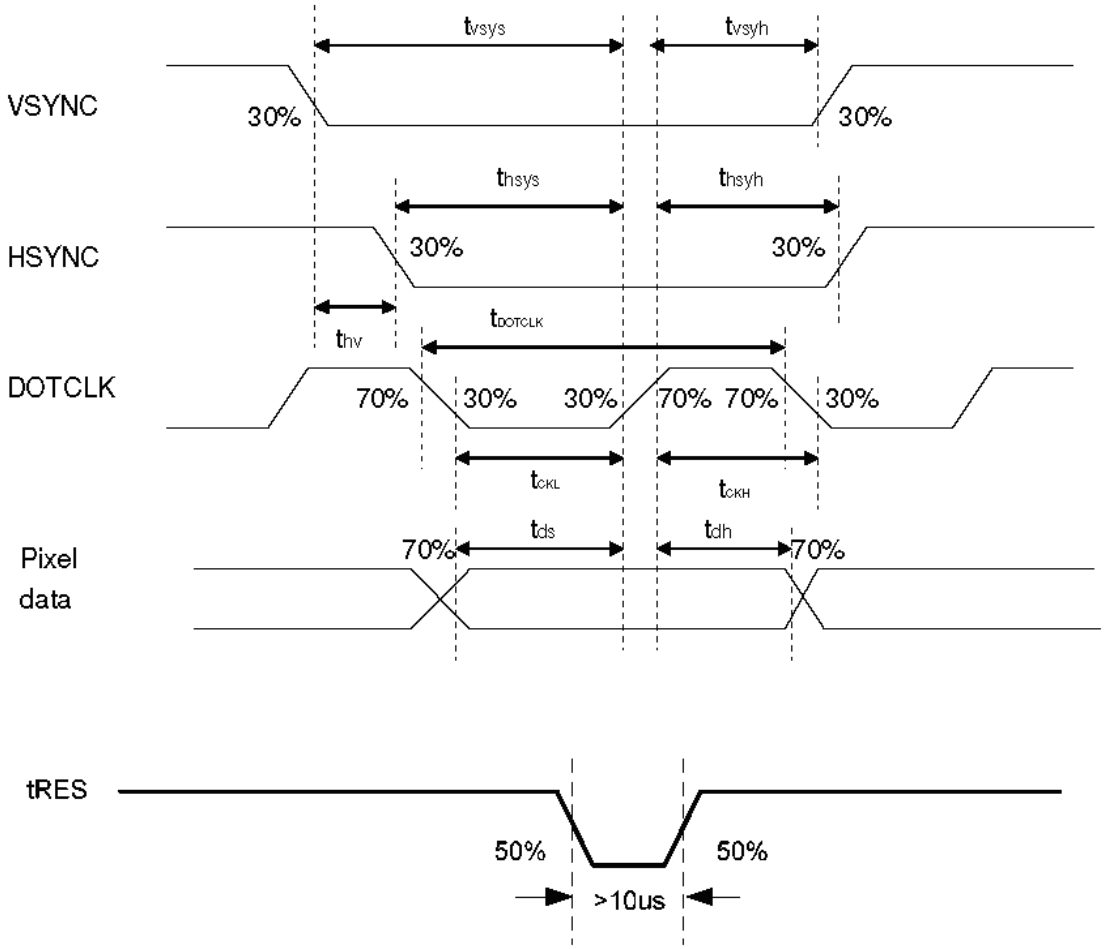
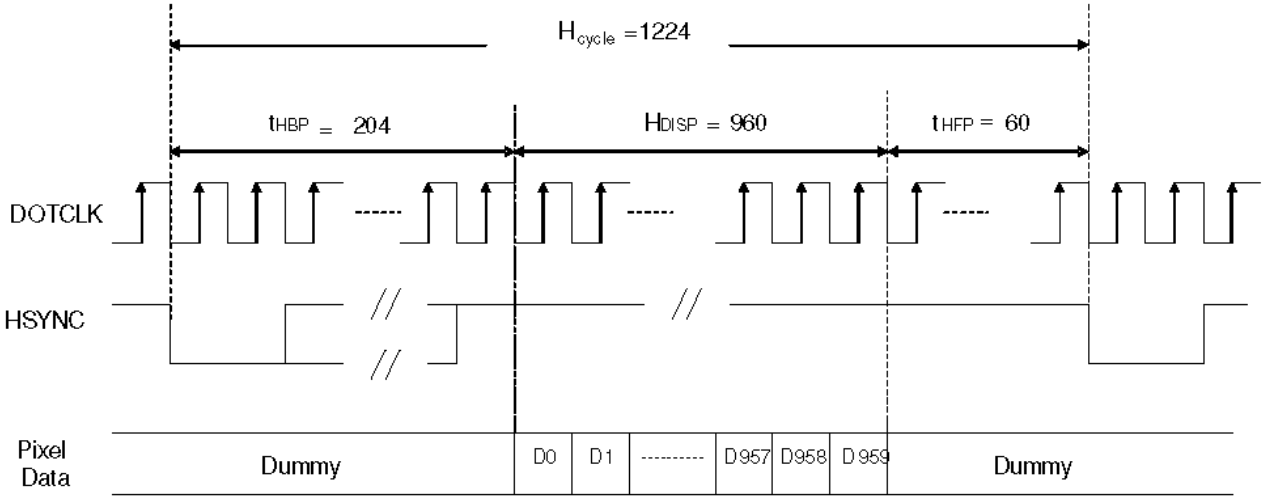


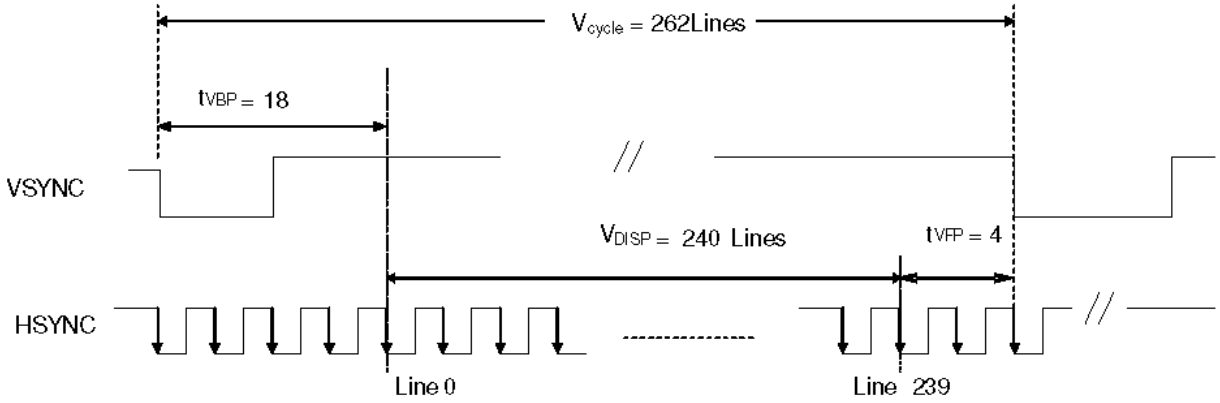
Figure 9.1-1 Pixel & tRES timing

Characteristics	Symbol	Min	Typ	Max	Unit
DOTCLK Frequency	fDOTCLK		19.5	30	MHz
DOTCLK Period	tDOTCLK	33.3	51.3		ns
Vertical Sync Setup Time	tvsys	10			ns
Vertical Sync Hold Time	tvsyh	10			ns
Horizontal Sync Setup Time	thsys	10			ns
Horizontal Sync Hold Time	thsyh	10			ns
Phase difference of Sync Signal Falling Edge	thv	1	-	240	tDOTCLK
DOTCLK Low Period	tCKL	15			ns
DOTCLK High Period	tCKH	15			ns
Data Setup Time	tds	8			ns
Data hold Time	tdh	8			ns
Reset pulse width	tRES	10	-	-	us

Table 9.1-1 Pixel & tRES timing



a) Horizontal Data Transaction Timing



b) Vertical Data Transaction Timing

Figure 9.1-2 Data transaction timing (SYNC mode)

Characteristics		Symbol	Min	Typ	Max	Unit
DOTCLK Frequency		fDOTCLK	-	19.5	30	MHz
DOTCLK Period		tDOTCLK	33.3	51.3	-	ns
Horizontal Frequency (Line)		fH	-	15.72	22.35	KHz
Vertical Frequency (Refresh)		fV	-	60	90	Hz
Horizontal Back Porch		tHBP	-	204	-	tDOTCLK
Horizontal Front Porch		tHFP	-	60	-	tDOTCLK
Horizontal Data Start Point		tHBP	-	204	-	tDOTCLK
Horizontal Blanking Period		tHBP + tHFP	-	264	-	tDOTCLK
Horizontal Display Area		HDISP	-	960	-	tDOTCLK
Horizontal Cycle		Hcycle	-	1224	1350	tDOTCLK
Vertical Back Porch		tVBP	-	18	-	Lines
Vertical Front Porch		tVFP	-	4	-	Lines
Vertical Data Start Point		tVBP	-	18	-	Lines
Vertical Blanking Period		tVBP + tVFP	-	22	-	Lines
VS Pulse width		tWV	-	4	-	Lines
Vertical Display Area	NTSC	VDISP	-	240	-	Lines
	PAL			280(PALM=0)		
				288(PALM=1)		
Vertical Cycle	NTSC	Vcycle	-	262	350	Lines
	PAL			313		

Table 9.1-2 Data transaction timing in normal operating mode

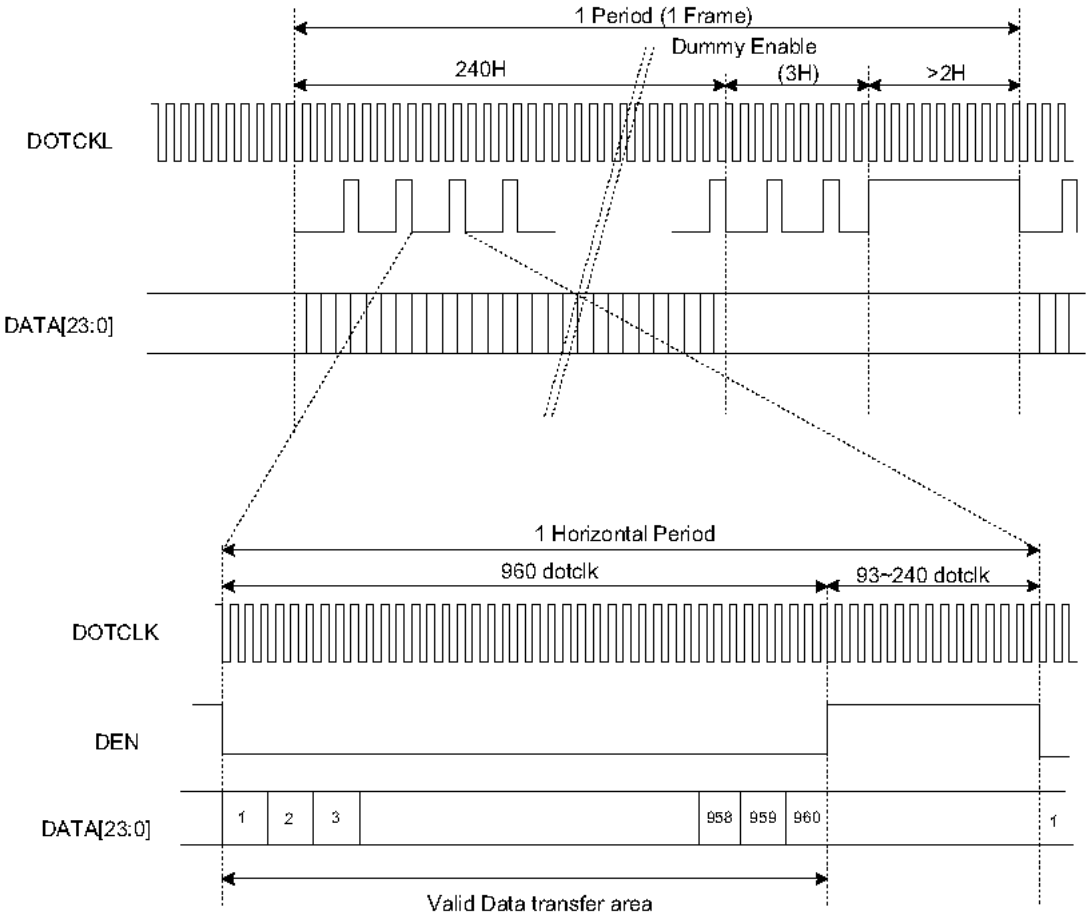


Figure 9.1-3 Signal timing in DE mode

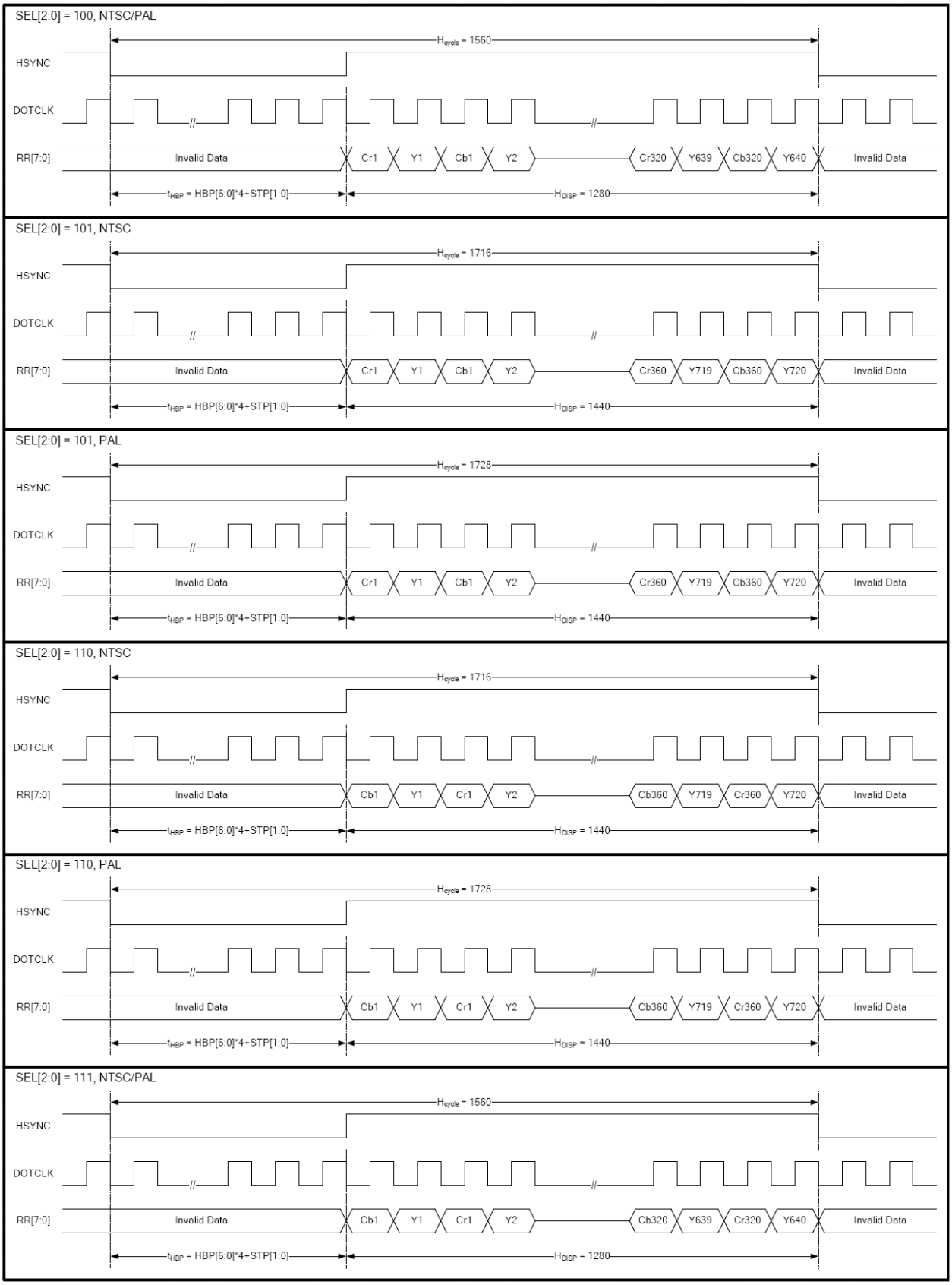


Figure 9.1-4 CCIR601 horizontal timing

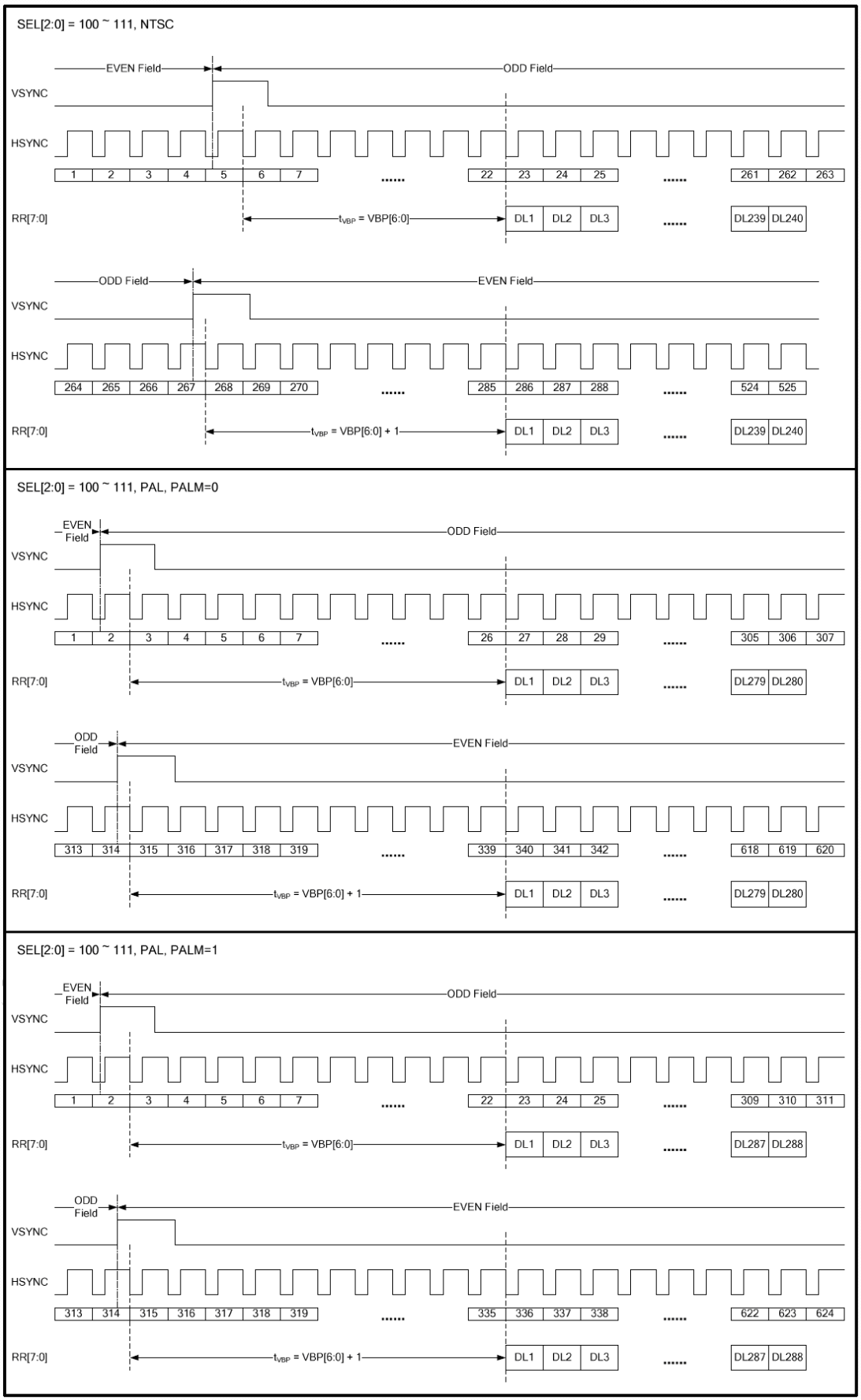


Figure 9.1-5 CCIR601 vertical timing

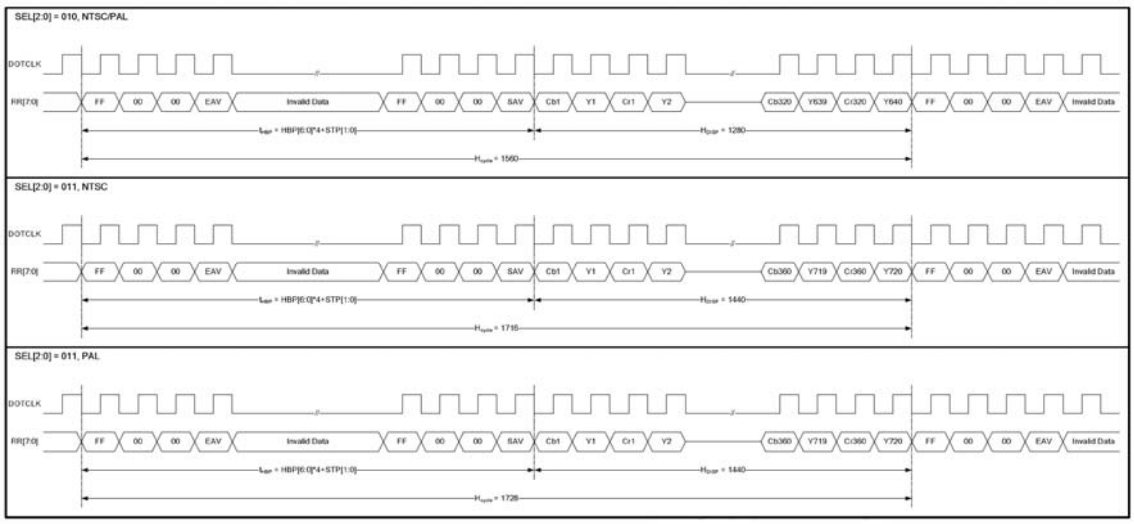


Figure 9.1-6 CCIR656 horizontal timing

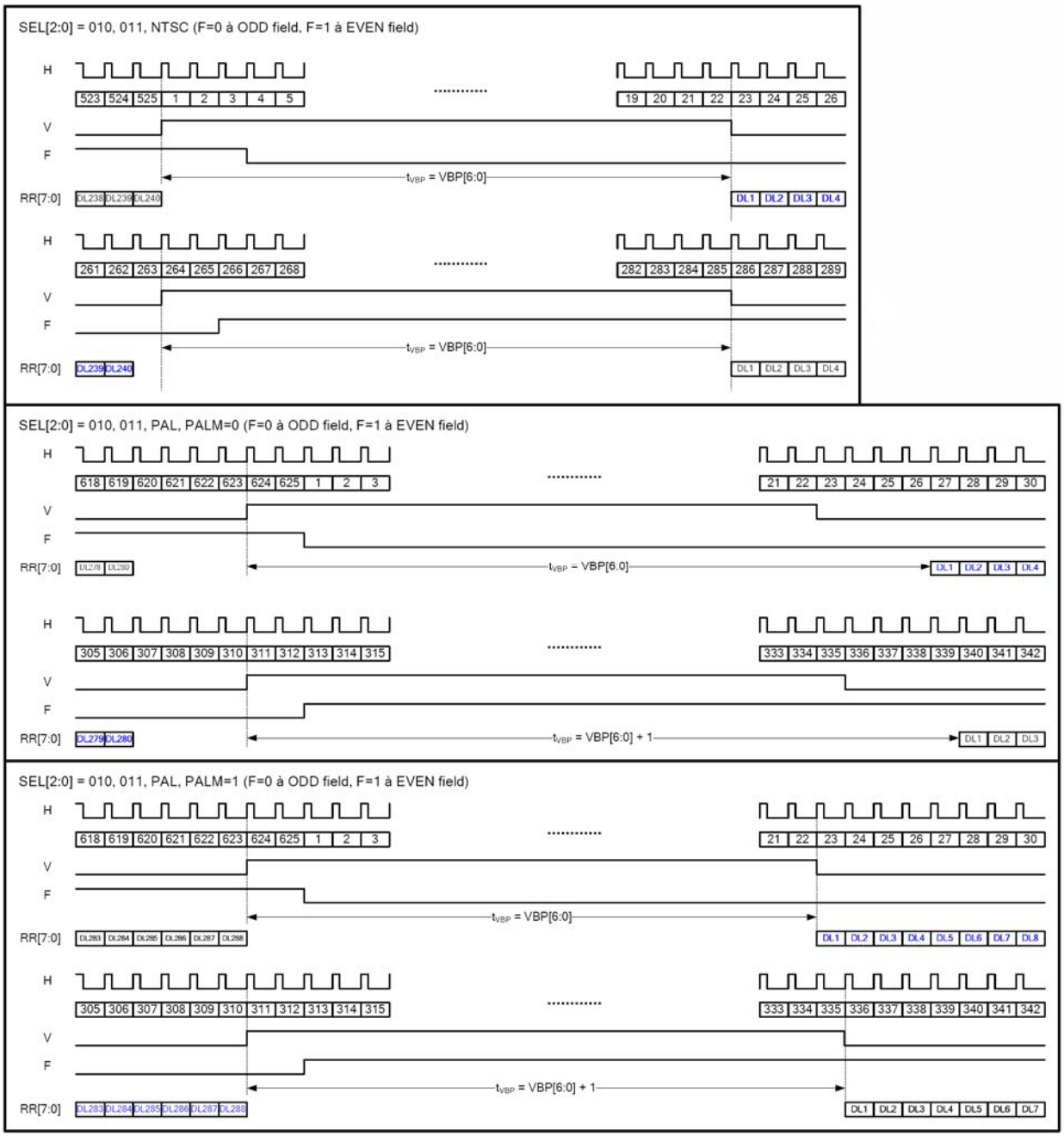
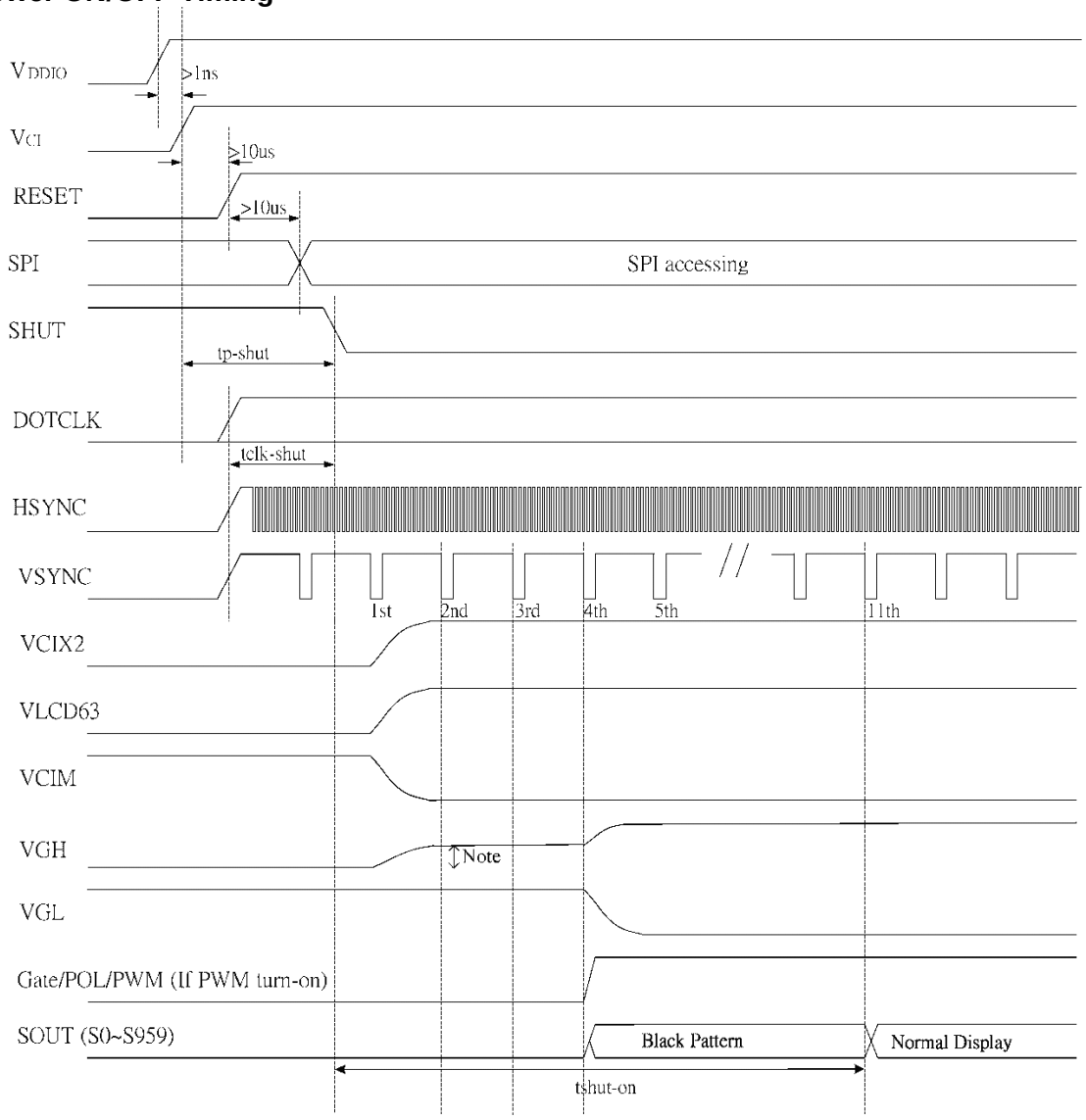


Figure 9.1-7 CCIR656 vertical timing

9.2 Power ON/OFF Timing



Note: There is a diode between VCIX2 and VGH. Switch on VCIX2 will move VGH up.

Figure 9.2-1 Power Up Sequence

Characteristics	Symbol	Min	Typ	Max	Units
VCI / VDDIO on to falling edge of SHUT	tp-shut	1	-	-	us
DOTCLK to falling edge of SHUT	tclk-shut (Note1)	1	-	-	clk
Falling edge of SHUT to display start -1 line: 408 clk -1 frame: 262 line -DOTCLK = 19.5MHz	tshut-on (Note2)	-	-	11	frame

Note1 : It is necessary to input DOTCLK before the falling edge of SHUT.
Note 2: Display starts at 11th falling edge of VSYNC after the falling edge of SHUT.
The display starts at the falling edge to VSYNC which is determined by BLT[1:0] of R04h.

Table 9.2-1 Power Up Sequence

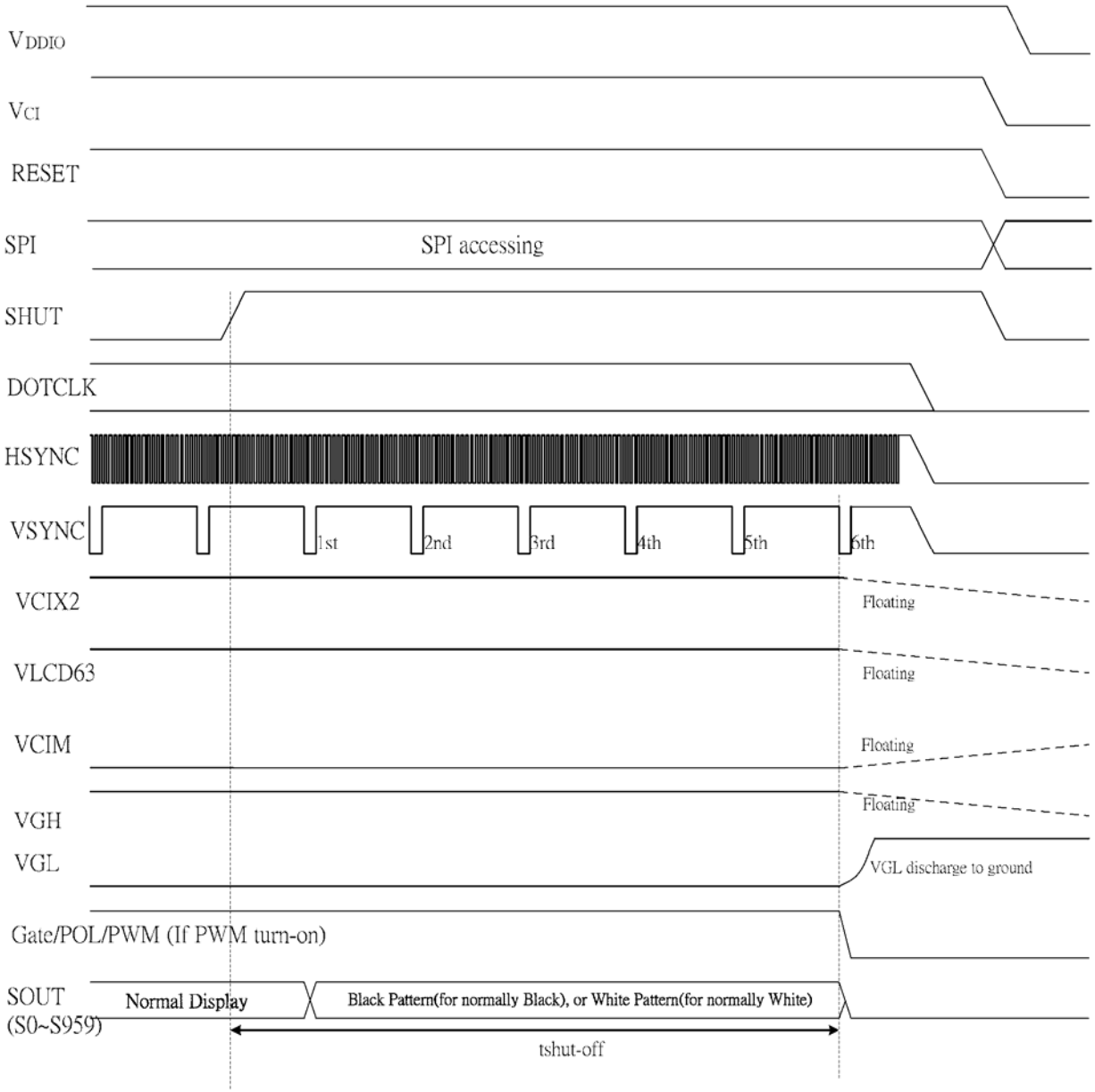


Figure 9.2-2 Power Down Sequence

Characteristics	Symbol	Min	Typ	Max	Unit
Rising edge of SHUT to display off -1 line: 408 clk -1 frame: 262 line -DOTCLK = 19.5MHz	Tshut-off	-	-	6	frame

Note: DOTCLK must be maintained at lease 6 frames after the rising edge of SHUT.
Display become off at the 6th falling edge of VSYNC after the falling edge of SHUT.
If RESET signal is necessary for power down, provide it after the 6-frames-cycle of the SHUT period.

Table 9.2-2 Power Down Sequence

9.3 Serial Interface

The SPI is available through the chip select line (CSB), serial transfer clock line (SCK), serial data input (SDI), and serial data output (SDO).

The Driver IC recognizes the start of data transfer at the falling edge of CSB input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of CSB input. The Driver IC is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the Driver IC are compared and both 6-bit data correspond. The identification code must be 011100. Two different chip addresses must be assigned to the Driver IC because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When the RS = 1, instruction write. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

After receiving the start byte, the Driver IC starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted (9th SCK started). All Driver IC instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (IB15 to 0---9th ~24th SCK).

RS	RW	status
0	0	Write SPI address
0	1	Read gate line number(Note)
1	0	Write SPI data
1	1	Read SPI data

Table9.3-1RS & RW setting

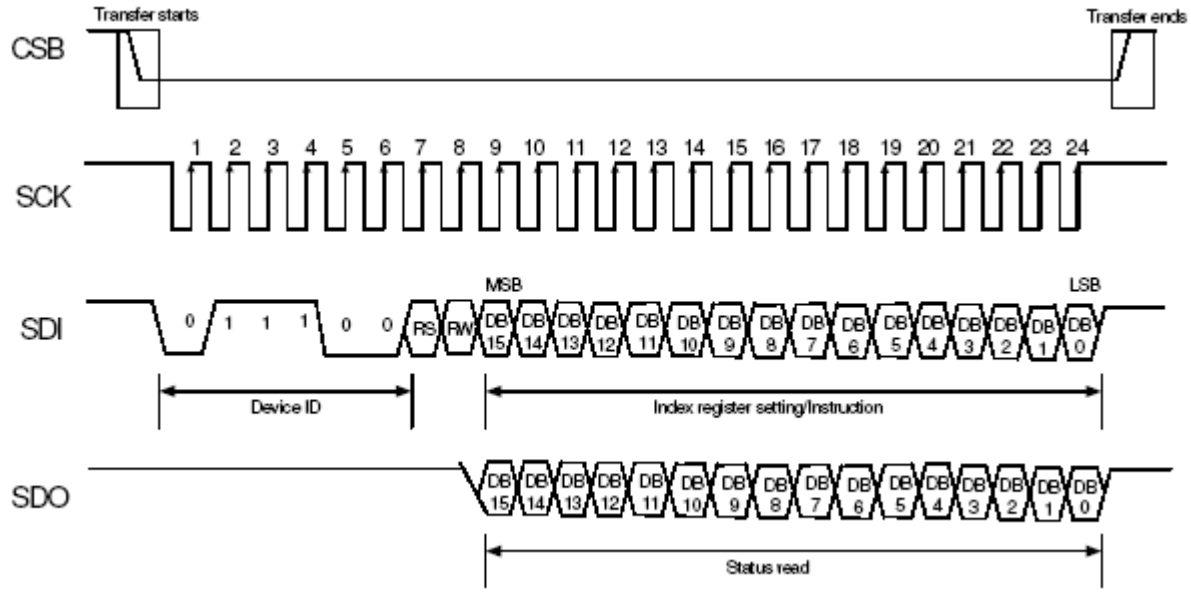
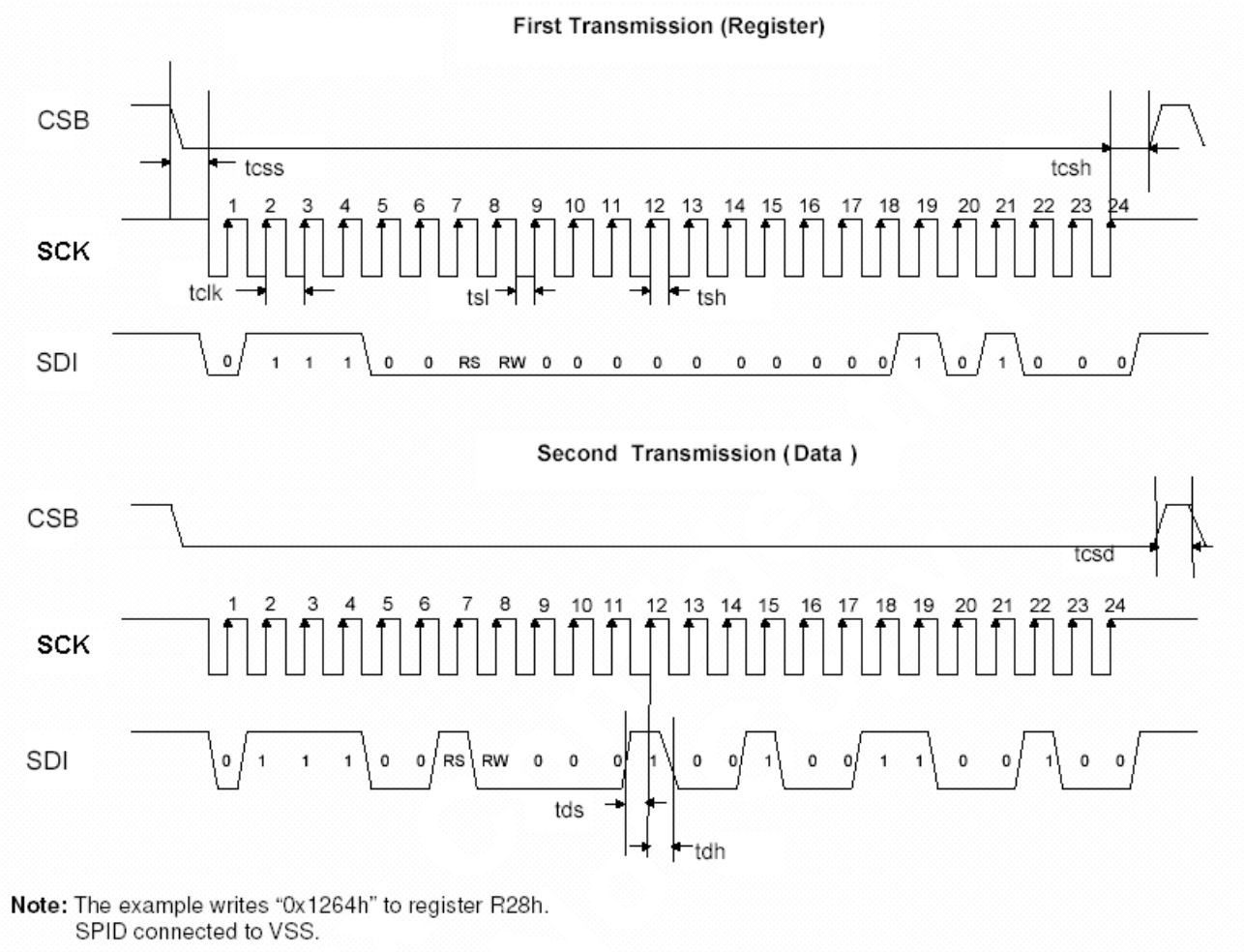


Figure9.3-1 SPI Timing

Under the standard condition, the number of CLK is twenty-four units. After CSB has transmitted twenty-four units of CLK, it has to change into High. When the number of CLK is less than 24 units, the data of SPI can't be downloaded. When the number of CLK is more than 25 units, the data of SPI will download the former data of the 24 units of CLK.

- **Write SPI**



Note: The example writes "0x1264h" to register R28h.
SPID connected to VSS.

Figure9.3-2 SPI interface Timing Diagram & W rite SPI Example

- **Read SPI**

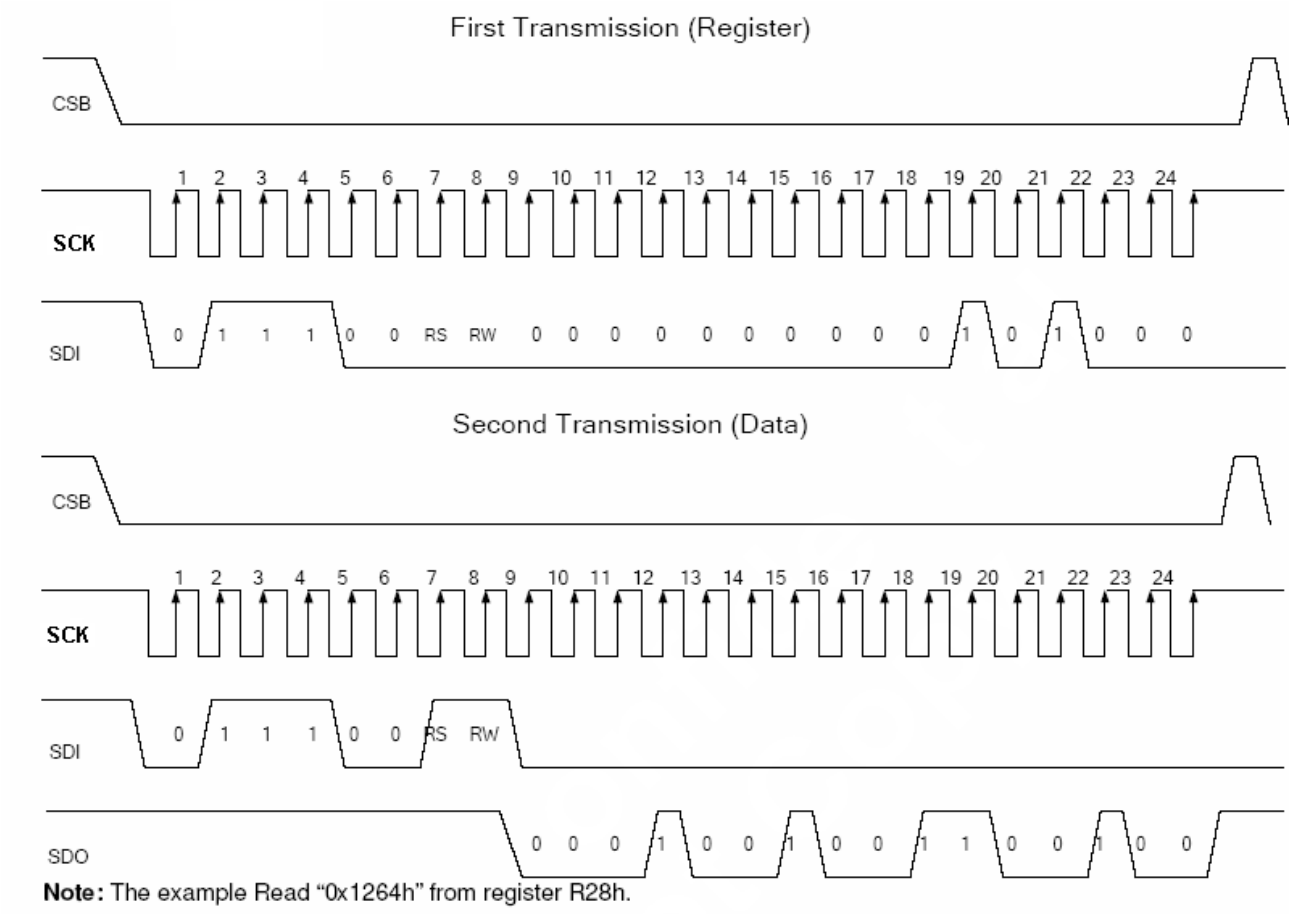


Figure9.3-3 SPI interface Timing Diagram & Read SPI Example

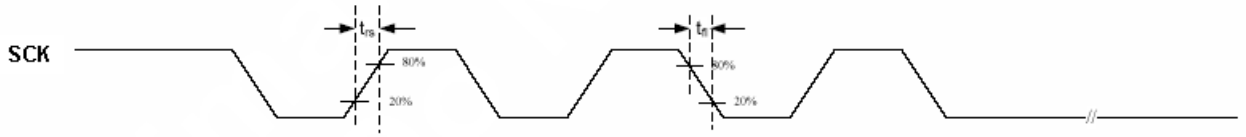


Figure9.3-4Rising/Falling time

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Clock Rising Time	trs	-	-	30	ns
Clock Falling Time	tfl	-	-	30	ns
Chip Select Setup Time	tcss	0	-	-	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

Table 9.3-2 SPI timing

9.4 Output Voltage Relationship

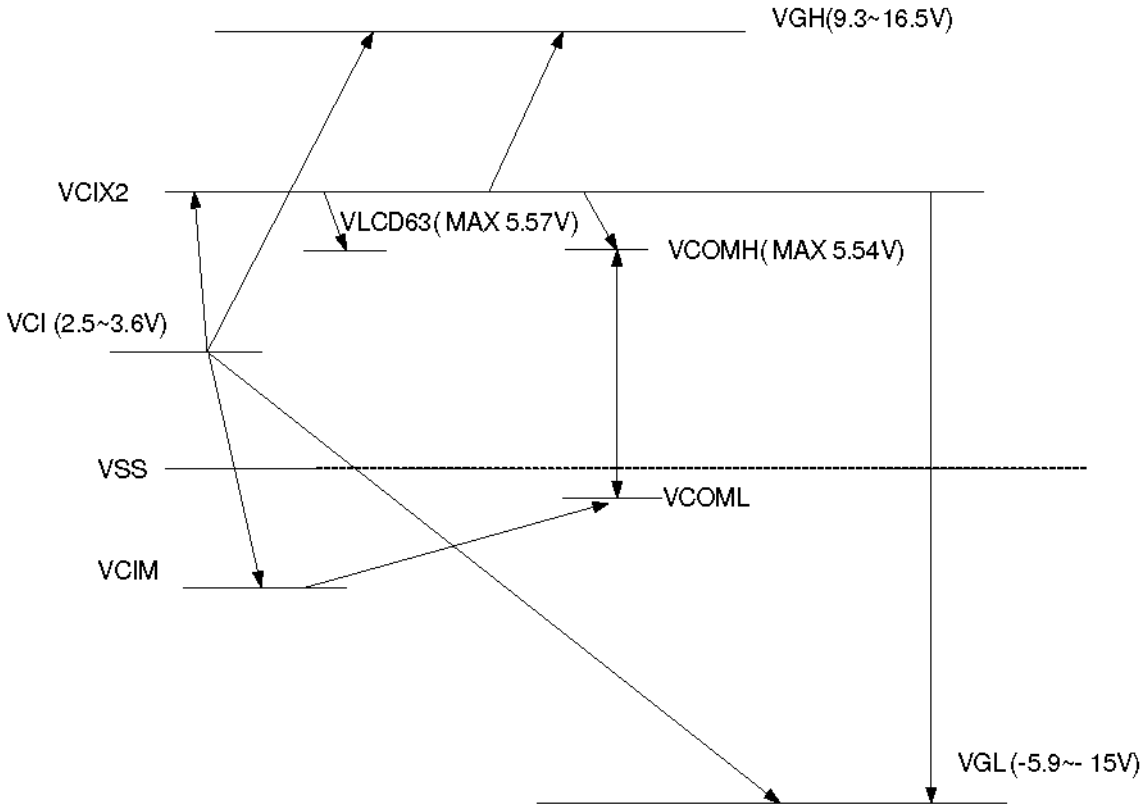


Figure 9.4-1 LCD driving voltage relationship

Note: The above voltages level assumed 100% efficiency of the internal booster. There has no voltage drop due to resistance from ITO trace of the panel.

10. COMMAND DESCRIPTION

10.1 Command Table

Reg#	Register	R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	PINV	BGR	SM	TB	CPE	0	0	0	0	0	0	0	0
R02h	LCD driver AC control	0	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
R04h	Data and color filter control	0	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	1	1	1
R05h	Function control	0	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0
R06h	Reserved	Reserved																	
R07h	Reserved	Reserved																	
R0Ah	Contrast/ Brightness control	0	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0
R0Dh	Power control (3)	0	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	1	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0
R0Fh	Gate scan starting Position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R16h	Horizontal Porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0
R17h	Vertical Porch	0	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R27h	Reserved	Reserved																	
R28h	Reserved	Reserved																	
R29h	Reserved	Reserved																	
R2Bh	Reserved	Reserved																	
R30h	γ control (1)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	γ control (9)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	γ control (10)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Software settings will override hardware pin (eg, BGR bits override BGR pin definition)

Table 10.1-1 Command tabl

10.2 REGISTER DESCRIPTION

Status Read

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 10.2-1 Status read

The status read instruction reads the internal status of the T–con IC.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	R L	REV	PINV	BGR	S M	T B	CPE	0	0	0	0	0	0	0	0

Figure 10.2-2 Driver output control

CPE: When CPE=0, Vcim is not shut down, but VGH, VGL, and Vcix2 are shut down. When CPE=1, internal charge pump Vcim, VGH, VGL, and Vcix2 are enabled.

REV: Displays all character and graphics display sections with reversal when REV = “0”. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below**.**

REV	RGB data	Source output level	
		VCOM = “H”	VCOM = “L”
0	00000H : 3FFFFH	V0 : V63	V63 : V0
1	00000H : 3FFFFH	V63 : V0	V0 : V63

Table 10.2-1 Source output level

PINV: When PINV=0, POL output is same phase with internal VCOM signal. When PINV=1, POL output phase is reversed with VCOM signal.

BGR: Selects the <R><G><B> arrangement. When BGR = “0” <R><G><B> color is assigned from S0.When BGR = “1” <B><G><R> color is assigned from S0.

SM: Change the division of gate driver. When SM = “0”, odd/even division (interlace mode) is selected. When SM = “1”, upper/lower division is selected. Select the division mode according to the mounting method.

TB: Selects the output shift direction of the gate driver. When TB = “1”, G0 shifts to G239. When TB = “0”, G239 shifts to G0.

RL: Selects the output shift direction of the source driver. When RL = “1”, S0 shifts to S959 and <R><G><B> color is assigned from S0. When RL = “0”, S959 shifts to S0 and <R><G><B> color is assigned from S959. Set RL bit and BGR bit when changing the dot order of R, G and B.

Note: The default setting of register bits **REV**, **BGR**, **TB** and **RL** are defined by the logic stage of corresponding hardware pins. These bits will override the hardware setting once software command was sent to set the bits.

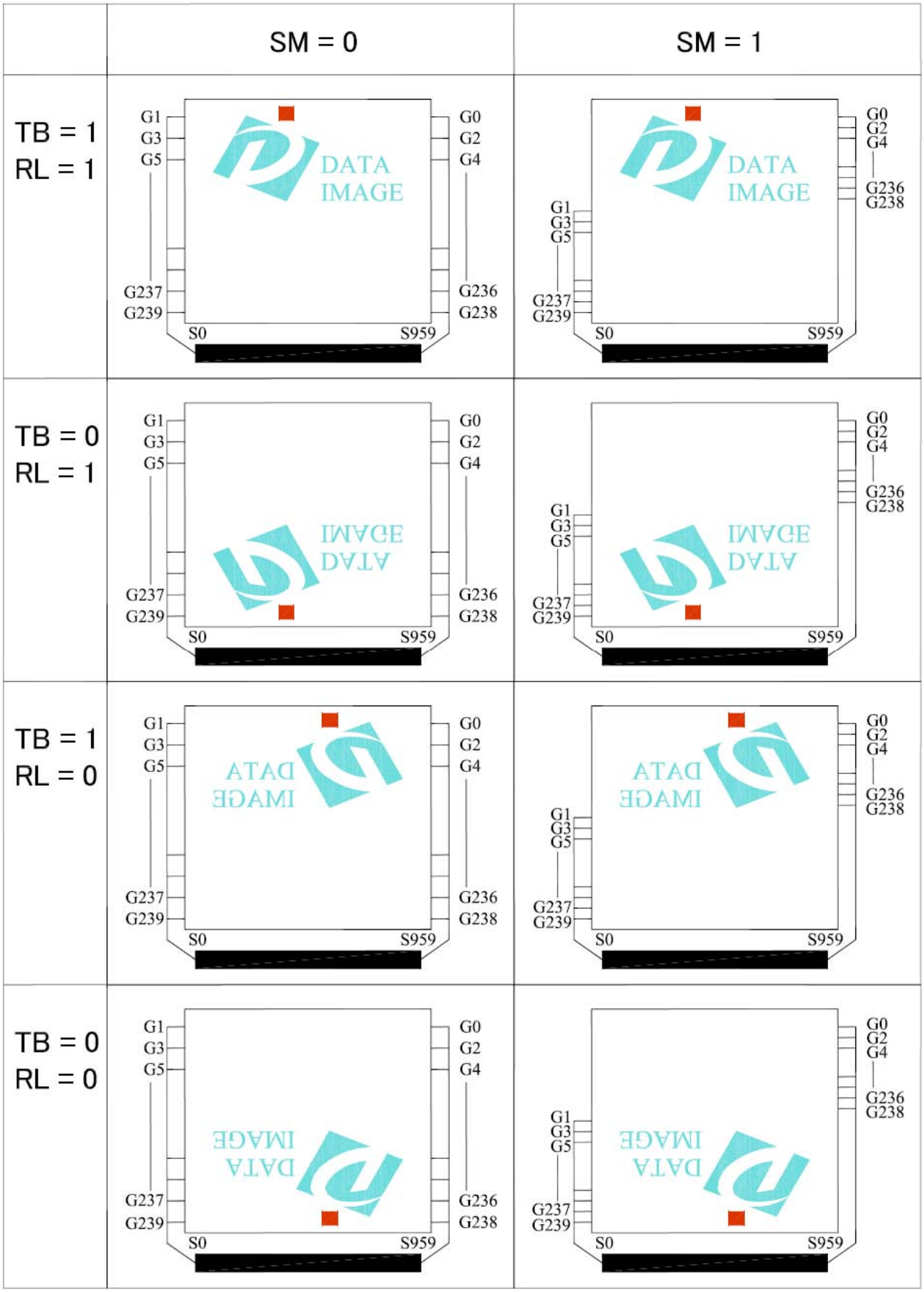


Figure 10.2-3 Scan direction & Display

LCD-Driving-Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B / C	0	0	0	0	0	0	0	0	0

Figure 10.2-4 LCD-driving-waveform control

B/C: When B/C = 0, frame inversion of the LCD driving signal is enabled. When B/C = 1, line inversion waveform is generated

Power control 1 (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0

Figure 10.2-5 Power control 1

DCT3-0: Set the step-up cycle of the step-up circuit for 8-color mode (CM = VDDIO). When the cycle is accelerated, the Vcim and Vcix2 driving ability of the step-up circuit increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption. VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

- Fline = horizontal frequency (Fline Typ. 15KHz)

Table10.2-2 Step-up cycle

BT2-0 & BTF: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power supply voltage to be used.

BTF	BT2	BT1	BT0	VGH output	VGL output
0	0	0	0	V_{CIX2} X 3	-(V_{CIX2} X 3) + V_{CI}
0	0	0	1	V_{CIX2} X 3	-(V_{CIX2} X 2)
0	0	1	0	V_{CIX2} X 3	-(V_{CIX2} X 3)
0	0	1	1	V_{CIX2} X 2 + V_{CI}	-(V_{CIX2} X 2) -V_{CI}
0	1	0	0	V_{CIX2} X 2 + V_{CI}	-(V_{CIX2} X 2)
0	1	0	1	V_{CIX2} X 2 + V_{CI}	-(V_{CIX2} X 2) + V_{CI}
0	1	1	0	V_{CIX2} X 2	-(V_{CIX2} X 2)
1	1	1	1	V_{CIX2} X 2	-(V_{CIX2} X 2) + V_{CI}
1	X	X	X	V_{CIX2} X 3	-V_{CIX2}

Table 10.2-3 VGH and VGL booster ratio

DC3-0: Set the step-up cycle of the step-up circuit for 262k-color mode (CM = VSS). When the cycle is accelerated, the Vcim and Vcix2 driving ability of the step-up circuit increase, but their current consumption increase, too. Adjust the cycle taking into account the display quality and power consumption. VGH and VGL are always fixed at the step-up cycle of Fline x 0.5.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline x 14
0	0	0	1	Fline x 12
0	0	1	0	Fline x 10
0	0	1	1	Fline x 8
0	1	0	0	Fline x 7
0	1	0	1	Fline x 6
0	1	1	0	Fline x 5
0	1	1	1	Fline x 4
1	0	0	0	Fline x 3
1	0	0	1	Fline x 2
1	0	1	0	Fline x 1
1	0	1	1	Fline x 0.5
1	1	0	0	Fline x 0.25
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

- Fline = horizontal frequency (Fline Typ. 15KHz)

Table 10.2-4 Step-up cycle

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current taking into account the power consumption. During times when there is no display, such as when the system is in a sleep mode, set AP2-0 = “000” to halt the operational amplifier circuit and the step-up circuits to educe current consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

Table 10.2-5 Op-amp power

Input Data and Color Filter Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	1	1	1

Figure 10.2-6 Input data and color filter control

SEL2-0: Define the input interface mode.

SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	Do not setting	Do not setting
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Table10.2-6 Interface type

OEA1-0: Odd/Even filed advanced function.

OEA1	OEA0	
0	0	Display Start @ VBP delay for Odd field and @ ***VBP-1*** for Even field.
0	1	Display Start @ VBP delay for Odd field and @ ***VBP*** for Even field.
1	0	Display Start @ VBP delay for Odd field and @ ***VBP+1*** for Even field.
1	1	No use

Table10.2-7 Odd/Even filed advanced function.

BLT[1:0]: Set the initial power on black image insertion time.
00: 10 fields
01: 20 fields
10: 40 fields
11: 80 fields

PALM: Set the input data line number in PAL mode
0: 280 lines
1: 288 lines

Function Control (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0

Figure 10.2-7 Function control

FB2-0: Set PWM feedback level adjustment.
000: 0.4V
001: 0.45V
010: 0.5V
011: 0.55V
100: 0.6V
101: 0.65V
110: 0.7V
111: 0.75V

PWM: When PWM=0, PWM function is disabled. When PWM=1, PWM function is enabled.
DIT: When DIT=0, dithering function is turned off. When DIT=1, dithering function is enabled.
DEO: When DEO=0, VSYNC/HSYNC are also needed in DE mode. Under this condition, vertical back porch is defined by VBP[6:0] and the horizontal first valid data is defined by DE signal. When DEO=1, only DEN signal is needed in DE mode.
HSP: When HSP=0, HSYNC is negative polarity. When HSP=1, HSYNC is positive polarity.
VSP: When VSP=0, VSYNC is negative polarity. When VSP=1, VSYNC is positive polarity.
CKP: When CKP=0, data is latched in DCLK falling edge. When CKP=1, data is latched by DCLK rising edge.
DEP: When DEP=0, DEN is negative polarity active. When DEP=1, DEN is positive polarity active.
LPF: When LPF=0, the low pass filter function in YUV mode is disabled. When LPF=1, the low pass filter function is YUV mode is enabled.
GDIS: When GDIS=0, VGL has no discharge path to VSS in standby mode. When GDIS=1, VGL will discharge to VSS in standby mode.
XDK: When XDK=0, VCIX2 is 2 stage pumping from VCI. (VCIX2=3 x VCI) When XDK=1, VCIX2 is 2 phase pumping from VCI. (VCIX2=2 x VCI)
GHN: When GHN=0, all gate outputs are forced to VGH. When GHN=1, gate driver is normal operation.

Contrast/Brightness Control (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0

Figure 10.2-8 Contrast/Brightness control

CON4-0: Display Contrast level adjustment. (0.125/step) Adjust range from 00h (level = 0) to 1Fh (level = 3.875). Default value is 08h (level = 1).

BR6-0: Display Brightness level adjustment. (2/step) Adjust range from 00h(level = -128) to 7Fh(level = +126). Default value is 40h(level = 0).

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0

Figure 10.2-9 Frame cycle control

NO1-0: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	1.5 us
0	1	3 us
1	0	4.5 us
1	1	6 us

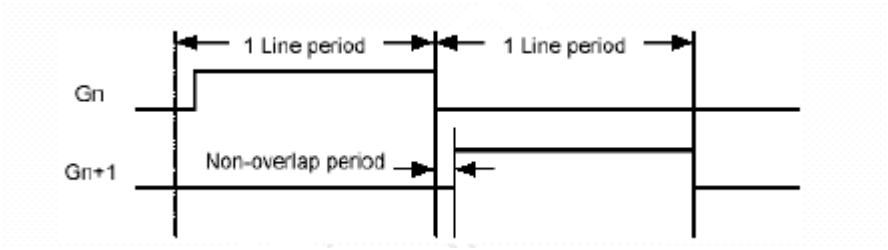


Figure 10.2-10 NO timing diagram

SDT1-0: Set delay amount from the gate output signal falling edge to the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	1 us
0	1	3 us
1	0	5 us
1	1	7 us

Table 10.2-8 Delay amount of the source output

EQ2-0: Sets the equalizing period.

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	3 us
0	1	0	4 us
0	1	1	5 us
1	0	0	6 us
1	0	1	7 us
1	1	0	8 us
1	1	1	9 us

Table 10.2-9 EQ period

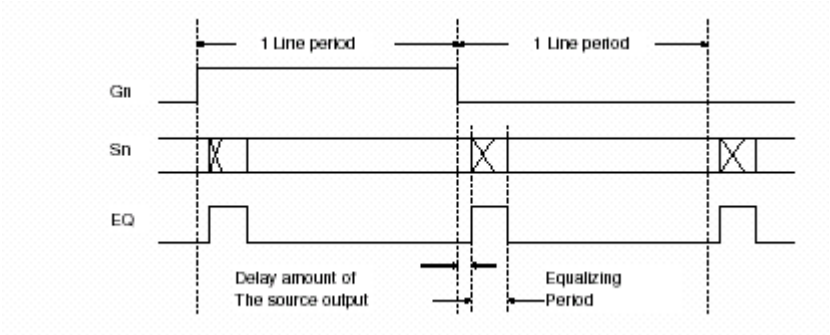


Figure 10.2-11 EQ timing diagram

Power Control 2 (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 10.2-12 Power control 2

VRC[2:0]: set the VCIX2 charge pump voltage clamp.
VRC[2:0]=000, 5.1V
VRC[2:0]=001, 5.3V
VRC[2:0]=010, 5.5V
VRC[2:0]=011, 5.7V
VRC[2:0]=100, 5.9V
VRC[2:0]=101, reserved
VRC[2:0]=110, reserved
VRC[2:0]=111, reserved

VDS[1:0]: set the VDD regulator voltage if pin “REGVDD” is set to VDDIO.
VDS[1:0]=00, 1.8V
VDS[1:0]=01, 2V
VDS[1:0]=10, 2.2V
VDS[1:0]=11, 2.5V

VRH5-0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 2.464 to 4.456 times the Vref voltage set by VRH5-0.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63Voltage
0	0	0	0	0	0	Vref x 2.456
0	0	0	0	0	1	Vref x 2.488
0	0	0	0	1	0	Vref x 2.520
0	0	0	0	1	1	Vref x 2.552
0	0	0	1	0	0	Vref x 2.584
0	0	0	1	0	1	Vref x 2.616
0	0	0	1	1	0	Vref x 2.648
0	0	0	1	1	1	Vref x 2.680
0	0	1	0	0	0	Vref x 2.712
0	0	1	0	0	1	Vref x 2.744
0	0	1	0	1	0	Vref x 2.776
0	0	1	0	1	1	Vref x 2.808
0	0	1	1	0	0	Vref x 2.840
0	0	1	1	0	1	Vref x 2.872
0	0	1	1	1	0	Vref x 2.904
0	0	1	1	1	1	Vref x 2.936
0	1	0	0	0	0	Vref x 2.968
0	1	0	0	0	1	Vref x 3.000
0	1	0	0	1	0	Vref x 3.032
0	1	0	0	1	1	Vref x 3.064
0	1	0	1	0	0	Vref x 3.096
0	1	0	1	0	1	Vref x 3.128
0	1	0	1	1	0	Vref x 3.160
0	1	0	1	1	1	Vref x 3.192
0	1	1	0	0	0	Vref x 3.224
0	1	1	0	0	1	Vref x 3.256
0	1	1	0	1	0	Vref x 3.288
0	1	1	0	1	1	Vref x 3.320
0	1	1	1	0	0	Vref x 3.352
0	1	1	1	0	1	Vref x 3.384
0	1	1	1	1	0	Vref x 3.416
0	1	1	1	1	1	Vref x 3.448

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VLCD63Voltage
1	0	0	0	0	0	Vref x 3.480
1	0	0	0	0	1	Vref x 3.512
1	0	0	0	1	0	Vref x 3.544
1	0	0	0	1	1	Vref x 3.576
1	0	0	1	0	0	Vref x 3.608
1	0	0	1	0	1	Vref x 3.640
1	0	0	1	1	0	Vref x 3.672
1	0	0	1	1	1	Vref x 3.704
1	0	1	0	0	0	Vref x 3.736
1	0	1	0	0	1	Vref x 3.768
1	0	1	0	1	0	Vref x 3.800
1	0	1	0	1	1	Vref x 3.832
1	0	1	1	0	0	Vref x 3.864
1	0	1	1	0	1	Vref x 3.896
1	0	1	1	1	0	Vref x 3.928
1	0	1	1	1	1	Vref x 3.960
1	1	0	0	0	0	Vref x 3.992
1	1	0	0	0	1	Vref x 4.024
1	1	0	0	1	0	Vref x 4.056
1	1	0	0	1	1	Vref x 4.088
1	1	0	1	0	0	Vref x 4.120
1	1	0	1	0	1	Vref x 4.152
1	1	0	1	1	0	Vref x 4.184
1	1	0	1	1	1	Vref x 4.216
1	1	1	0	0	0	Vref x 4.248
1	1	1	0	0	1	Vref x 4.280
1	1	1	0	1	0	Vref x 4.312
1	1	1	0	1	1	Vref x 4.344
1	1	1	1	0	0	Vref x 4.376
1	1	1	1	0	1	Vref x 4.408
1	1	1	1	1	0	Vref x 4.440
1	1	1	1	1	1	Vref x 4.472

*Vref is the internal reference voltage equals to 1.25V.

Table 10.2-10 VLCD63 voltage

Power Control 3 (R0Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	1	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0

Figure 10.2-13 Power control 3

VDV6-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM amplitude 0.6 to 1.2525 times the VLCD63 voltage. When VCOMG = "0", the settings become invalid. External voltage at VCOMR is referenced when VDV = "01111xx".

VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	0	0	VLCD63 x 0.6000
0	0	0	0	0	0	1	VLCD63 x 0.6075
0	0	0	0	0	1	0	VLCD63 x 0.6150
0	0	0	0	0	1	1	VLCD63 x 0.6225
0	0	0	0	1	0	0	VLCD63 x 0.6300
:	:	:	:	:	:	:	: Step = 0.0075 :
0	1	1	1	0	1	0	VLCD63 x 1.0350
0	1	1	1	0	1	1	VLCD63 x 1.0425
							Reference from
0	1	1	1	1	*	*	external voltage (VCOMR)
1	0	0	0	0	0	0	VLCD63 x 1.0500
1	0	0	0	0	0	1	VLCD63 x 1.0575
:	:	:	:	:	:	:	: Step = 0.0075 :
1	0	1	1	0	1	0	VLCD63 x 1.2450
1	0	1	1	0	1	1	VLCD63 x 1.2525
1	0	1	1	1	*	*	Reserved
1	1	*	*	*	*	*	Reserved

Table 10.2-11 VCOM amplitude

Gate Scan Position (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 10.2-14 Gate scan position

SCN8-0: Set the scanning starting position of the gate driver.

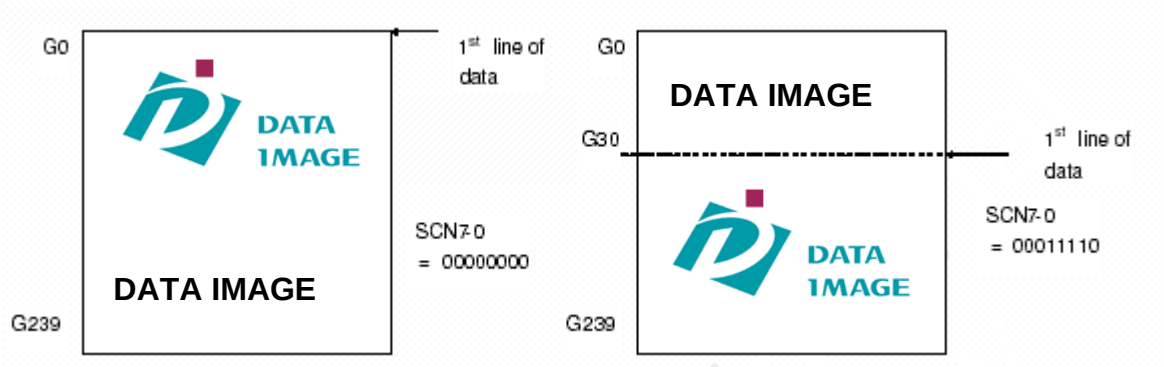


Figure 10.2-15 Gate scan display position

Horizontal Porch (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0

Figure 10.2-16 Horizontal Porch

XLIM8-0: Set the number of valid pixel per line.

XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				:					:
				:					Step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	Reserved
1	1	*	*	*	*	*	*	*	Reserved

Table 10.2-12 No. of pixel per line

Vertical Porch (R17h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 10.2-17 Vertical porch

HBP6-0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XLIM8-0 and before the first valid data will be treated as dummy data. The setting is only effective in SYNC mode timing.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle	
							Serial	YUV
0	0	0	0	0	0	0	Can't set	
0	0	0	0	0	0	1	Can't set	
0	0	0	0	0	1	0	Can't set	
0	0	0	0	0	1	1	Can't set	
0	0	0	0	1	0	0	Can't set	
0	0	0	0	1	0	1	Can't set	
0	0	0	0	1	1	0	Can't set	
0	0	0	0	1	1	1	Can't set	
0	0	0	1	0	0	0	Can't set	
0	0	0	1	0	0	1	27	36
0	0	0	1	0	1	0	30	40
							:	:
							Step = 3	Step = 4
							:	:
1	1	1	1	1	1	0	378	504
1	1	1	1	1	1	1	381	508

Table 10.2-13 No. of clock cycle of clock

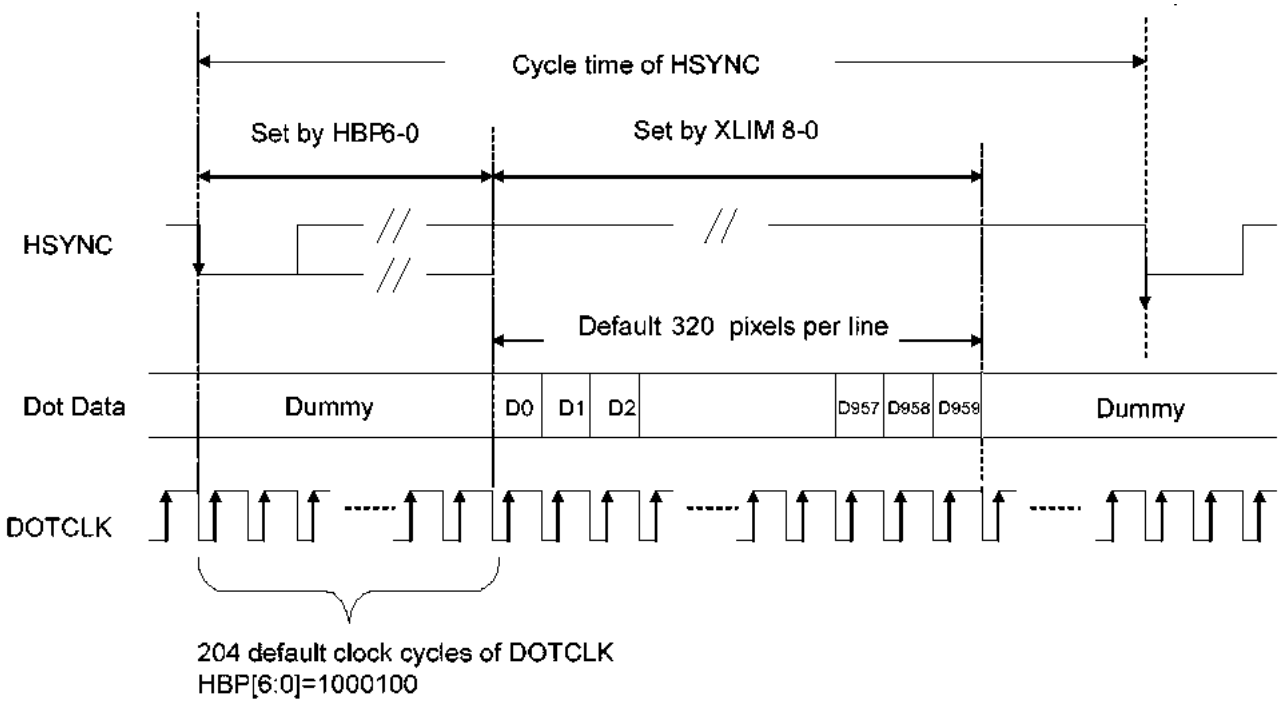


Figure 10.2-18 No. of clock cycle of clock

STH1-0: Adjust the first valid data by dot clock. This setting is not valid in parallel RGB input interface.
STH = 00: +0 dot clock
STH = 01: +1 dot clock
STH = 10: +2 dot clock
STH = 11: +3 dot clock

VBP6-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line. The setting is only effective in SYNC mode timing.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	Can't set
0	0	0	0	0	0	1	Can't set
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
			:				: Step = 1 :
1	1	1	1	1	0	0	124
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Table 10.2-14 No. of clock cycle of HSYNC

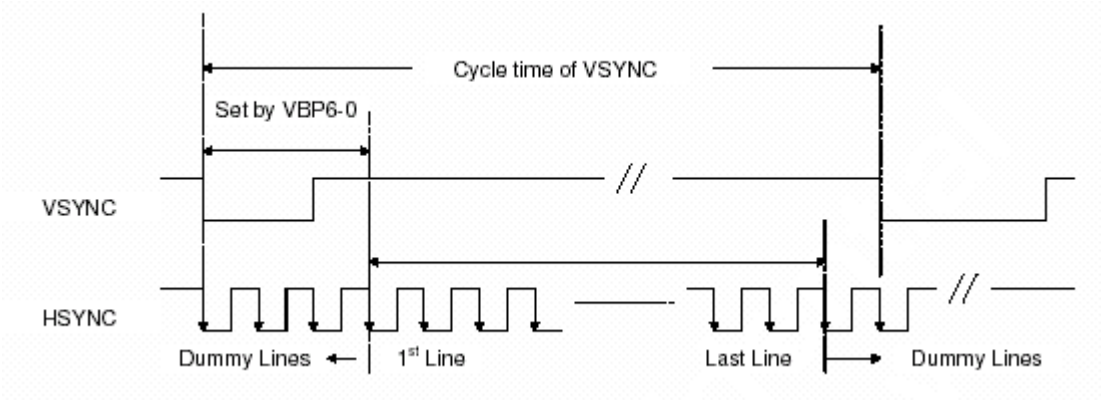


Figure 10.2-19 No. of clock cycle of HSYNC

Power Control 4 (R1Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 10.2-20 Power control 4

nOTP: nOTP equals to “0” after power on reset and VCOMH voltage equals to programmed OTP value. When nOTP set to “1”, setting of VCM6-0 becomes valid and voltage of VCOMH can be adjusted.

VCM6-0: Set the VCOMH voltage if nOTP = “1”. These bits amplify the VCOMH voltage 0.36 to 0.995 times the VLCD63 voltage.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VLCD63 x 0.360
0	0	0	0	0	0	1	VLCD63 x 0.365
0	0	0	0	0	1	0	VLCD63 x 0.370
0	0	0	0	0	1	1	VLCD63 x 0.375
0	0	0	0	1	0	0	VLCD63 x 0.380
			:			:	:
			:				Step = 0.005
			:			:	:
1	1	1	1	1	0	0	VLCD63 x 0.980
1	1	1	1	1	0	1	VLCD63 x 0.985
1	1	1	1	1	1	0	VLCD63 x 0.990
1	1	1	1	1	1	1	VLCD63 x 0.995

Note: $2V < V_{COMH} < V_{LCD63}$

Table10.2-15 VCOMH

Gamma Control 1 (R30h to R37h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1	PKP1	PKP1	0	0	0	0	0	PKP0	PKP0	PKP0
W	1	0	0	0	0	0	PKP3	PKP3	PKP3	0	0	0	0	0	PKP2	PKP2	PKP2
W	1	0	0	0	0	0	PKP5	PKP5	PKP5	0	0	0	0	0	PKP4	PKP4	PKP4
W	1	0	0	0	0	0	PRP1	PRP1	PRP1	0	0	0	0	0	PRP0	PRP0	PRP0
W	1	0	0	0	0	0	PKN1	PKN1	PKN1	0	0	0	0	0	PKN0	PKN0	PKN0
W	1	0	0	0	0	0	PKN3	PKN3	PKN3	0	0	0	0	0	PKN2	PKN2	PKN2
W	1	0	0	0	0	0	PKN5	PKN5	PKN5	0	0	0	0	0	PKN4	PKN4	PKN4
W	1	0	0	0	0	0	PRN1	PRN1	PRN1	0	0	0	0	0	PRN0	PRN0	PRN0

Figure 10.2-21 Gamma control 1

PKP52–00: Gamma micro adjustment registers for the positive polarity output.
PRP12-00: Gradient adjustment registers for the positive polarity output.
PKN52-00: Gamma micro adjustment registers for the negative polarity output.
PRN12-00: Gradient adjustment registers for the negative polarity output.

Gamma Control 2 (R3Ah to R3Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

Figure 10.2-23 Gamma control 2

VRP14-00: Adjustment registers for amplification adjustment of the positive polarity output.
VRN14-00: Adjustment registers for the amplification adjustment of the negative polarity output.
(Refer to Gamma Adjustment Function for details)

10.3 SPI Setting Code

Reg#	Hex Code	Register Bit Value
R01h	XX00	RL = X REV = X PINV = X BGR = X SM = “0” TB = X CPE = X
R02h	0200	B/C = “1”
R03h	6364	DCT= “0110” BT = “011” BTF = “0” DC = “0110” AP = “010”
R04h	04XX	PALM = “1” BLT = ”00” OEA = **Note(2)** SEL = X
R05h		GHN=”1” XDK=”0” GDIS=”1” LPF=”1” DEP=”0” CKP=”1” VSP= **Note(2)** HSP=”0” DEO=”1” DIT=”1” PWM=”0” FB=”100”
R0Ah	4008	BR = “1000000” CON = “01000”
R0Bh	D400	NO = “11” SDT = “01” EQ = “100”
R0Dh	3229	VRC = “011” VDS = “10” VRH = “101001”
R0Eh	3200	VDV = “1001000”
R0Fh	0000	SCN = “00000000”
R16h	9F80	XLIM = “100111111”
R17h		STH = “00” HBP = **Note(2)** VBP = **Note(2)**
R1Eh	0052	nOTP = “0” VCM = “1010010”
R30h	0000	PKP1 = “000” PKP0 = “000”
R31h	0407	PKP3 = “100” PKP2 = “111”
R32h	0202	PKP5 = “010” PKP4 = “010”
R33h	0000	PRP1 = “000” PRP0 = “000”
R34h	0505	PKN1 = “101” PKN0 = “101”
R35h	0003	PKN3 = “000” PKN2 = “011”
R36h	0707	PKN5 = “111” PKN4 = “111”
R37h	0000	PRN1 = “000” PRN0 = “000”
R3Ah	0904	VRP1 = “01001” VRP0 = “0100”
R3Bh	0904	VRN1 = “01001” VRN0 = “0100”

Note: (1) X means the bit is refer to the logic stage of the corresponding hardware pin.
(2) The default values of the VSP 、OEA、HBP、VBP are automatically set by SEL.

Default Value auto setting			VSP	OEA[1:0]	HBP[6:0]	VBP[6:0]
SEL[2:0] = 000	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 001	NTSC		0	01	1000100	0010010
	PAL	PALM=0	0	01	1000100	0010010
		PALM=1				0010010
SEL[2:0] = 010	NTSC		0	01	1000101	0010110
	PAL	PALM=0	0	10	1000101	0011100
		PALM=1				0011000
SEL[2:0] = 011	NTSC		0	01	1000100	0010110
	PAL	PALM=0	0	10	1000111	0011100
		PALM=1				0011000
SEL[2:0] = 100	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100
SEL[2:0] = 101	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 110	NTSC		1	10	1000101	0010001
	PAL	PALM=0	1	10	1001000	0011000
		PALM=1				0010100
SEL[2:0] = 111	NTSC		1	10	1000110	0010001
	PAL	PALM=0	1	10	1000110	0011000
		PALM=1				0010100

Table 10.3-1Registers Default Value

11. GAMMA ADJUSTMENT FUNCTION

The IC incorporates gamma adjustment function for the 262K-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

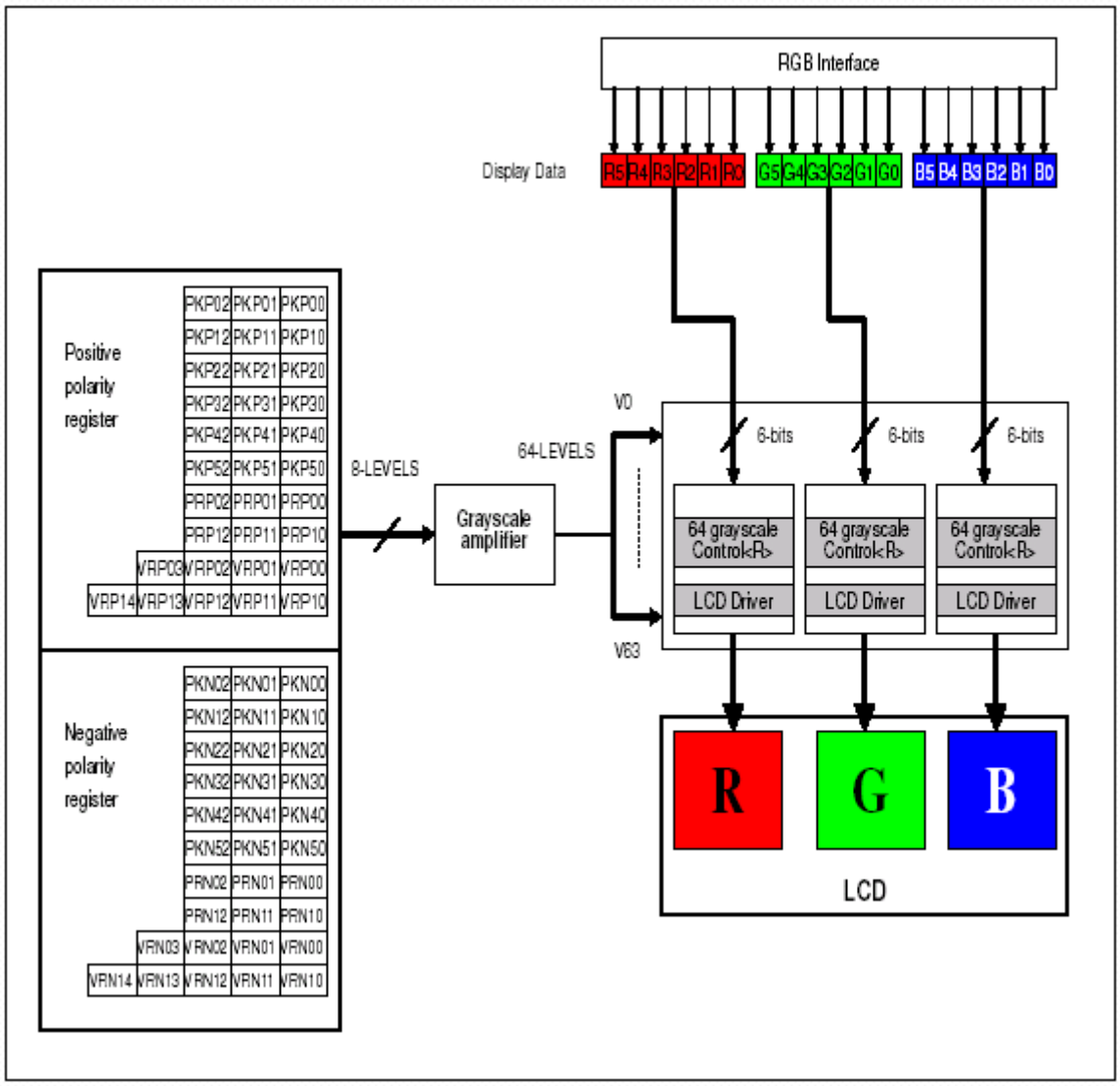


Figure 11-1 Grayscale control block

11.1 Structure of Grayscale Amplifier

Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.

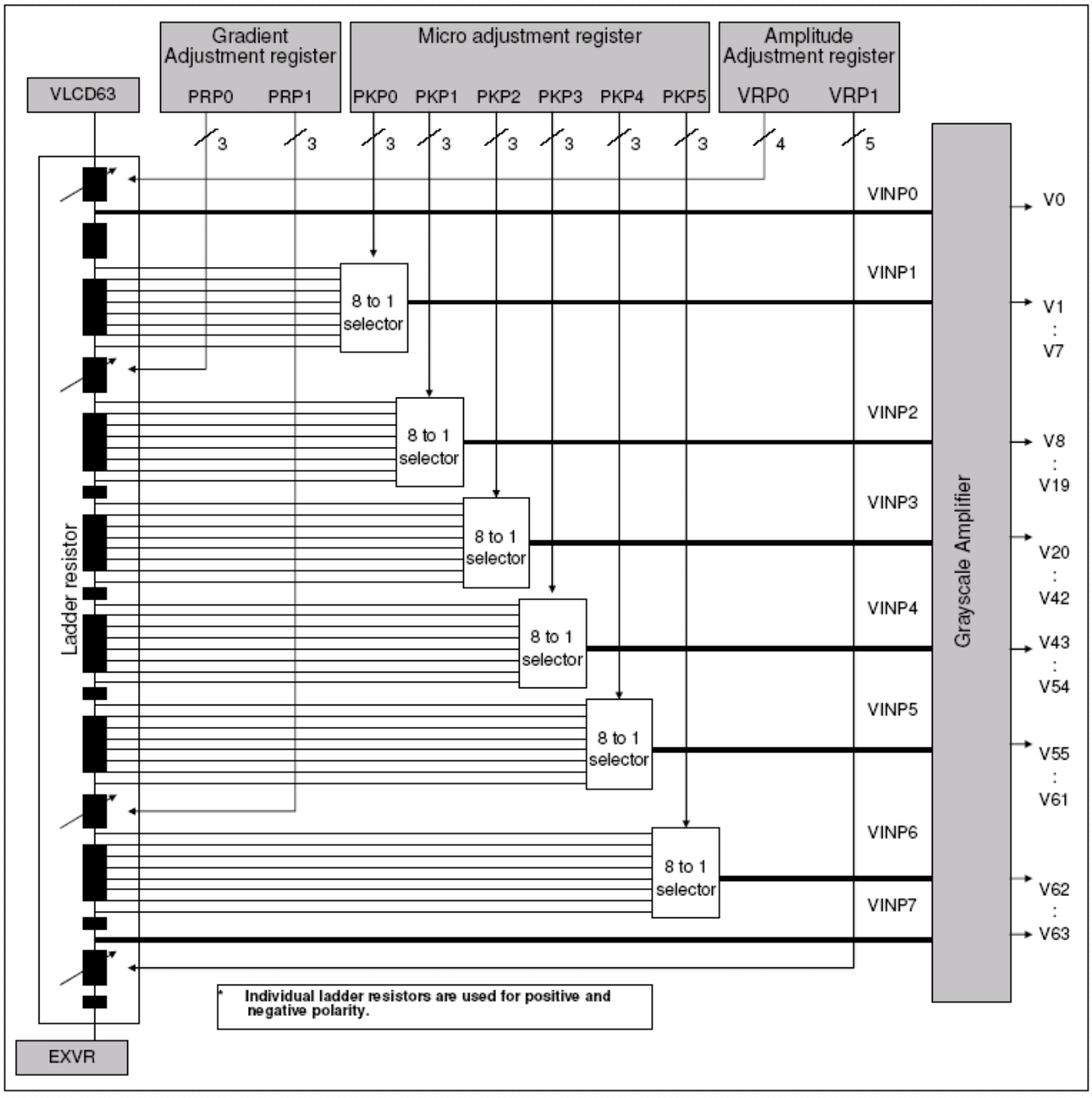


Figure 11.1-1 Grayscale amplifier

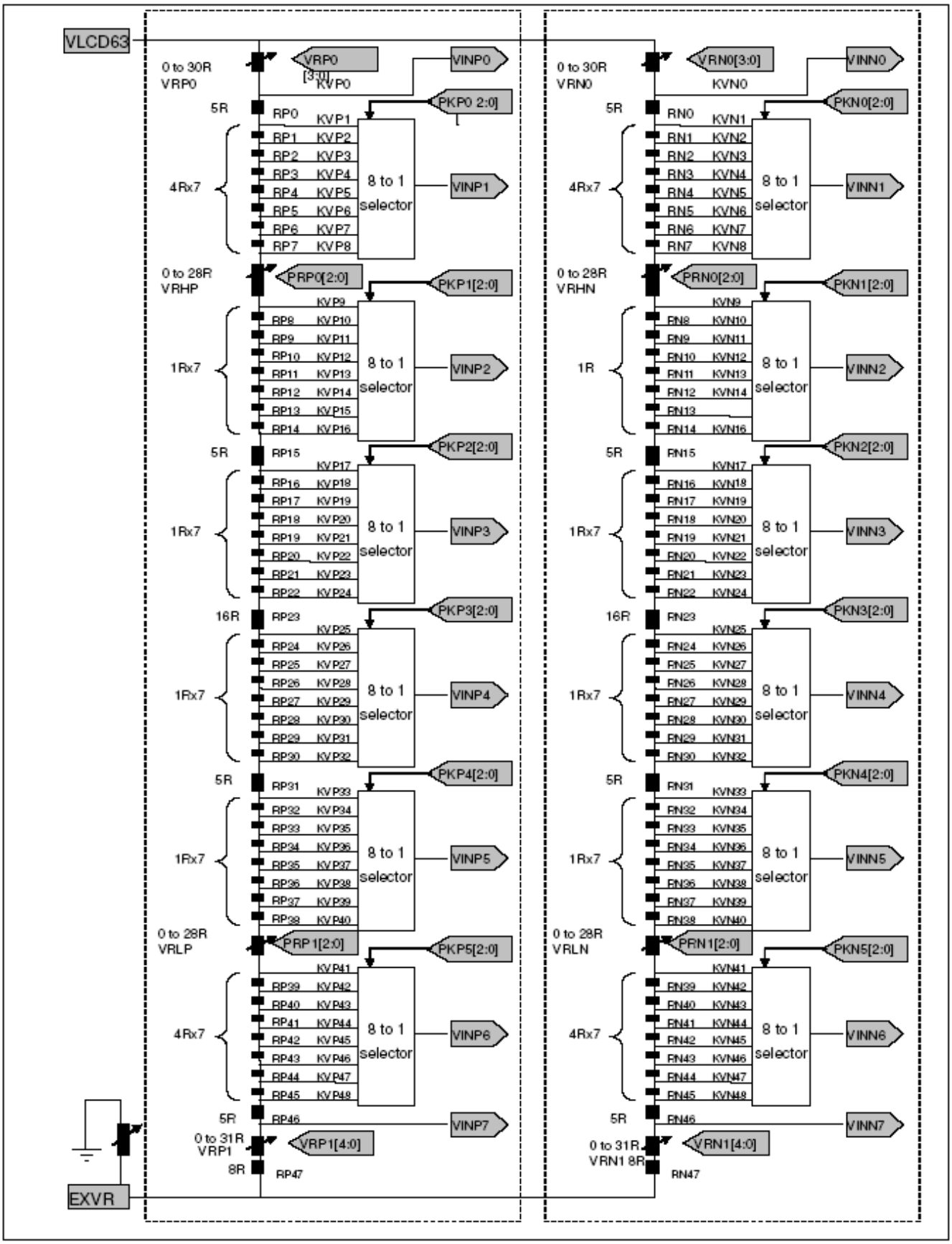


Figure 11.1-2 Resistor Ladder for Gamma Voltages Generation

11.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) following graphics indicates the operation of each adjusting register.

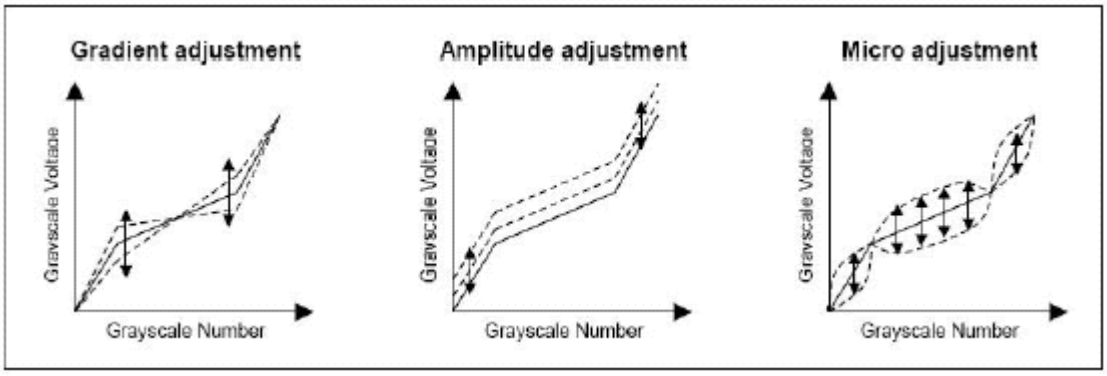


Figure 11.2-1 Gamma adjustment function

11.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

11.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

11.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

11.3 Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors. Also, there has pin (EXVR) that can be connected to VSS or an external variable resistor for compensating the dispersion of length between one panel to another.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 11.2-1 PRP(N)

VRP(N)0	Resistance
0000	0R
0001	2R
0010	4R
: Step=2R :	
1110	28R
1111	30R

Table 11.2-2 VRP(N)0

VRP(N)1	Resistance
0000	0R
0001	1R
0010	2R
: Step=1R :	
1110	28R
1111	30R

Table 11.2-3 VRP(N)1

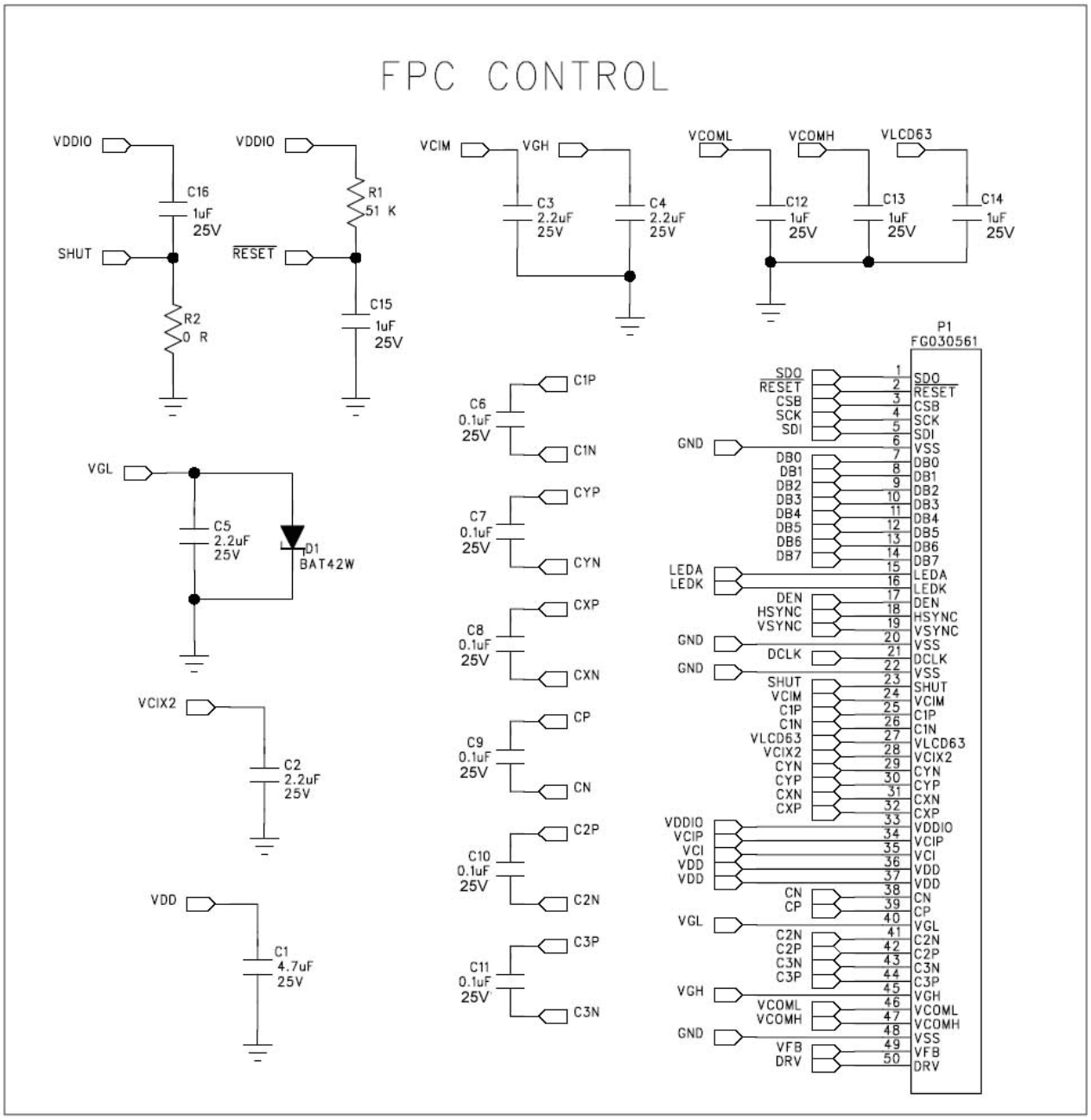
8 to 1 Selector

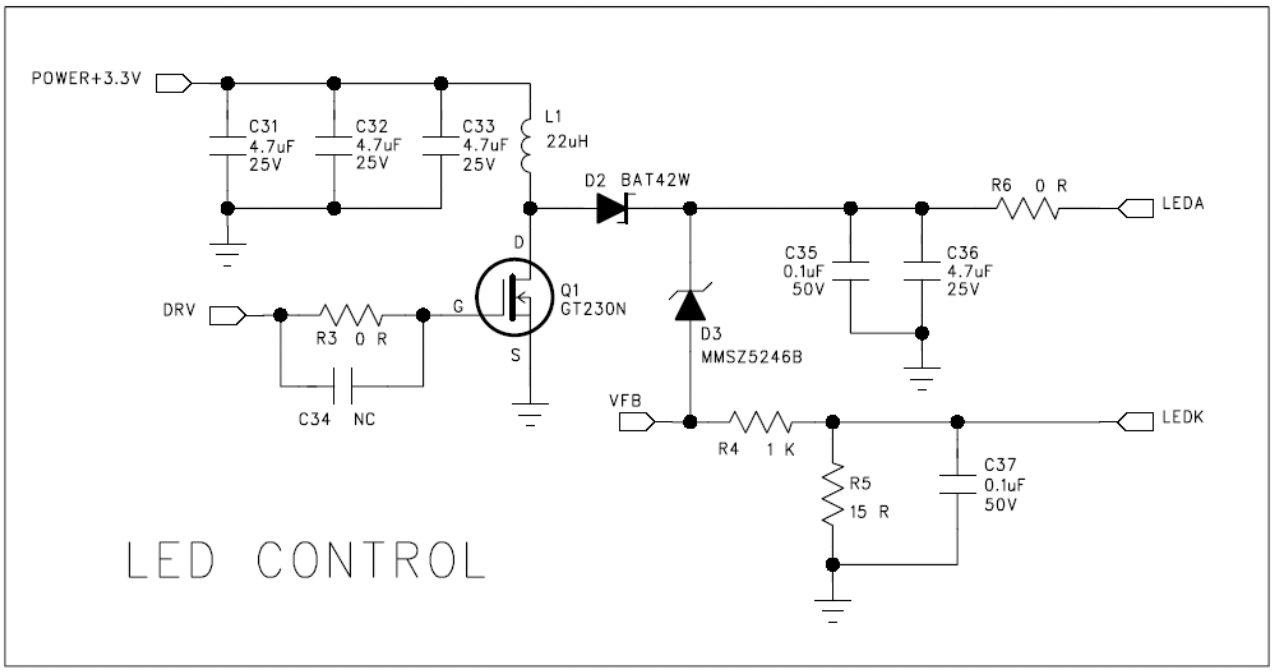
In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro adjusting register and the selecting voltage.

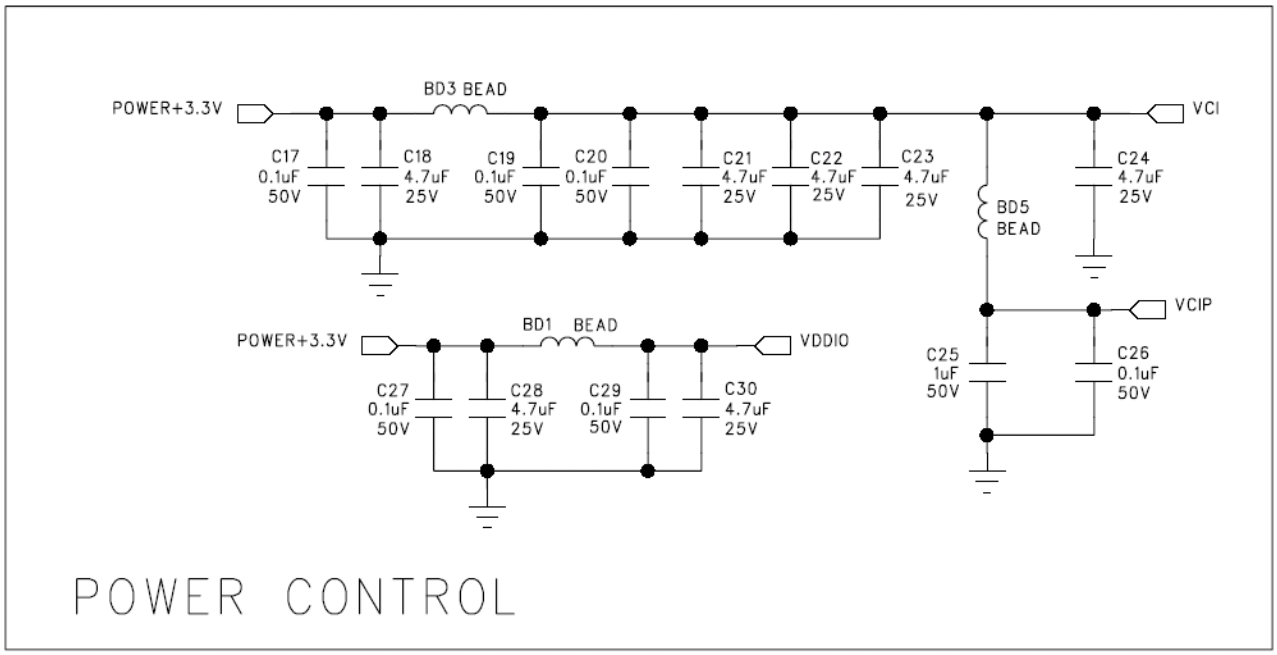
Positive polarity							**Negative polarity**						
Register	**Selected voltage**						**Register**	**Selected voltage**					
PKP[2:0]	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6	**PKN[2:0]**	VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Table11.2-4 PKP and PKN

12. APPLICATION CIRCUIT




POWER+3.3V
C31
4.7uF
25V
C32
4.7uF
25V
C33
4.7uF
25V
L1
22uH
D2 BAT42W
R6 0 R
LEDA
D
Q1
GT230N
G
S
DRV
R3 0 R
C34 NC
D3
MMSZ5246B
C35
0.1uF
50V
C36
4.7uF
25V
VFB
R4 1 K
LEDK
R5
15 R
C37
0.1uF
50V
LED CONTROL


POWER+3.3V
BD3 BEAD
VCI
C17
0.1uF
50V
C18
4.7uF
25V
C19
0.1uF
50V
C20
0.1uF
50V
C21
4.7uF
25V
C22
4.7uF
25V
C23
4.7uF
25V
BD5
BEAD
C24
4.7uF
25V
VCIP
POWER+3.3V
BD1 BEAD
VDDIO
C25
1uF
50V
C26
0.1uF
50V
C27
0.1uF
50V
C28
4.7uF
25V
C29
0.1uF
50V
C30
4.7uF
25V
POWER CONTROL

13 OPTICAL CHARACTERISTICS

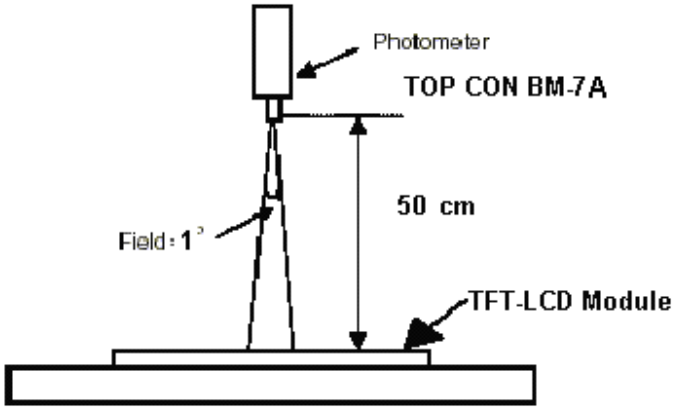
13.1 Specification:

Ta = 25°C

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ_x+	Center CR≥10	60	70	--	deg	Note 1,4
		θ_x-		60	70	--		
	Vertical	θ_Y+		40	50	--		
		θ_Y-		60	70	--		
Contrast Ratio		CR	at optimized viewing angle	200	300			Note 1,3
Response time	Rise	Tr	Center θx=θy =0° IL=40mA	-	15	30	ms	Note 1,6
	Fall	Tf		-	35	50	ms	
Brightness		L		260	330	--	cd/㎡	Note 1,2
Chromaticity		x_W		0.27	0.32	0.37		Note 1,7
		y_W		0.28	0.33	0.38		
Uniformity		B-uni	θx=θy =0°	70	80	--	%	Note1,5

The following optical specifications shall be measured in a darkroom or equivalent state(ambient luminance ≤1 lux, and at room temperature). The operation temperature is 25°C±2°C. The measurement method is shown in Note1.

Note1: The method of optical measurement:

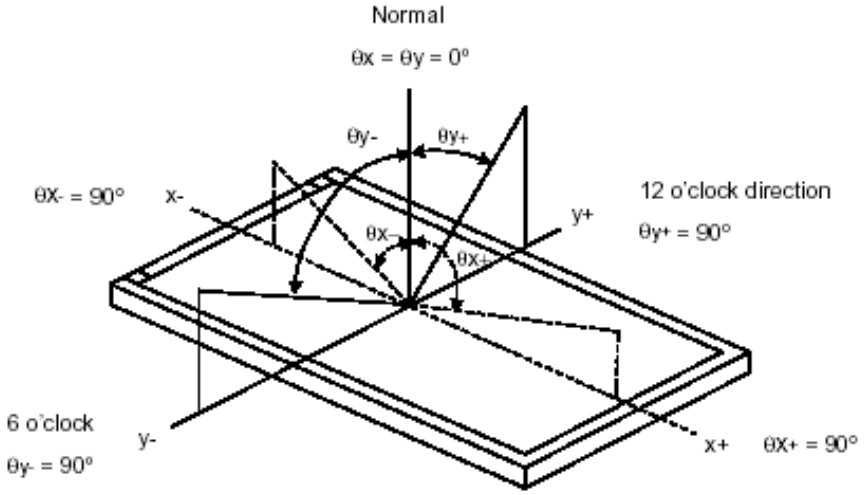


Note2: Measured at the center area of the panel and at the viewing angle of the θx=θy =0°

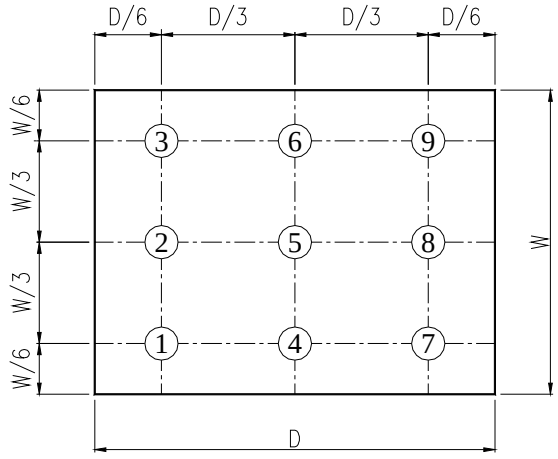
Note3: Definition of Contrast Ratio (CR):

$$CR = \frac{\text{Luminance with all pixels in white state}}{\text{Luminance with all pixels in Black state}}$$

Note4: Definition of Viewing Angle



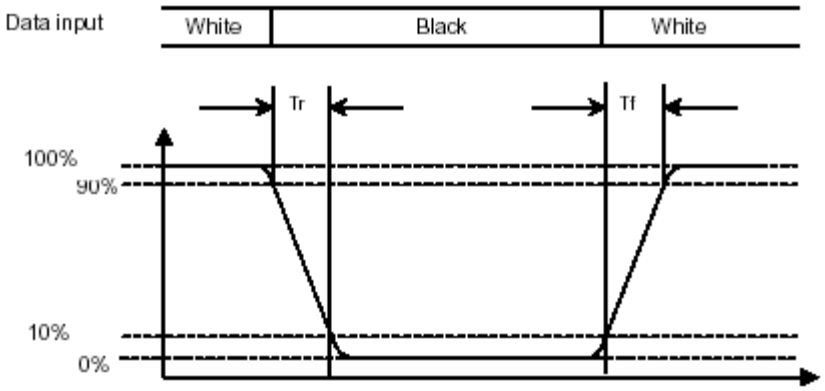
Note 5: Definition of Brightness Uniformity (B-uni):



$$\text{B-uni} = \frac{\text{Minimum luminance of 9 points}}{\text{Maximum luminance of 9points}} \quad \text{(Note 5).}$$

Note6: Definition of Response Time:

The Response Time is set initially by defining the “Rising Time (Tr)” and the “Falling Time (Tf)” respectively. Tr and Tf are defined as following figure.



Note 7: Definition of Chromaticity:

The color coordinate (x_W,y_W) is, are obtained with all pixels in the viewing field at white.

14. TOUCH PANEL CHARACTERISTICS

1.Input Method and Activation Force

Input Method	Average Activation Force
1.6mm dia. Delrin stylus	20~80g
16mm dia. ilicon “finger”	10~60g

2.Typical Optical Characteristics

ITEM	Parameter
Visible Light Transmission	>80%

3. Electrical Specification

ITEM		Parameter
Operating Voltage		DC 5V
Contact current		According to individual design
Circuit close resistance	X	200~900Ω
	Y	200~900Ω
Circuit open resistance		≧20MΩ
Contact bounce		≤10ms
Linear Test		≤1.5%

4.Linearity

ITEM		Parameter
Linear Test Specification Direction	X	0±1.5%
	Y	0±1.5%

5.Specification

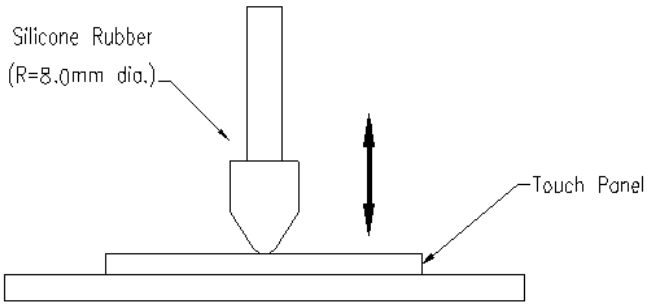
ITEM	Parameter
Operating Temperature	-20°C~+60°C
Storage Temperature	-30°C~+70°C

6.Durability test:

6.1 Finger touches

Touch panel is hit 10 millions times with a silicone rubber of R8 finger, hitting rate is by 250g at 2 times per second. The measurement must satisfy the following:

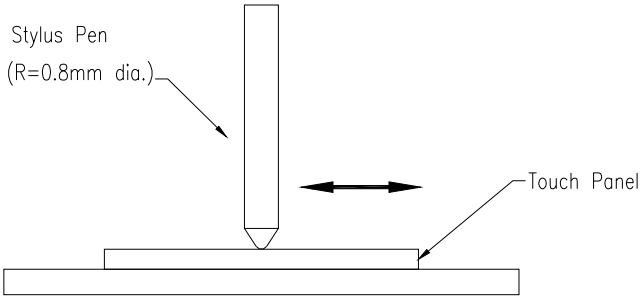
- Circuit close resistance: x 200~900Ω ; y 200~900Ω
- Circuit open resistance: ≧20MΩ
- Contact bounce: ≤10ms
- Linearity test: X: ≤1.5% ;Y: ≤1.5%



6.2 Stylus writing

Touch panel is drawn by R0.8 Derlin stylus pen, at 250g forces, repeat one inch by 100k times. The measurement must satisfy the following:

- Circuit close resistance: x 200~900Ω ; y 200~900Ω
- Circuit open resistance: ≧20MΩ
- Contact bounce: ≤10ms
- Linearity test: X: ≤1.5% ;Y: ≤1.5%



15. QUALITY ASSURANCE

15.1Test Condition

15.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 20 ± 5°C
Humidity : 65 ± 5%

15.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

15.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

15.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

15.1.5 Test Method

No.	Reliability Test Item & Level	Test Level	Remark
1	High Temperature Storage Test	T=70°C,240hrs	IEC68-2-2
2	Low Temperature Storage Test	T=-30°C,240hrs	IEC68-2-1
3	High Temperature Operation Test	T=60°C,240hrs	IEC68-2-2
4	Low Temperature Operation Test	T=-20°C,240hrs	IEC68-2-1
5	High Temperature and High Humidity Operation Test	T=60°C,90%RH,240hrs	IEC68-2-2
6	Temperature Cycle Test (No operation)	-30°C → +25°C → +70°C,50 Cycles 30 min 5min 30 min	IEC68-2-14
7	Vibration Test	Frequency:10 ~ 55 Hz Amplitude:1.5 mm Sweep Time:11min Test Period:6 Cycles for each Direction of X,Y,Z	IEC68-2-6
8	Drop Test	Height:60cm 1 conner,3edges,6surfaces	IEC68-2-32
9	Shock Test	100G,6ms,Direction:±X±Y±Z Cycle:3times	IEC68-2-27
10	ESD Test	State: operating Location: LCM/TP surface Condition:150pf 330Ω Contact +/- 6kV Air +/-8kV Criteria: Class C	IEC61000-4-2

15.2 Judgment standard

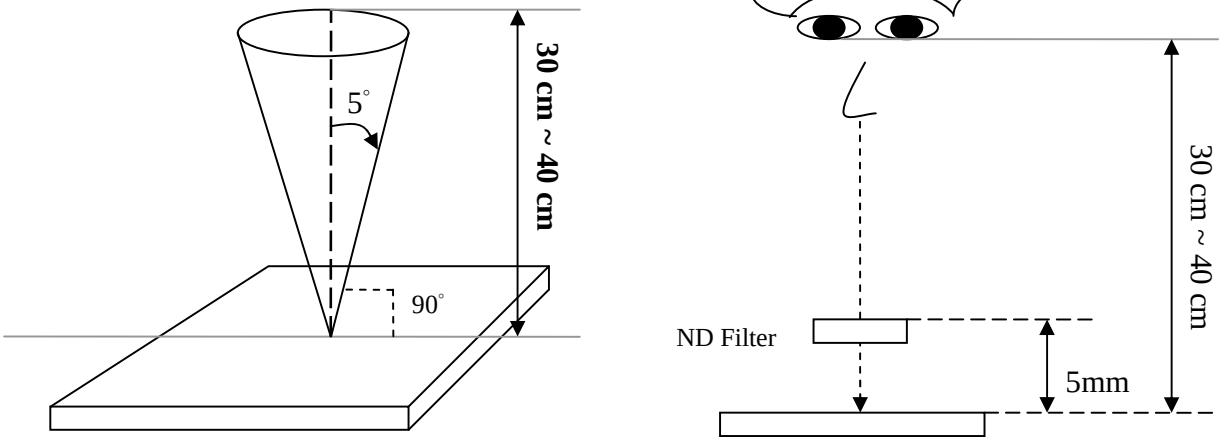
The Judgment of the above test should be made as follow:
Pass: Normal display image with no obvious non-uniformity and no line defect. Partial transformation of the module parts should be ignored.
Fail: No display image, obvious non-uniformity, or line defect.

15.3 Inspection condition

15.3.1 Inspection conditions

15.3.1.1 Inspection Distance : 35 ± 5 cm

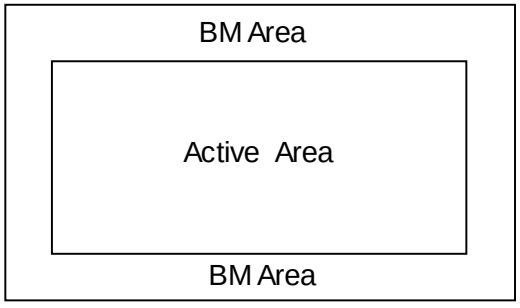
15.3.1.2 View Angle : Inspection under test condition : ±5°



15.3.2 Environment conditions :

Ambient Temperature :		**25±5℃**
Ambient Humidity :		**65±5%**
Ambient Illumination	Functional Inspection	**300~ 500 lux**

15.3.3 Definition of applicable Zones



15.3.4 Inspection Parameters

<table>
<tr><th>No.</th><th>Parameter</th><th>Criteria</th></tr>
<tr><td rowspan="2">1</td><td rowspan="2">Operating</td><td>Display function: No Display malfunction (Major)</td></tr>
<tr><td>Line Defect: No obvious Vertical and Horizontal line defect in bright, dark and colored. (Major) (Note:1)</td></tr>
<tr><td colspan="2"></td><td>Point Defect (Red, green, blue, dark): Active area ≤4dots (Minor)(Note:1)
<table>
<tr><th>Item</th><th>Acceptable number</th><th>Total</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>Bright</td><td>2</td><td rowspan="2">4</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>Dark</td><td>3</td></tr>
<tr><td>Adjacent Bright</td><td>1</td><td>1</td></tr>
<tr><td>Adjacent Dark</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td colspan="2"></td><td>Non-uniformity:
Visible through 2%ND filter white, R, G, B and gray 50%pattern. (Minor)</td></tr>
<tr><td colspan="2"></td><td>Foreign material in Black or White spots shape (W>1/4L) (Note: 5)
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>D ≤ 0.3</td><td>*</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>0.3 < D ≤0.5</td><td>3</td></tr>
<tr><td>D> 0.5</td><td>0</td></tr>
</table>
D = (Long + Short) / 2 ∗ : Disregard</td></tr>
<tr><td colspan="2"></td><td>Foreign Material in Line or spiral shape (W≤1/4L) (Note: 4)
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>W>0.1mm,L>5mm</td><td>0</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>L≦5mm,0.05mm<W≦0.1mm</td><td>3</td></tr>
<tr><td>L≦5mm,W<0.05mm</td><td>*</td></tr>
</table>
L : Length W : Width ∗ : Disregard</td></tr>
<tr><td rowspan="3">2</td><td rowspan="3">External Inspection (non-operating)</td><td>Dimension: Outline (Major)</td></tr>
<tr><td>Bezel appearance: uneven (Minor)</td></tr>
<tr><td>Scratch on the polarize & Touch Panel: (Note:2)
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>W>0.1mm,L>5mm</td><td>0</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>L≦5mm,0.05mm<W≦0.1mm</td><td>3</td></tr>
<tr><td>L≦5mm,W<0.05mm</td><td>*</td></tr>
</table>
L : Length W : Width ∗ : Disregard</td></tr>
<tr><td colspan="2"></td><td>Dent and spots shape on the polarize (Note:2): (Note: 5)
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>D ≤ 0.3</td><td>*</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>0.3 < D ≤0.5</td><td>3</td></tr>
<tr><td>D> 0.5</td><td>0</td></tr>
</table>
D = (Long + Short) / 2 ∗ : Disregard</td></tr>
</table>

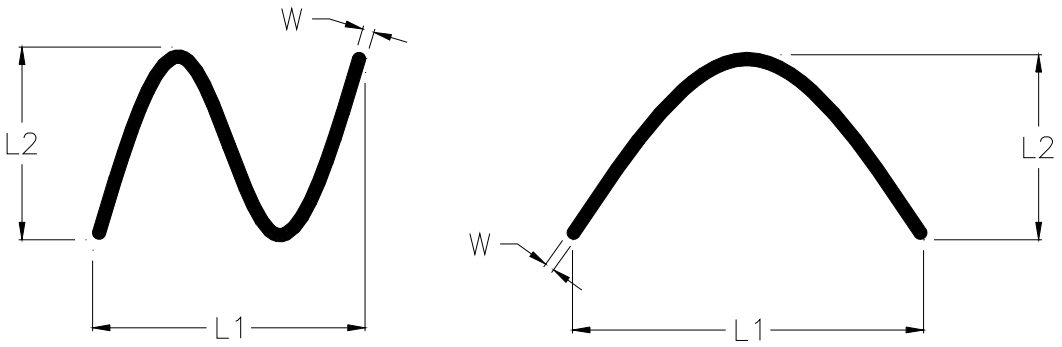
Class of defects	**Major**	AQL 0.65	**Definition** It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.
	Minor	AQL 1.5	It is a defect that will not result in functioning problem with deviation classified.

Note:1.(a)Bright point defect is defined as point defect of R,G,B with area >1/2 dot respectively
(b)Dark point defect is defined as visible in full white pattern.
(c)Definition of distribution of point defect is as follows:
-minumum separation between dark point defects should be larger than 5mm.
-minumum separation between bright point defects should be larger than 5mm.
(d)Definition of joined bright point defect and joined dark point defect are as follows:
-Three or more joined bright point defects must be nil.
-Three joined dark point defects must be nil.
-Coupling of one dark and one bright point in junction is counted as one dark and bright spot with 1 pair maximum.

Note:2 The external inspection should be conducted at the distance 35± 5cm between the eyes of inspctor and the panel .

Note:3 Luminance measurement for contrast ratio is at the distance 50± 5cm between the detective head and the panel with ambient illuminance less than 1 lux. Contrast ratio is obtained at optimum view angle.

Note:4 W-Width in mm , L-length of Max.(L1,L2) in mm.



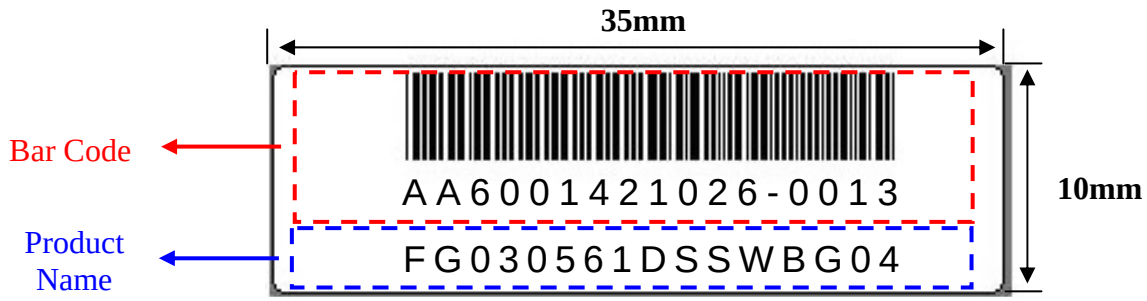
15.4 Sampling Condition

Unless otherwise agree in written, the sampling inspection shall be applied to the incoming inspection of customer.
Lot size: Quantity of shipment lot per model.
Sampling type: normal inspection, single sampling
Sampling table: ISO2859

Inspection level: Level II

16. LCM PRODUCT LABEL DEFINE

Product Label style:

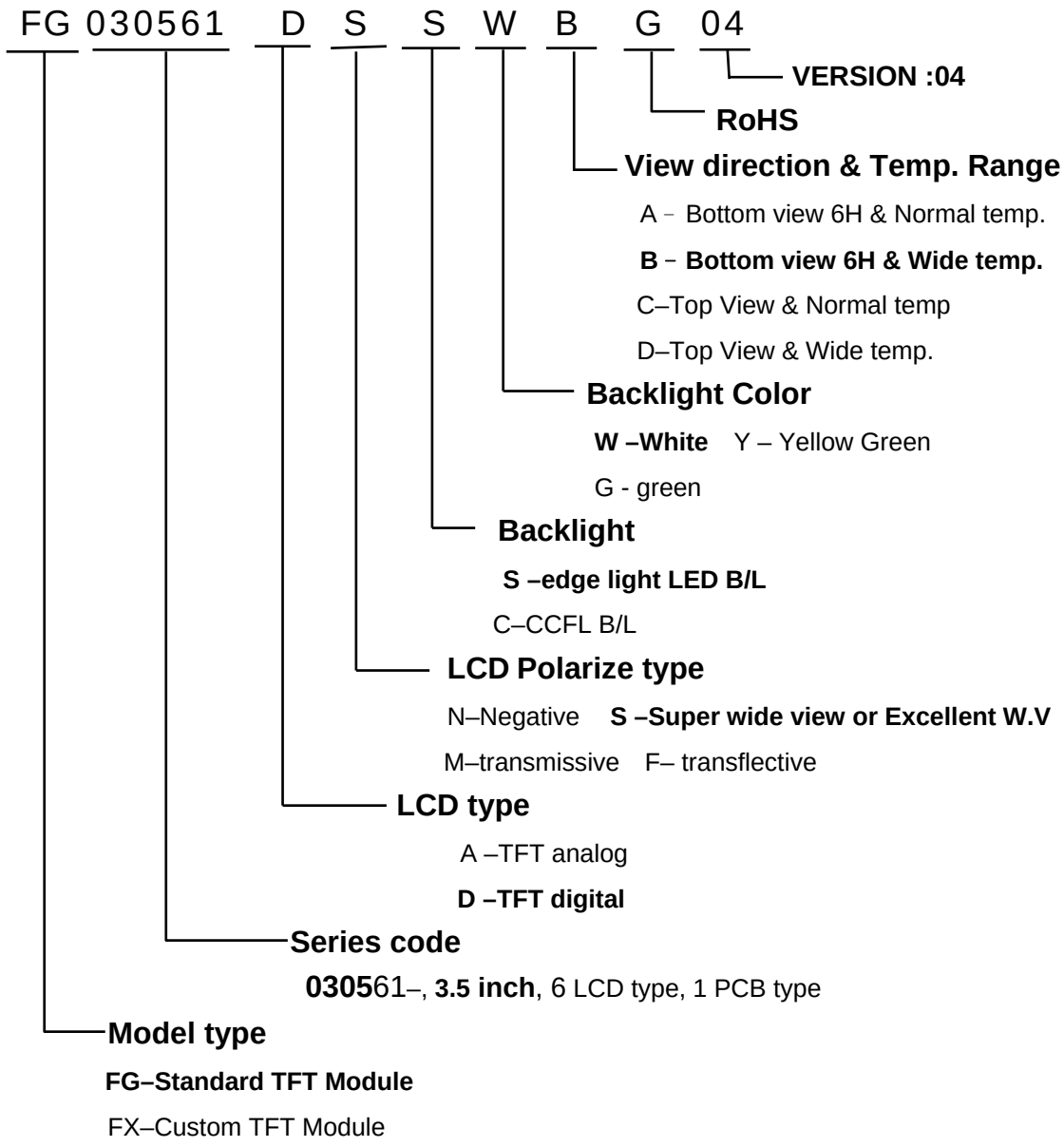


BarCode Define:

A A 6 0014 2 10 26-0013

- **A A** — The first 3 numbers of work order
- **6** — Year of work order
- **0014** — Month of work order
- **2** — Serial number of work order
  Serial number starts from 0000 each month
- **10** — Storage area
- **26** — Year of production
- **-0013** — Week of production
  Serial number of the products
  Serial number starts from 0000
  Every work order is 10K at most

Product Name Define:

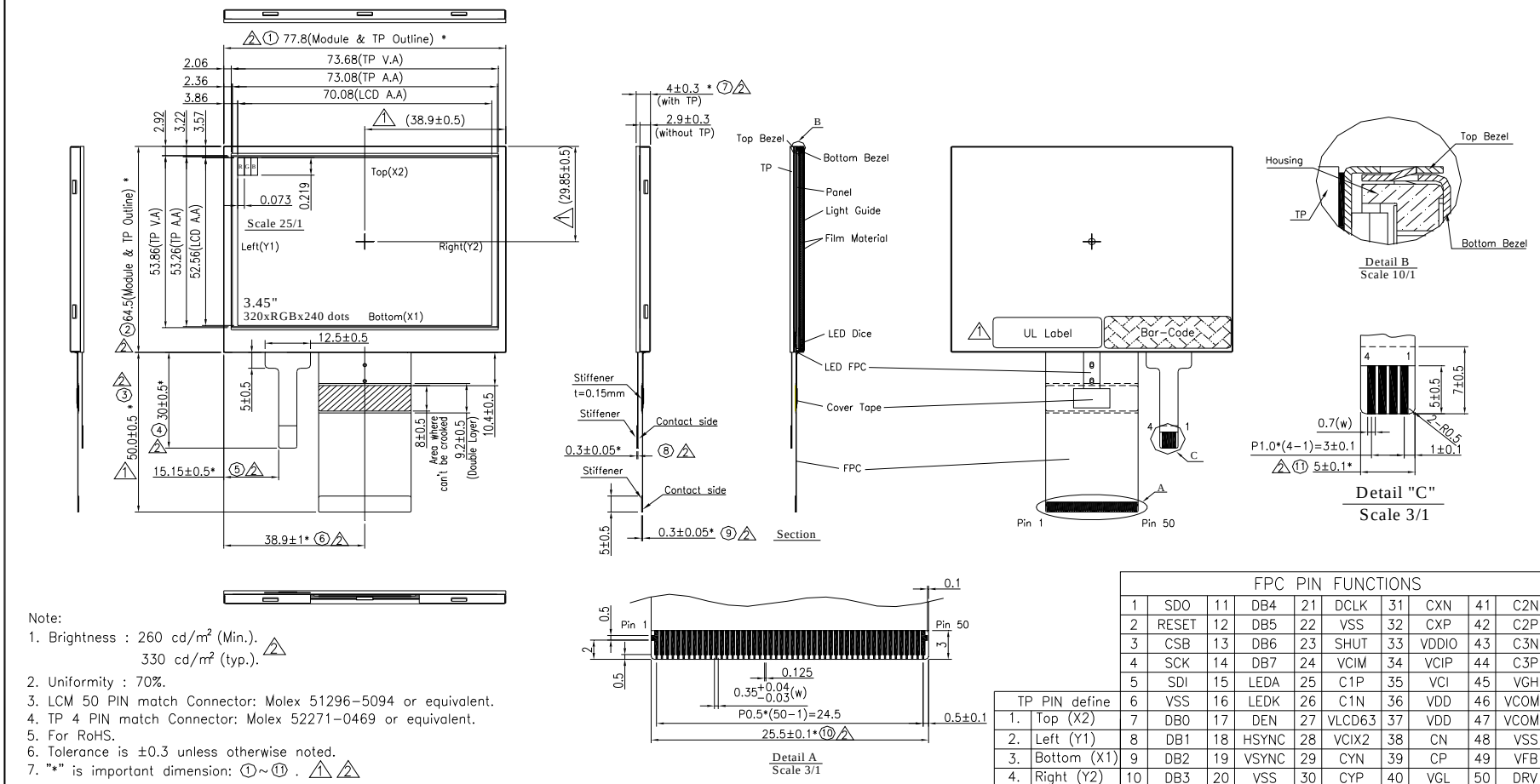


17. PRECAUTIONS IN USE LCM

1. ASSEMBLY PRECAUTIONS
   (1) You must mount a module using holes arranged in four corners or four sides.
   (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
   (3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
   (4) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
   (5) Do not open the case because inside circuits do not have sufficient strength.
   (6) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
   (7) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
   (8) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.
2. OPERATING PRECAUTIONS
   (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
   (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification
   (3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
   (4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
   (5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
   (6) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
3. ELECTROSTATIC DISCHARGE CONTROL
   (1) The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such the copper leads on the PCB and the interface terminals with any parts of the human body.
   (2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
   (3) Only properly grounded soldering irons should be used.
   (4) If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.
   (5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended
   (6) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.
4. STORAGE PRECAUTIONS
   (1) When you store LCDs for a long time, it is recommended to keep the temperature between 0°C-40°C without the exposure of sunlight and to keep the humidity less than 90%RH.
   (2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C 90%RH
   (3) Please do not leave the LCDs in the environment of low temperature; below -20°C.
5. OTHERS
   (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays
   (2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
   (3) For the packaging box, please pay attention to the followings:
      a. Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
      b. Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
      c. Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)
6. LIMITED WARRANTY

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events.

18. OUTLINE DRAWING



Note:
1. Brightness : 260 cd/m² (Min.). 2
   330 cd/m² (typ.).
2. Uniformity : 70%.
3. LCM 50 PIN match Connector: Molex 51296-5094 or equivalent.
4. TP 4 PIN match Connector: Molex 52271-0469 or equivalent.
5. For RoHS.
6. Tolerance is ±0.3 unless otherwise noted.
7. "*" is important dimension: ①~⑪ . 1 2

FPC PIN FUNCTIONS

1	SDO	11	DB4	21	DCLK	31	CXN	41	C2N
2	RESET	12	DB5	22	VSS	32	CXP	42	C2P
3	CSB	13	DB6	23	SHUT	33	VDDIO	43	C3N
4	SCK	14	DB7	24	VCIM	34	VCIP	44	C3P
5	SDI	15	LEDA	25	C1P	35	VCI	45	VGH
6	VSS	16	LEDK	26	C1N	36	VDD	46	VCOML
7	DB0	17	DEN	27	VLCD63	37	VDD	47	VCOMH
8	DB1	18	HSYNC	28	VCIX2	38	CN	48	VSS
9	DB2	19	VSYNC	29	CYN	39	CP	49	VFB
10	DB3	20	VSS	30	CYP	40	VGL	50	DRV

TP PIN define

1.	Top (X2)	
2.	Left (Y1)	
3.	Bottom (X1)	
4.	Right (Y2)	

AUTH	DESCRIPTION	DATE	APPROVED
2	Change LCM Brightness ; Add important dimension number <<ECR 11S-FB0001>>	11/21/15'	
1	Add the UL Label and Note 7 and add tolerance. <<ECR 11S-990032>>	09/02/10'	
	<<ESR 9609016>>		

REVISIONS

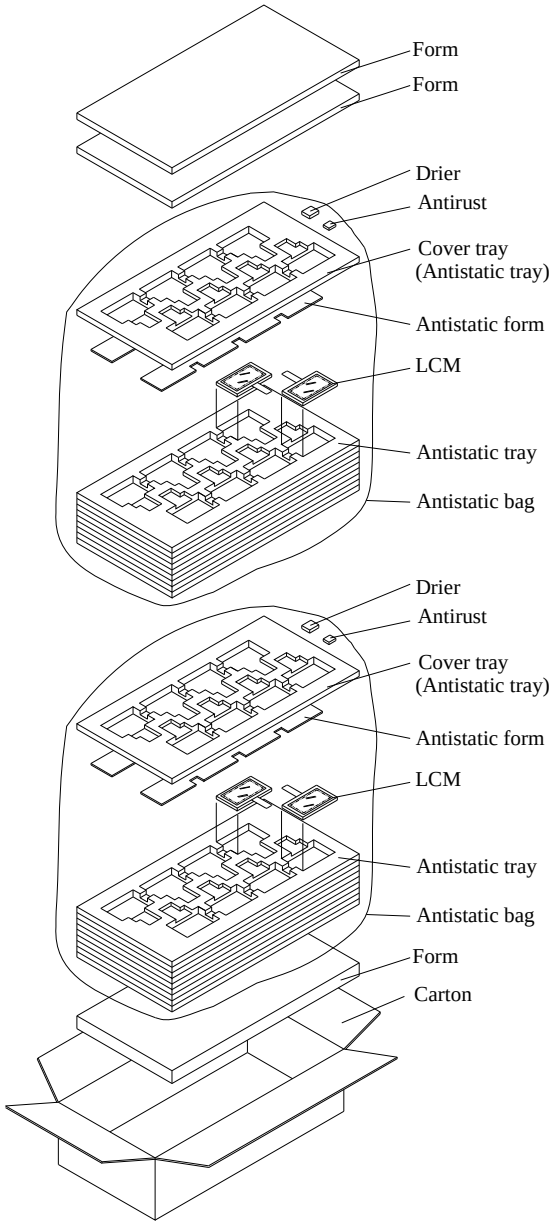
DATE:	09/22/07'
DRAWN:	
CHECK:	
APPROVE:	

TITLE: LCM OUTLINE DIMENSION

DWG. NO.	FG030561SG04		
UNITS M M		REV.	3
SCALE 1 / 1	SHEET 1 OF 1		

DATA IMAGE

19. PACKAGE INFORMATION



Material

1 Carton + 2 Anti-static bag + 2 Form(15mm) + 1 Form(35mm)
+ 20 Anti-static tray + 2 Drier + 2 Antirust

Total pcs

1 Antistatic tray = 8 panel pcs

1 Anti-static bag = 9 Anti-static tray + cover tray = 9*8 +1*0 = 72 pcs

1 Carton = 2 Anti-static bag = 2*72 = 144 pcs

1 Carton = 144 pcs

Carton size : 485L x 282W x 279H (mm)

Total Weight ≒8.5 kgw

FG030561 TFT LCM PACKING