DATA IMAGE CORPORATION

TFT Module Specification
Preliminary
ITEM NO.: **FG0208F1DSSWDG01**

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Customer Companies	R&D Dept.	Q.C. Dept.	Eng. Dept.	Prod. Dept.
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2. RECORD OF REVISION

Rev	Date	Item	Page	Comment
1	16/NOV/11’			Initial Preliminary

3. GENERAL SPECIFICATIONS

The FG0208F1DSSWDG01 is a kind of Tran missive TFT, active matrix color liquid crystal display (LCD) comprising an amorphous silicon TFT attached to each signal electrode. This module is consisting of TFT-LCD module, a driver circuit, a back-light unit, The resolution of a 2.8'' contains 240(RGB)x320 pixels and can display up to 262k colors.

Parameter		Specifications	Unit
Screen Size		2.8" (diagonal)	inch
Pixel configuration		RGB Stripe	
Display Format		240(RGB) X 320	Dot
Active Area		57.6(W) x43.2 (H)	mm
Pixel Size		0.18(W) x0.18(H)	mm
Outline Dimension		68.1(W)x49(H)x4.0(T)	mm
Viewing direction		12 o'clock	
Surface Treatment		Glare	
Temperature Range	Operation	-20~70	°C
	Storage	-30~80	°C

4. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	MIN.	Typ.	MAX.	Unit	Comment
Power supply Voltage	VDD	-0.3	--	+4.6	V	Notes 1,2

Notes:
1.If the LSI is used above these absolute maximum ratings, it may become permanently damaged.
Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation.
If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.
2. VDD,GND must be maintained.

5. ELECTRICAL CHARACTERISTICS

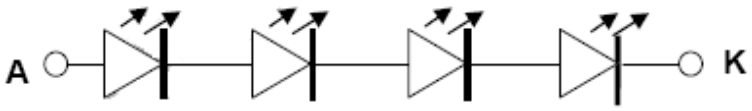
GND=0V,Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply Voltage	VDD	2.5	2.8	3.3	V	
Input high voltage	VIH	0.7VDD	--	VDD	V	
Input low voltage	VIL	GND	--	0.3VDD	V	
Current consumption	I_{DD}	--	9	--	mA	

5.1. Backlight driving for power conditions

Item	Symbol	Min.	Typical	Max.	Unit	Remark
LED module Forward voltage	VLED	9.6V	12.4	15V	V	
LED module current	ILED	--	20	--	mA	
LED life time		10,000			Hours	Note 1

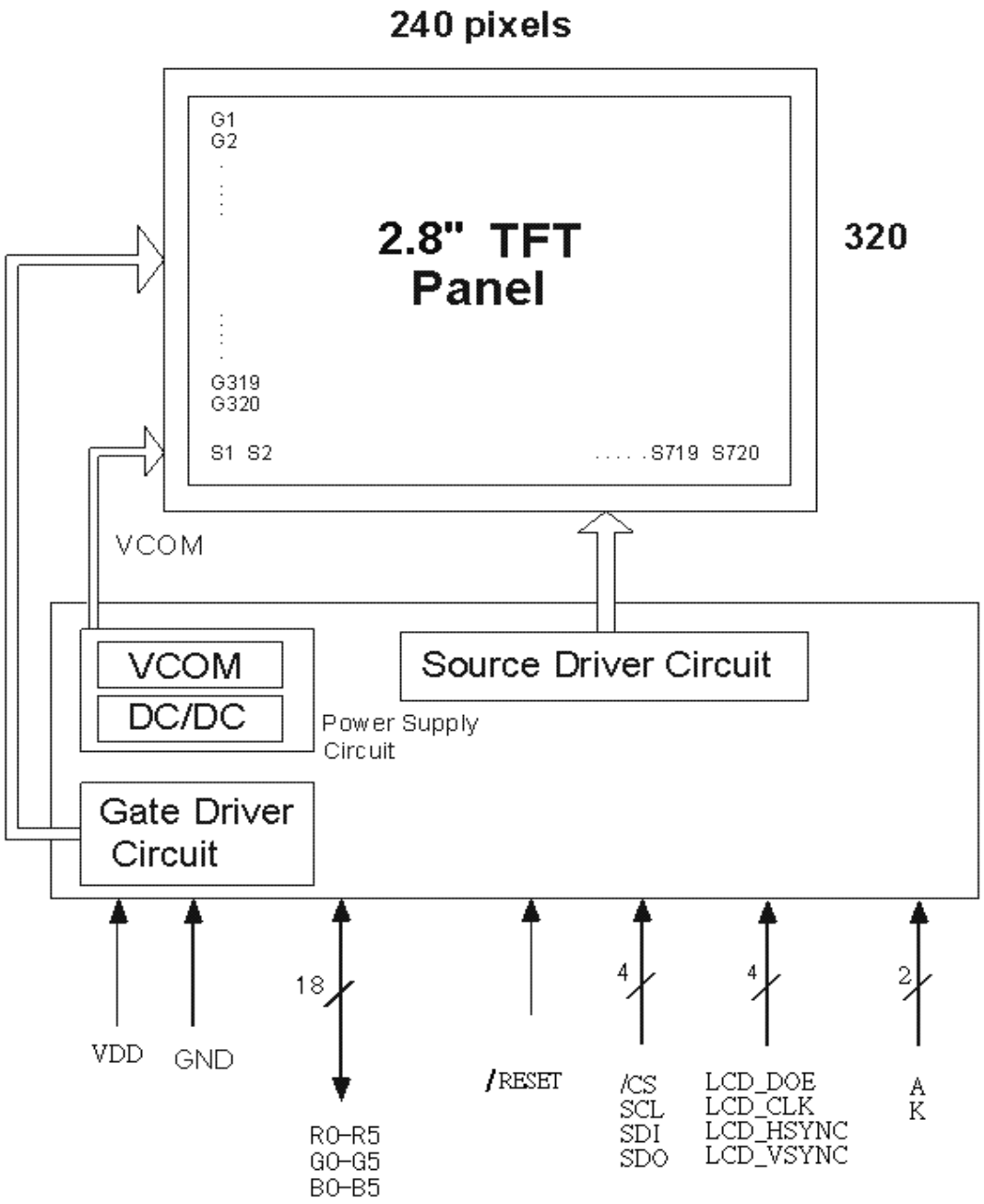
Note 1 The “LED dice life time” is defined as the brightness decrease to 50% original brightness that the ambient temperature is 22℃ and LED dice current=20mA.



6. PIN CONNECTIONS

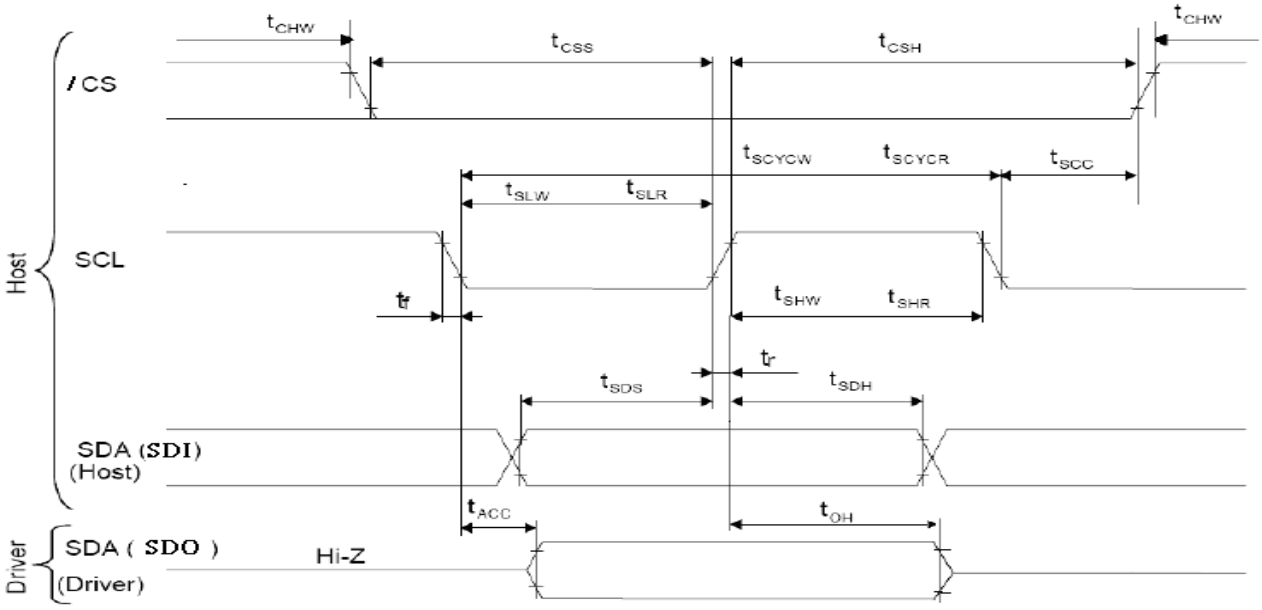
Pin No	Symbol	Description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	TAMPER	Wire to pin 42
5	GND	Ground
6	VDD	power source
7	VDD	power source
8	/CS	Chip select pin
9	SCL	SCL：SPI clock signal
10	SDI	SPI input pin
11	SDO	SPI output pin
12	GND	Ground
13~18	B(0~5)	Blue data
19	GND	Ground
20~25	G(0~5)	Green data
26	GND	Ground
27~32	R(0~5)	Red data
33	GND	Ground
34	LCD_DOE	Data ENABLE signal
35	GND	Ground
36	LCD_CLK	Dot clock signal
37	GND	Ground
38	LCD_HSYNC	Line synchronizing signal
39	LCD_VSYNC	Frame synchronizing signal
40	/RESET	System Reset signal
41	GND	Ground
42	TAMPER _Signal	Wire to pin 4
43	A	LED anode (A)
44	K	LED cathode (K)
45	GND	Ground

7. BLOCK DIAGRAM



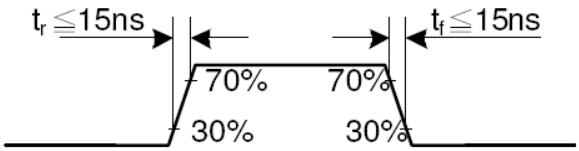
8. AC Characteristics

8.1. Display Serial Interface Timing Characteristics (3-line SPI system)

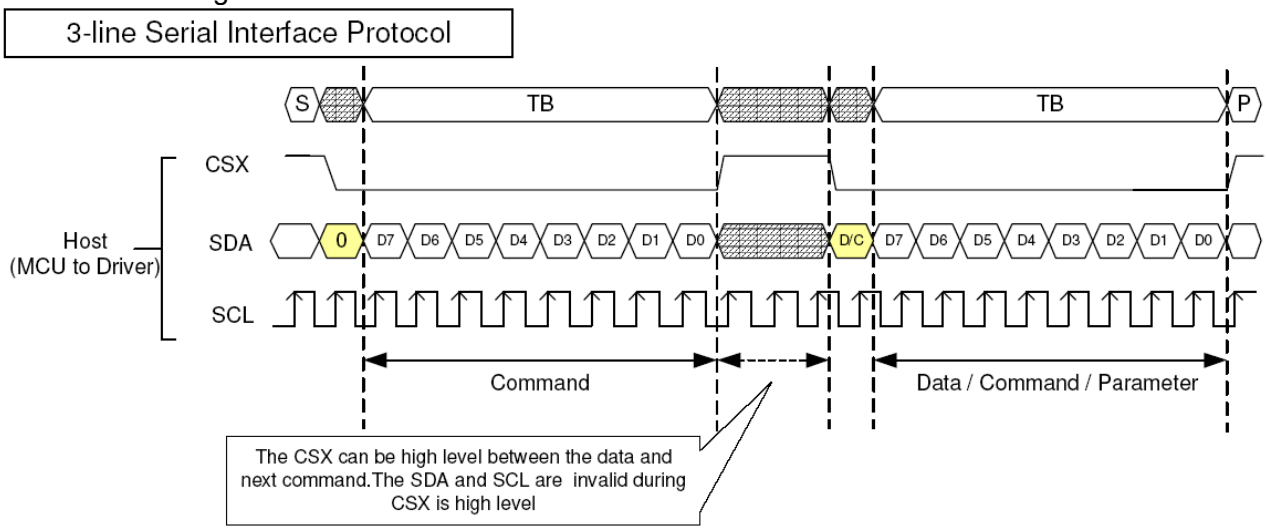


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
/CS	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 ℃, VDD = 2.5 *V to 3.3V*



Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9341 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.



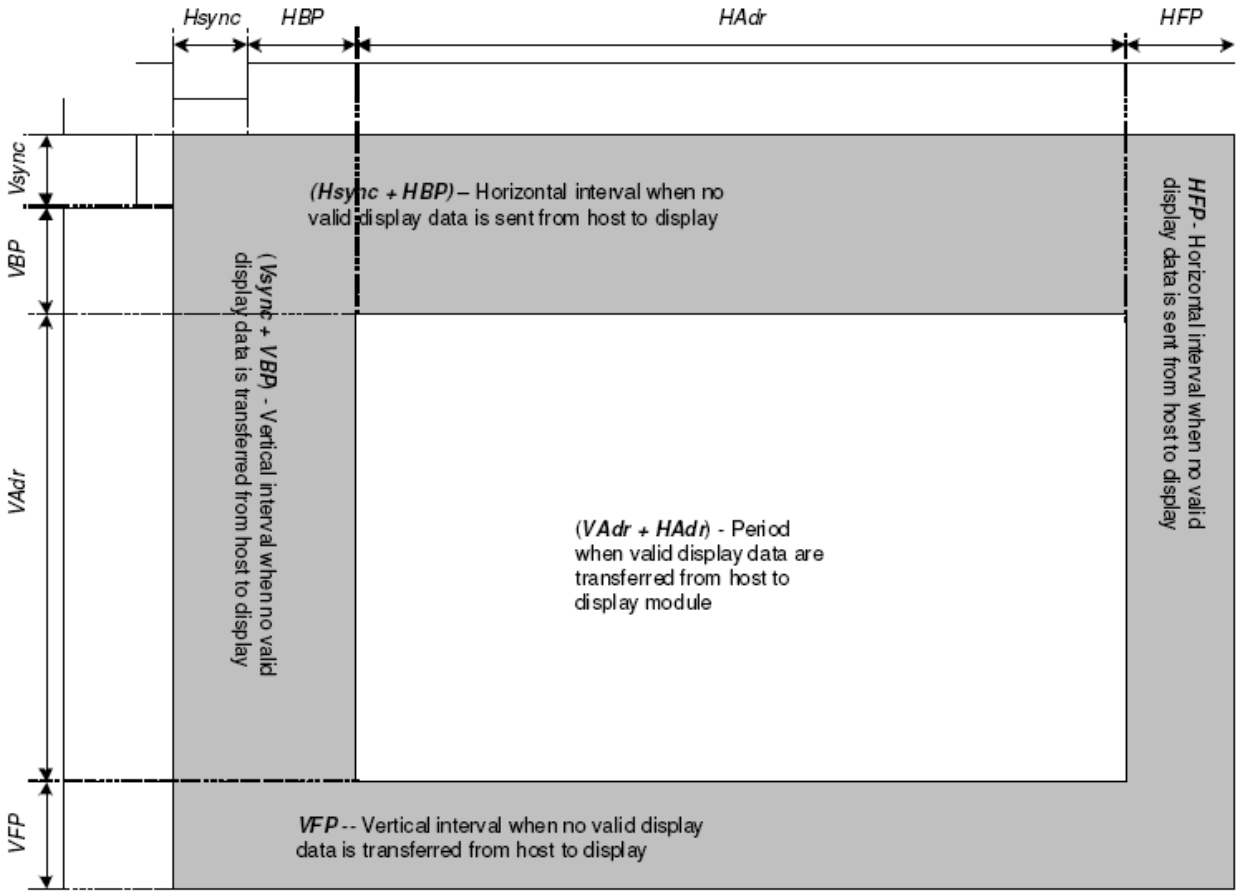
8.2. RGB Interface Characteristics

8.2.1 RGB Interface data

18-bit data bus interface

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.
Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.
In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of DOTCLK). D [17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Typical values are setting example when used with panel resolution 240 x 320 (QVGA), clock frequency 6.35MHz and frame frequency about 70Hz.

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

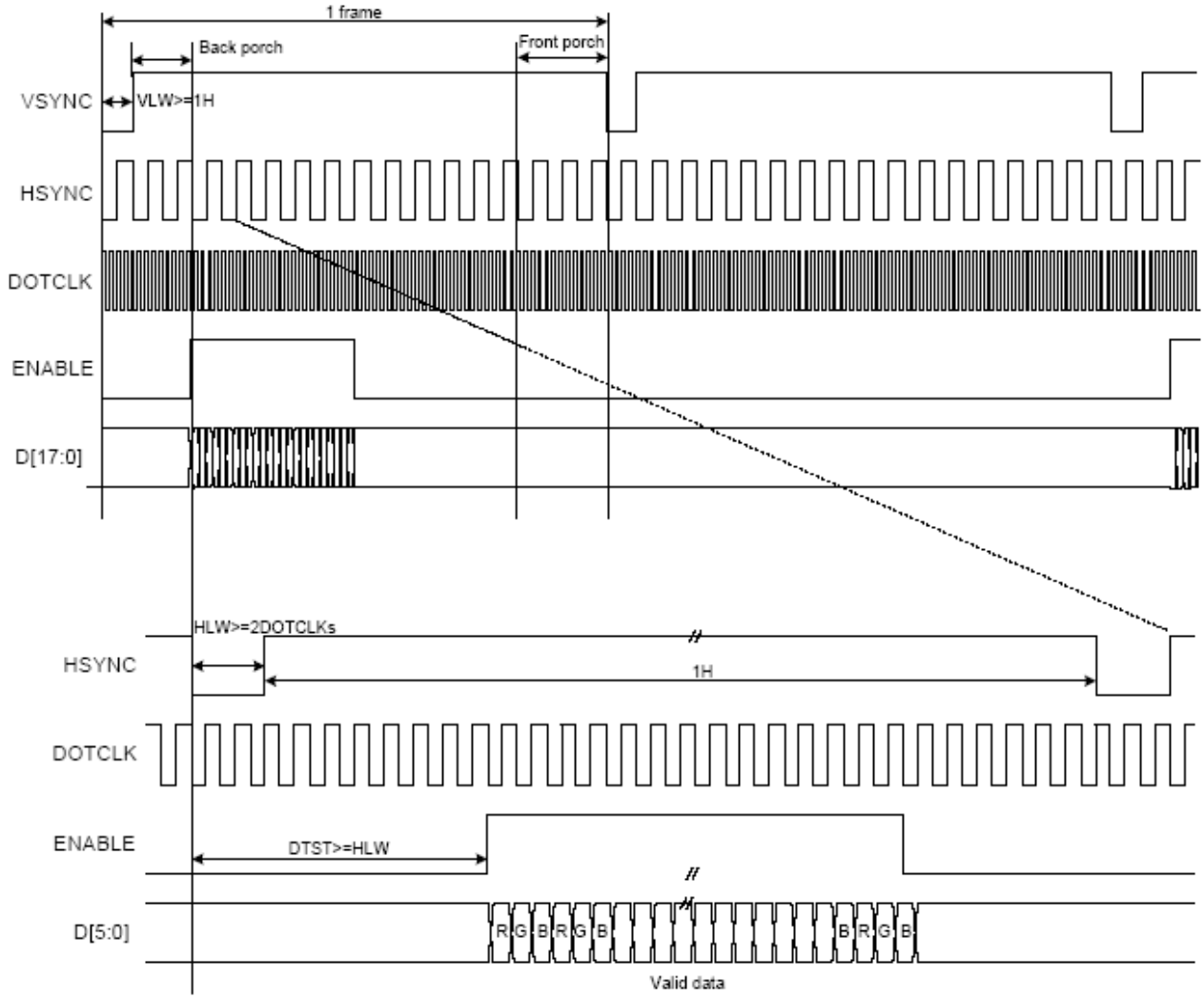
(Number of PCLK per 1 line) G (Number of RTN clock) x Division ratio (DIV) x PCDIV

Setting Example for Display Control Clock in RGB Interface Operation

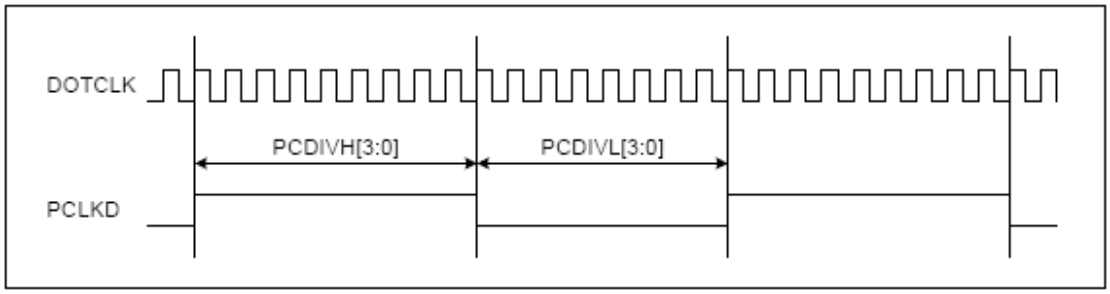
Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

8.2.2 RGB Interface Timing

The timing chart of 18-bit RGB interface mode is shown as below.

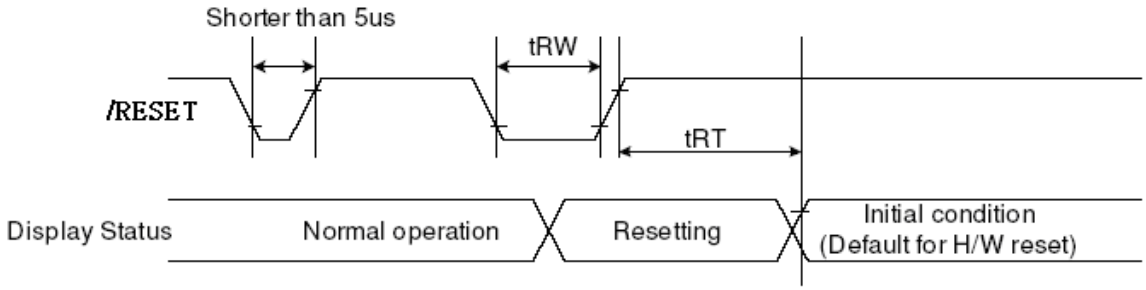


VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

8.2.3. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
/RESET	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

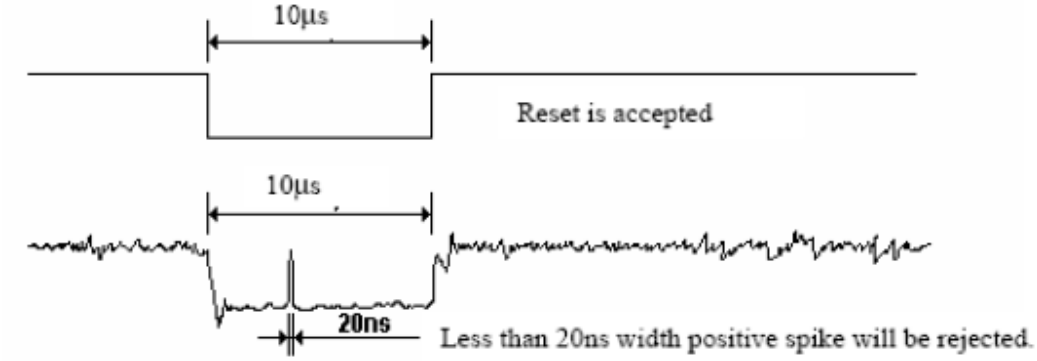
Note 1: The /reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of /RESET.

Note 2: Spike due to an electrostatic discharge on /RESET line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

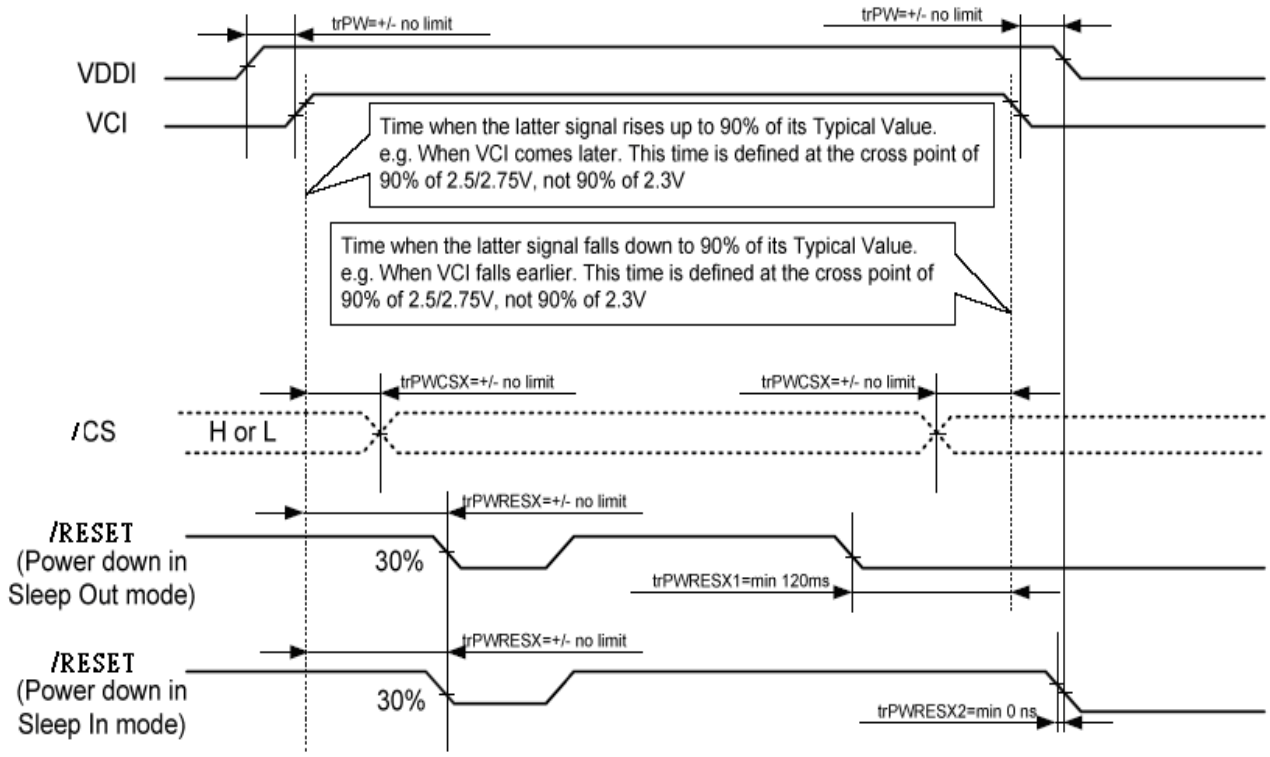
Note 7: It is necessary to wait 5msec after releasing /RESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

8.2.4. Power ON/OFF Sequence

VDD can be applied in any order.
VDD can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VDD must be powered down minimum 120msec after /RESET has been released.
During power off, if LCD is in the Sleep In mode, VDD can be powered down minimum 0msec after /RESET has been released.
/CS can be applied at any timing or can be permanently grounded. /RESET has priority over /CS.
Note 1: There will be no damage to the display module if the power sequences are not met.
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
Note 4: If /RESET line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (/RESET) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

8.2.4.1 Case 1 – /RESET line is held High or Unstable by Host at Power ON

If /RESET line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

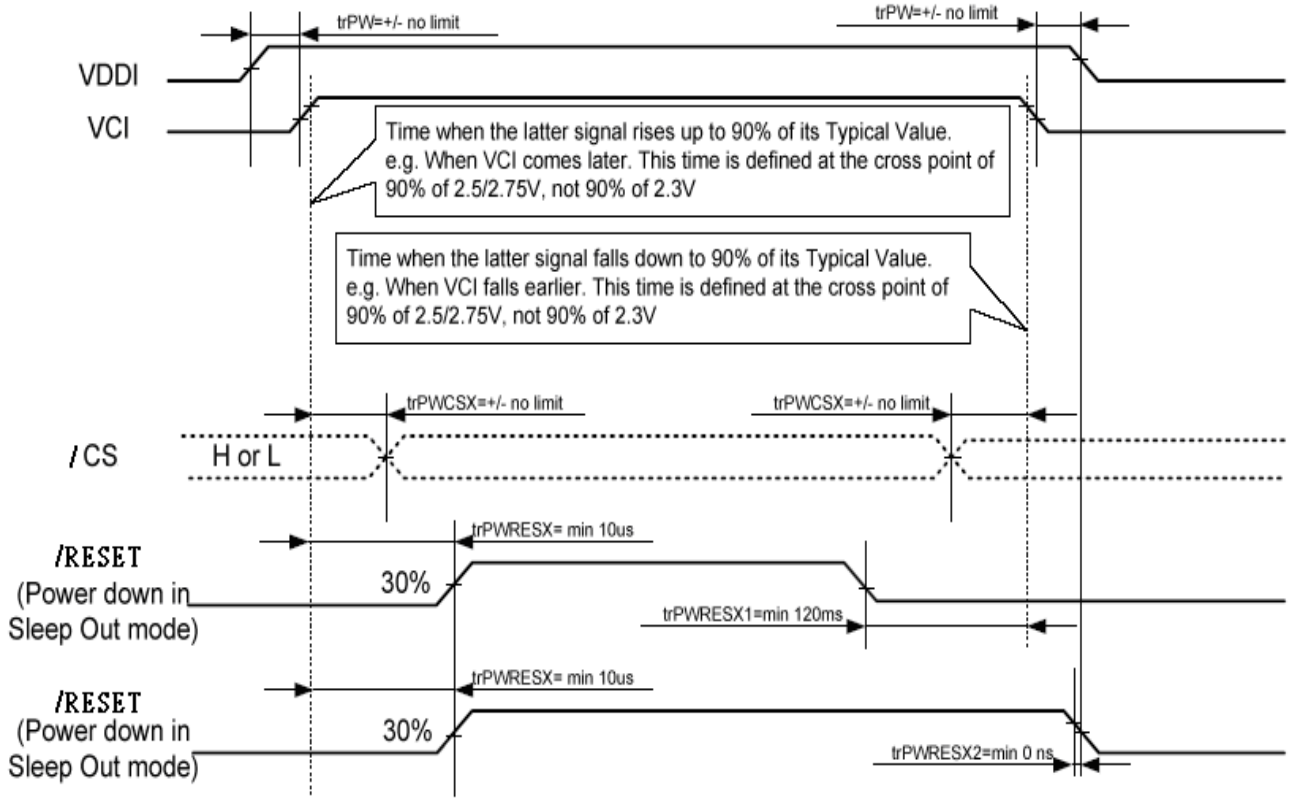


trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: VDDI and VCI connect to VDD.

8.2.4.2 Case 2 – /RESET line is held Low by Host at Power ON

If /RESET line is held Low (and stable) by the host during Power On, then the /RESET must be held low for minimum 10μsec after both VDD have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

Note 2: VDDI and VCI connect to VDD.

8.2.4.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9341 will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” actives.

9. OPTICAL CHARACTERISTICS

Item		Symbol	Conditions	Specifications			Unit	Note
				Min.	Typ.	Max.		
Brightness		B	Center, θ x= θ y=0°	160	200	--	Cd/m^2	Note: 4,5
Uniformity					85		%	Note: 4,5
Contrast Ratio		CR	Center θ x= θ y=0°	--	300	--		Note: 1,4
Response Time		Ton+ Toff		--	30	--	ms	Note: 2
Chromaticity	Red	XR		--	TBD	--	--	Note: 4
		YR		--	TBD	--	--	
	Green	XG		--	TBD	--	--	
		YG		--	TBD	--	--	
	Blue	XB		--	TBD	--	--	
		YB		--	TBD	--	--	
	White	XW		0.244	0.294	0.344	--	
		YW		0.284	0.334	0.384	--	
Viewing Angle	Hor.	θ x+	Center CR≥10	--	45	--	deg.	Note: 3,4
		θ x-		--	45	--		
	Ver.	θ y+		--	45	--		
		θ y-		--	20	--		

Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression. Contrast Ratio (CR) = L63 / L0

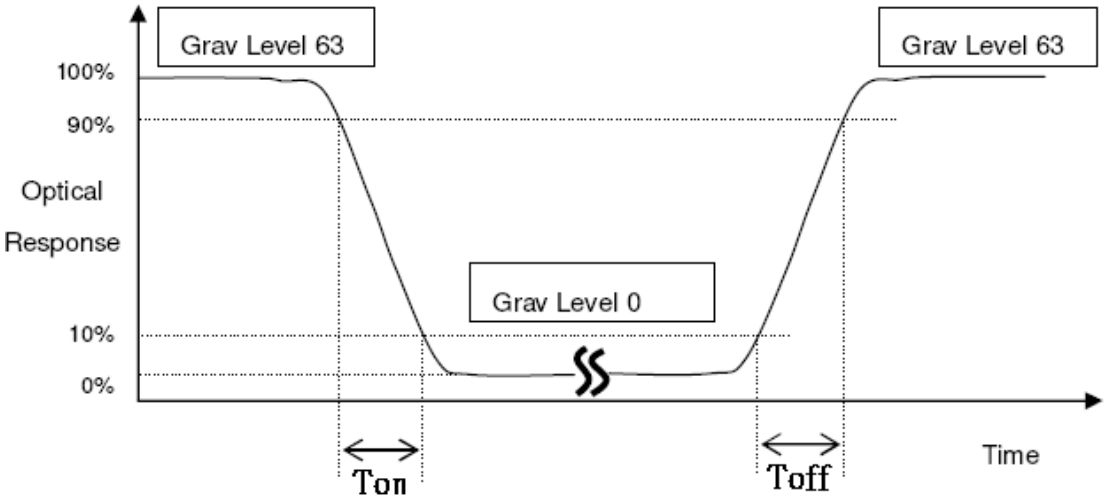
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

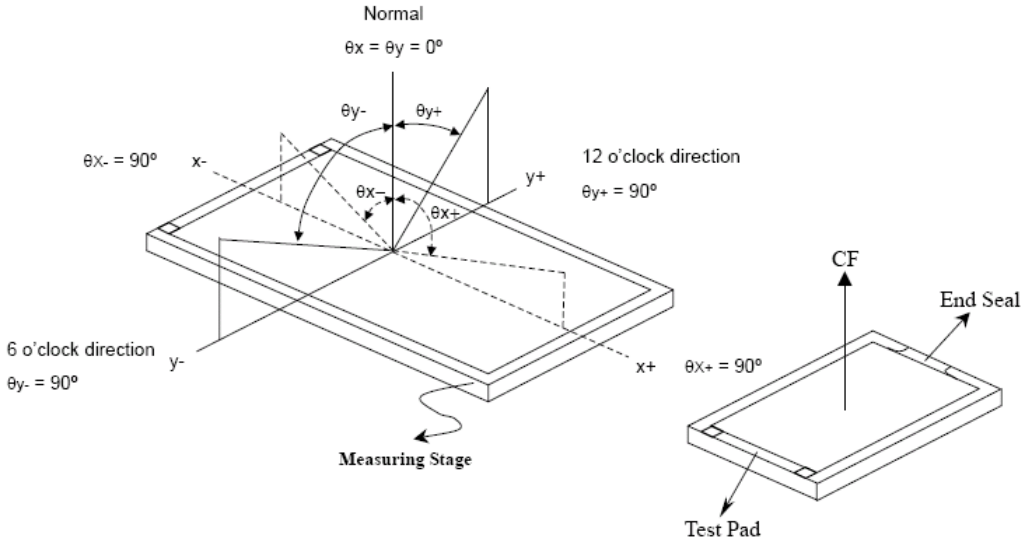
CR =CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

Note (2) Definition of Response Time (Ton, Toff):

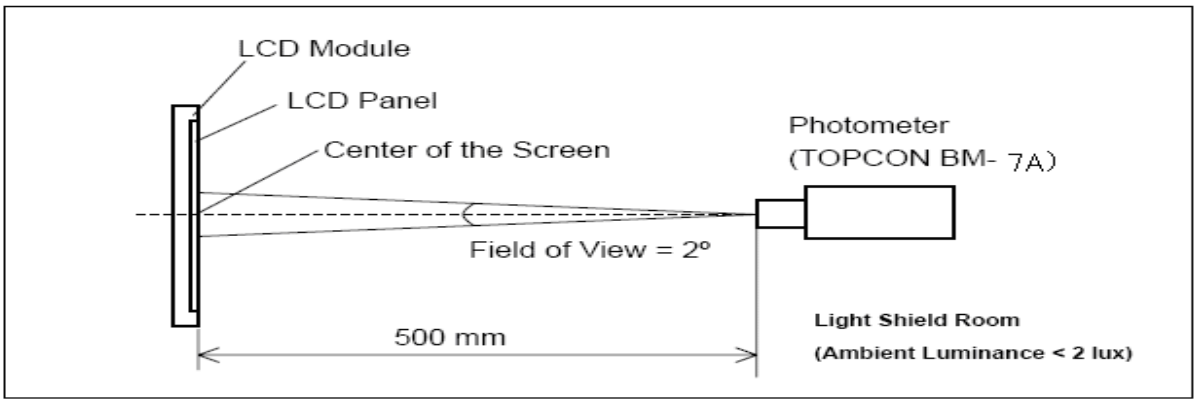


Note(3) Definition of Viewing Angle

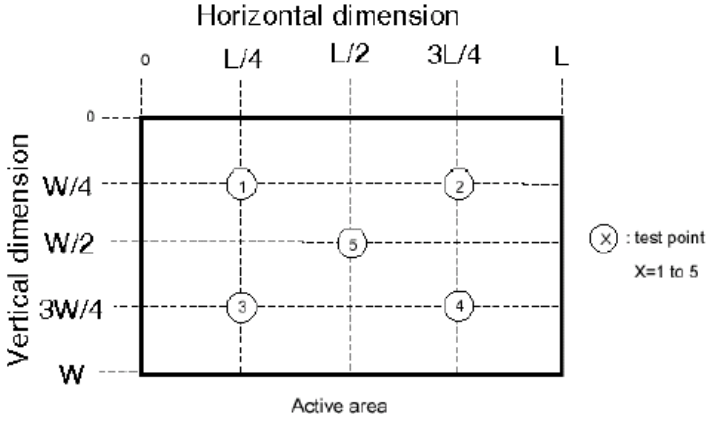


Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (5) Definition of Brightness Uniformity (B-uni):



$$\text{B-uni} = \frac{\text{Minimum luminance of 5 points}}{\text{Maximum luminance of 5points}} \quad \text{(Note 5).}$$

10. INITIAL CODE FOR REFERENCE

```
Void ILI9341_CMO2.8_Initial(void)
{
   // VCI=2.8V
   //************* Reset LCD Driver ****************//
   LCD_nRESET = 1;
   delayms(1); // Delay 1ms
   LCD_nRESET = 0;
   delayms(10); // Delay 10ms // This delay time is necessary
   LCD_nRESET = 1;
   delayms(120); // Delay 120 ms

   //************* Start Initial Sequence **********//

   LCD_ILI9341_CMD(0xB0); //RGB Interface Signal Control
       LCD_ILI9341_Parameter(0xC0);
   LCD_ILI9341_CMD(0xF6, 0x00); //Interface Control
       LCD_ILI9341_Parameter(0x01);
       LCD_ILI9341_Parameter(0x00);
       LCD_ILI9341_Parameter(0x06);
   LCD_ILI9341_CMD(0x13);     //Normal Display Mode ON
   LCD_ILI9341_CMD(0x20);     //Display Inversion OFF
   LCD_ILI9341_CMD(0x3A);     //Pixel Format Setup
       LCD_ILI9341_Parameter(0x66);
   LCD_ILI9341_CMD(0xCF);     // Power control
       LCD_ILI9341_Parameter(0x00);
       LCD_ILI9341_Parameter(0xC1);
       LCD_ILI9341_Parameter(0x30);
   LCD_ILI9341_CMD(0xED);     // Power on sequence control
       LCD_ILI9341_Parameter(0x64);
       LCD_ILI9341_Parameter(0x03);
       LCD_ILI9341_Parameter(0x12);
       LCD_ILI9341_Parameter(0x81);
   LCD_ILI9341_CMD(0xE8);     // Driver timing control
       LCD_ILI9341_Parameter(0x85);
       LCD_ILI9341_Parameter(0x11);
       LCD_ILI9341_Parameter(0x78);
   LCD_ILI9341_CMD(0xCB);     // Power control
       LCD_ILI9341_Parameter(0x39);
       LCD_ILI9341_Parameter(0x2C);
       LCD_ILI9341_Parameter(0x00);
       LCD_ILI9341_Parameter(0x34);
       LCD_ILI9341_Parameter(0x02);
   LCD_ILI9341_CMD(0xF7);     // Pump ratio control
       LCD_ILI9341_Parameter(0x20);
   LCD_ILI9341_CMD(0xEA);     // Driver timing control
       LCD_ILI9341_Parameter(0x00);
       LCD_ILI9341_Parameter(0x00);
   LCD_ILI9341_CMD(0xB1);     // Frame Rate Control
       LCD_ILI9341_Parameter(0x00);
       LCD_ILI9341_Parameter(0x1B);
   LCD_ILI9341_CMD(0xB6);     // Display Function Control
       LCD_ILI9341_Parameter(0x0A);
       LCD_ILI9341_Parameter(0xA2);
   LCD_ILI9341_CMD(0xC0);     // Power Control
       LCD_ILI9341_Parameter(0x23);
```

```
  LCD_ILI9341_CMD(0xC1);     // Power Control
      LCD_ILI9341_Parameter(0x12);
  LCD_ILI9341_CMD(0xC5);     // VCOM Control
      LCD_ILI9341_Parameter(0x21);
      LCD_ILI9341_Parameter(0x2C);
  LCD_ILI9341_CMD(0xC7);     // VCOM Control
      LCD_ILI9341_Parameter(0xB6);
  LCD_ILI9341_CMD(0x36);     // Memory Access Control
      LCD_ILI9341_Parameter(0x08);
  LCD_ILI9341_CMD(0xF2);     // Enable 3G
      LCD_ILI9341_Parameter(0x00);
  LCD_ILI9341_CMD(0x26);     // Gamma Setup
      LCD_ILI9341_Parameter(0x01);
  LCD_ILI9341_CMD(0xE0);     // Positive Gamma Correction
      LCD_ILI9341_Parameter(0x0F);
      LCD_ILI9341_Parameter(0x1B);
      LCD_ILI9341_Parameter(0x1A);
      LCD_ILI9341_Parameter(0x0C);
      LCD_ILI9341_Parameter(0x10);
      LCD_ILI9341_Parameter(0x09);
      LCD_ILI9341_Parameter(0x47);
      LCD_ILI9341_Parameter(0xB8);
      LCD_ILI9341_Parameter(0x35);
      LCD_ILI9341_Parameter(0x0A);
      LCD_ILI9341_Parameter(0x11);
      LCD_ILI9341_Parameter(0x04);
      LCD_ILI9341_Parameter(0x08);
      LCD_ILI9341_Parameter(0x06);
      LCD_ILI9341_Parameter(0x00);
  LCD_ILI9341_CMD(0xE1);     // Negative Gamma Correction
      LCD_ILI9341_Parameter(0x00);
      LCD_ILI9341_Parameter(0x23);
      LCD_ILI9341_Parameter(0x25);
      LCD_ILI9341_Parameter(0x03);
      LCD_ILI9341_Parameter(0x0F);
      LCD_ILI9341_Parameter(0x07);
      LCD_ILI9341_Parameter(0x38);
      LCD_ILI9341_Parameter(0x47);
      LCD_ILI9341_Parameter(0x4A);
      LCD_ILI9341_Parameter(0x04);
      LCD_ILI9341_Parameter(0x0E);
      LCD_ILI9341_Parameter(0x0B);
      LCD_ILI9341_Parameter(0x37);
      LCD_ILI9341_Parameter(0x39);
      LCD_ILI9341_Parameter(0x0F);
  LCD_ILI9341_CMD(0x11);     // Sleep Out
  delayms(120); // Delay 120 ms
  LCD_ILI9341_CMD(0x29);     // Display ON

}
```

11. QUALITY ASSURANCE

Test Condition

13.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 20 ± 5°C

Humidity : 65 ± 5%

13.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

13.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

13.1.4 Test Frequency

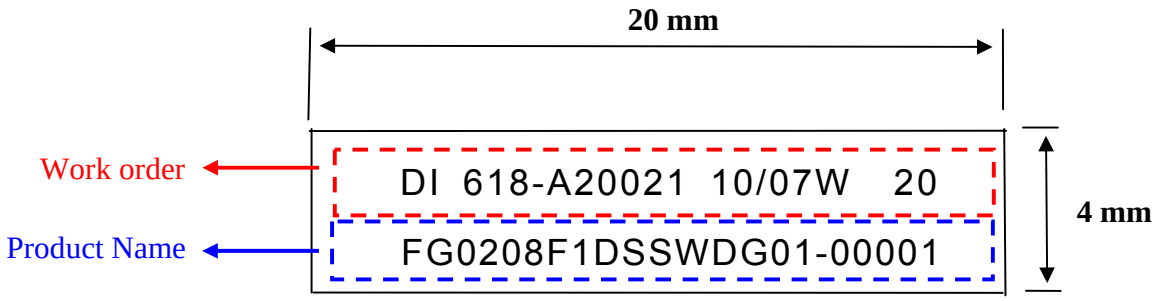
In case of related to deterioration such as shock test. It will be conducted only once.

13.1.5 Test Method

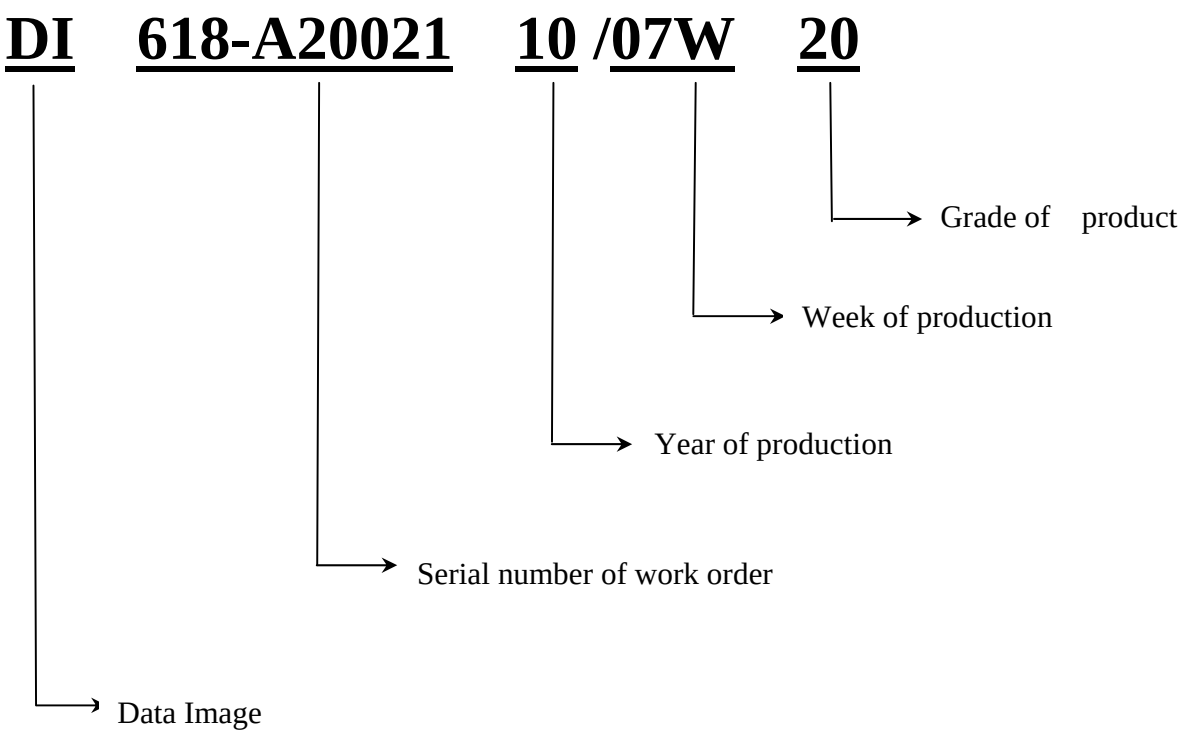
No.	Reliability Test Item & Level	Test Level
1	High Temperature Storage Test	Ta=80°C,240hrs
2	Low Temperature Storage Test	Ta =-30°C,240hrs
3	High Temperature Operation Test	Ta =70°C,240hrs
4	Low Temperature Operation Test	Ta =-20°C,240hrs
5	High Temperature and High Humidity Operation Test	Ta =60°C,90% RH,240hrs
6	Temperature Cycle Test (No operation)	-30°C → +25°C → +80°C,50 Cycles 30 min 5min 50 min
7	Vibration Test (No operation)	Frequency:10 ~ 55 Hz Amplitude:1.0 mm Sweep Time:11min Test Period:6 Cycles for each Direction of X,Y,Z
8	Electrostatic Discharge Test (No operation)	150pF,330Ω Air:± 15KV;Contact: ± 8KV 10 times/point;4 points/panel face

12. LCM PRODUCT LABEL DEFINE

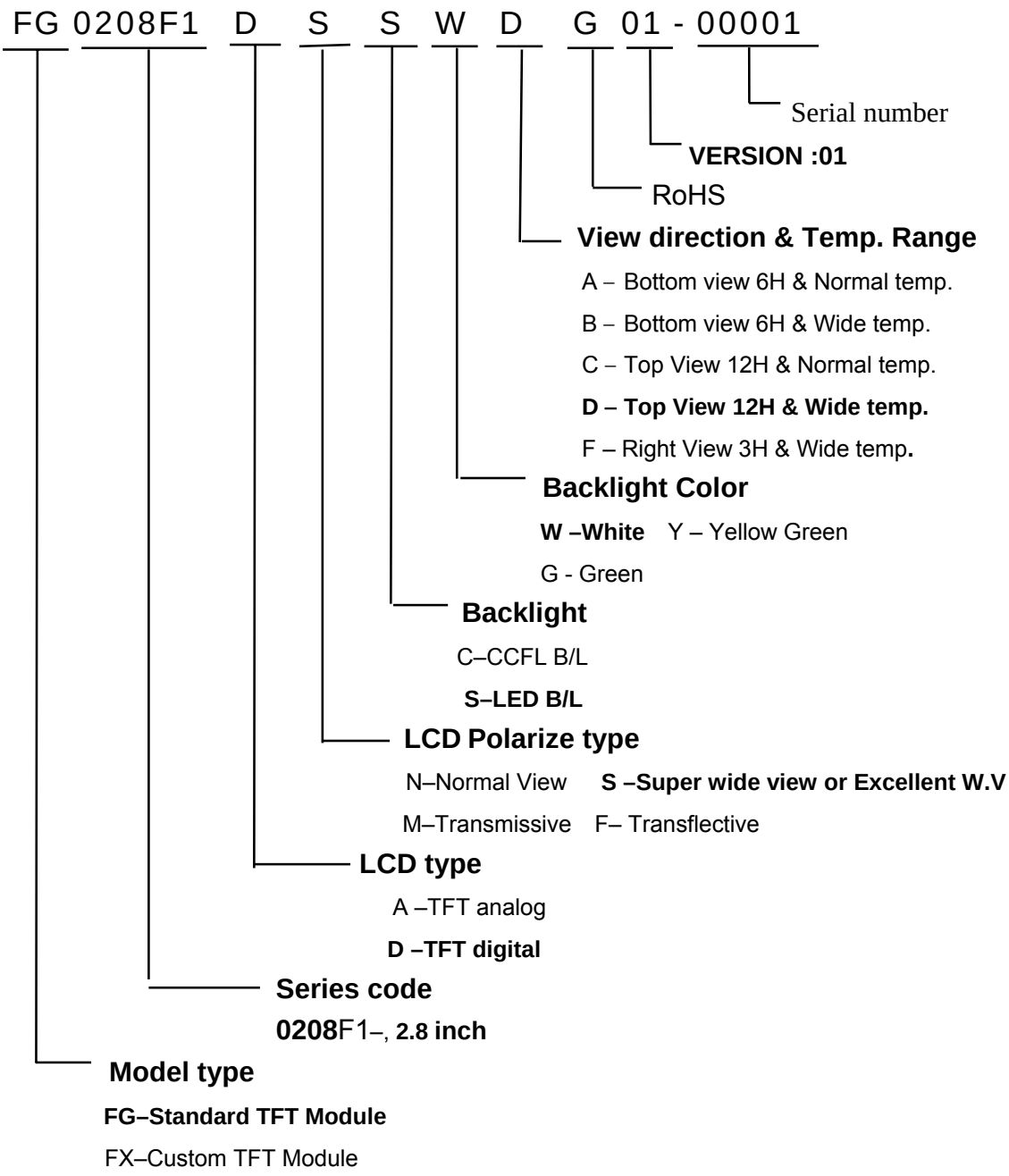
Product Label style:



Work order Define:



Product Name Define:



13. PRECAUTIONS IN USE LCM

1. LIQUID CRYSTAL DISPLAY (LCD)

LCD is made up of glass, organic sealant, organic fluid, and polymer based polarizers. The following precautions should be taken when handing,

(1). Keep the temperature within range of use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel off or bubble.

(2). Do not contact the exposed polarizers with anything harder than an HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin.

(3). Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.

(4). Glass can be easily chipped or cracked from rough handling, especially at corners and edges.

(5). Do not drive LCD with DC voltage.

2. Liquid Crystal Display Modules

2.1 Mechanical Considerations

LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.

(1). Do not tamper in any way with the tabs on the metal frame.

(2). Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.

(3). Do not touch the elastomer connector, especially insert an backlight panel (for example, EL).

(4). When mounting a LCM make sure that the PCB is not under any stress such as bending or twisting . Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.

(5). Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.

2.2. Static Electricity

LCM contains CMOS LSI's and the same precaution for such devices should apply, namely

(1). The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.

(2). The modules should be kept in antistatic bags or other containers resistant to static for storage.

(3). Only properly grounded soldering irons should be used.

(4). If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.

(5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.

(6). Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.

2.3 Soldering

(1). Solder only to the I/O terminals.

(2). Use only soldering irons with proper grounding and no leakage.

(3). Soldering temperature : 280°C ± 10°C

(4). Soldering time: 3 to 4 sec.

(5). Use eutectic solder with resin flux fill.

(6). If flux is used, the LCD surface should be covered to avoid flux spatters. Flux residue should be removed after wards.

2.4 Operation

(1). The viewing angle can be adjusted by varying the LCD driving voltage V0.

(2). Driving voltage should be kept within specified range; excess voltage shortens display life.

(3). Response time increases with decrease in temperature.

(4). Display may turn black or dark blue at temperatures above its operational range; this is (however not pressing on the viewing area) may cause the segments to appear "fractured".

(5). Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured".

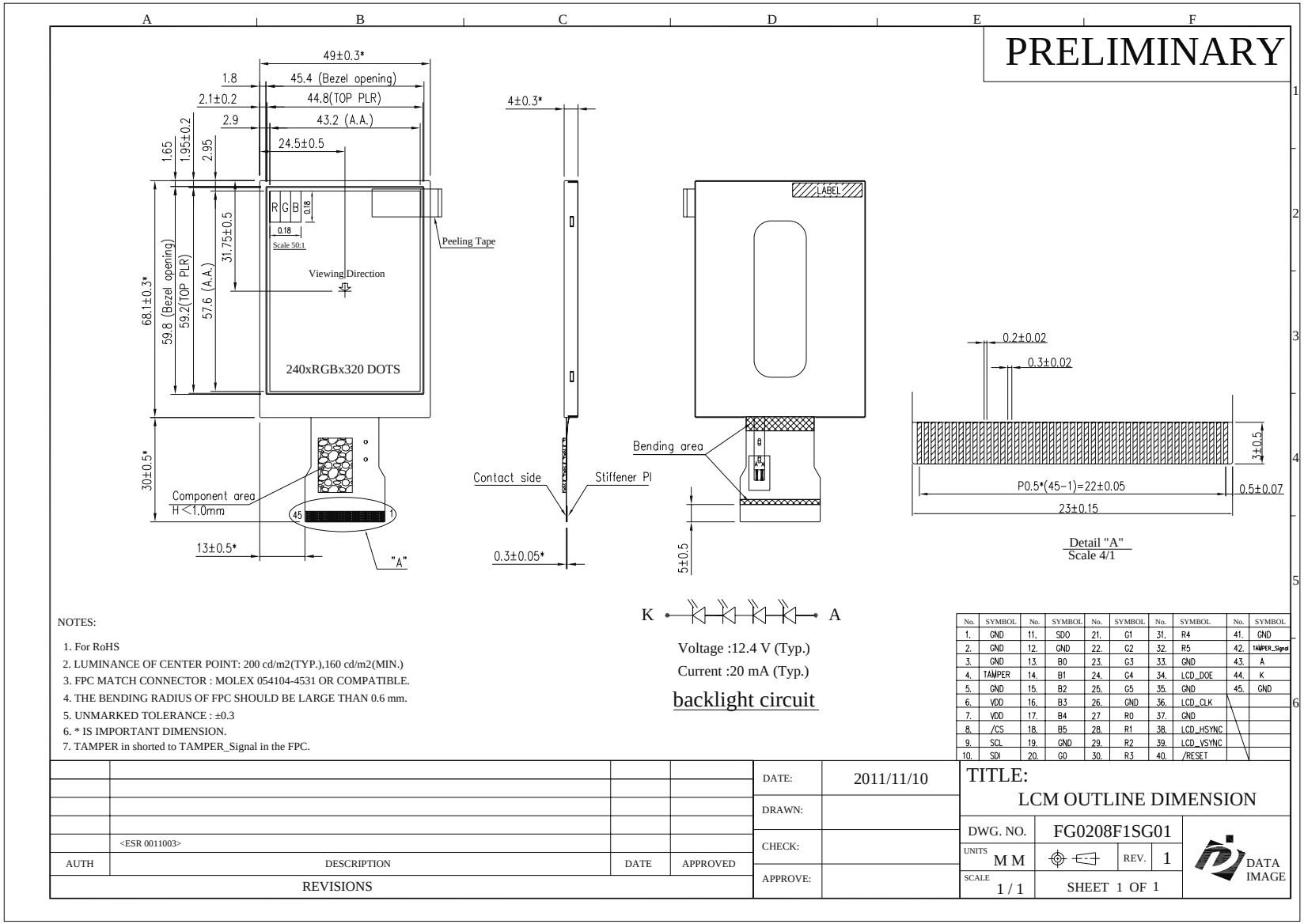
2.5 Storage

If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all the time.

2.6 Limited Warranty

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events.

14. OUTLINE DRAWING



NOTES:

1. For RoHS
2. LUMINANCE OF CENTER POINT: 200 cd/m2(TYP.),160 cd/m2(MIN.)
3. FPC MATCH CONNECTOR : MOLEX 054104-4531 OR COMPATIBLE.
4. THE BENDING RADIUS OF FPC SHOULD BE LARGE THAN 0.6 mm.
5. UNMARKED TOLERANCE : ±0.3
6. * IS IMPORTANT DIMENSION.
7. TAMPER in shorted to TAMPER_Signal in the FPC.

No.	SYMBOL	No.	SYMBOL	No.	SYMBOL	No.	SYMBOL	No.	SYMBOL
1.	GND	11.	SDO	21.	G1	31.	R4	41.	GND
2.	GND	12.	GND	22.	G2	32.	R5	42.	TAMPER_Signal
3.	GND	13.	B0	23.	G3	33.	GND	43.	A
4.	TAMPER	14.	B1	24.	G4	34.	LCD_DOE	44.	K
5.	GND	15.	B2	25.	G5	35.	GND	45.	GND
6.	VDD	16.	B3	26.	GND	36.	LCD_CLK		
7.	VDD	17.	B4	27	R0	37.	GND		
8.	/CS	18.	B5	28.	R1	38.	LCD_HSYNC		
9.	SCL	19.	GND	29.	R2	39.	LCD_VSYNC		
10.	SDI	20.	G0	30.	R3	40.	/RESET		

AUTH	DESCRIPTION	DATE	APPROVED
	<ESR 0011003>		

REVISIONS

DATE:	2011/11/10
DRAWN:	
CHECK:	
APPROVE:	

TITLE: LCM OUTLINE DIMENSION

DWG. NO.	FG0208F1SG01		
UNITS M M		REV.	1
SCALE 1 / 1	SHEET 1 OF 1		

DATA IMAGE

15. PACKAGE INFORMATION

TBD