

ESM-QM57

Intel Core i7/ Celeron COM Express Module

User's Manual



1st Ed – 6 April 2011

FCC Statement



THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRE OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

THESE LIMITS ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST HARMFUL INTERFERENCE WHEN THE EQUIPMENT IS OPERATED IN A COMMERCIAL ENVIRONMENT. THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE HARMFUL INTERFERENCE TO RADIO COMMUNICATIONS.

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5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

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1. Getting Started

1.1 Safety Precautions

Warning!



Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!



Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

1.2 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 x ESM-QM57 Intel Core i7/ Celeron COM Express Module
- 1 x Quick Installation Guide
- 1 x DVD-ROM contains the followings:
 - User's Manual (this manual in PDF file)
 - Chipset and Ethernet driver



If any of the above items is damaged or missing, contact your retailer.

1.3 Document Amendment History

Revision	Date	Comment
1 st	April 2011	Initial Release

1.4 Manual Objectives

This manual describes in detail the Avalue Technology ESM-QM57 Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with ESM-QM57 series or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

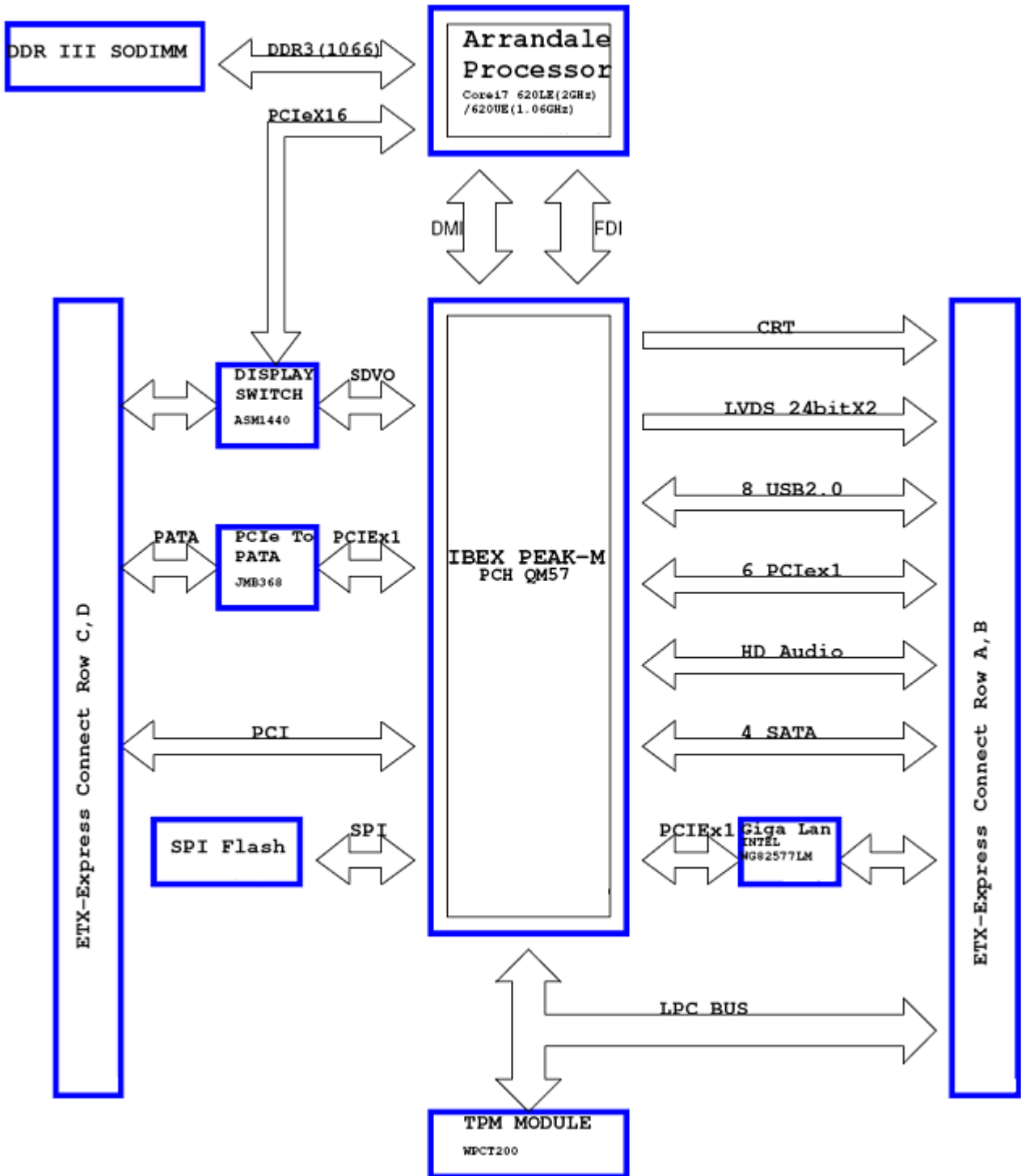
1.5 System Specifications

System	
CPU	Intel Core i7 620LE (2.00GHz) / 620 UE (1.06GHz)
BIOS	AMI 8 MBit Flash BIOS
System Chipset	Intel QM57
I/O Chip	N/A
System Memory	Two 204-pin SODIMM sockets up to 8GB DDR3 800/1066 SDRAM
Expansion	LPC, 4 PCI (PCI Rev. 2.3 compliant), 6 PCIe x1, 1 PCIe x16 (shared with SDVO, HDMI & Displayport)
TPM	Nuvoton WPCT200A
I/O	
MIO	1 x EIDE (Ultra DMA 100), LPC, SMBus/I ² C Bus, 4 x SATA
USB	8 x USB 2.0 ports
DIO	4-bit GPI and 4-bit GPO
Display	
Chipset	Intel QM57
Resolution	CRT mode: 2048 x 1536 @ 60 Hz LCD/Simultaneous mode: 1600x1200 @ 75Hz
Multiple Display	CRT + LVDS, CRT+ SDVO, LVDS + SDVO
LCD Interface	Dual-Channel 18/24-bit LVDS
TV-out	N/A
HDMI DisplayPort	HDMI, DisplayPort shared with PCIe x16
Audio	
Chipset	Intel QM57
Audio Interface	Intel High Definition Audio
Ethernet	
LAN Chip	Intel 82577LM (PHY) Gigabit LAN , supports Wake on LAN
Ethernet Interface	1000Base-Tx Gigabit Ethernet compatible
Mechanical & Environmental	
Power Requirement	+9 ~ +19V
ACPI	Single power ATX Support S0, S3, S4, S5 ACPI 3.0 Compliant
Power Type	AT / ATX

Operating Temp.	0~60°C
Storage Temp.	-40 ~ 75°C
Operating Humidity	0%~90% relative humidity, non-condensing
Size (L x W)	5" x 3.7" (125 mm x 95 mm)
Weight	0.44 lbs (0.2 Kg)

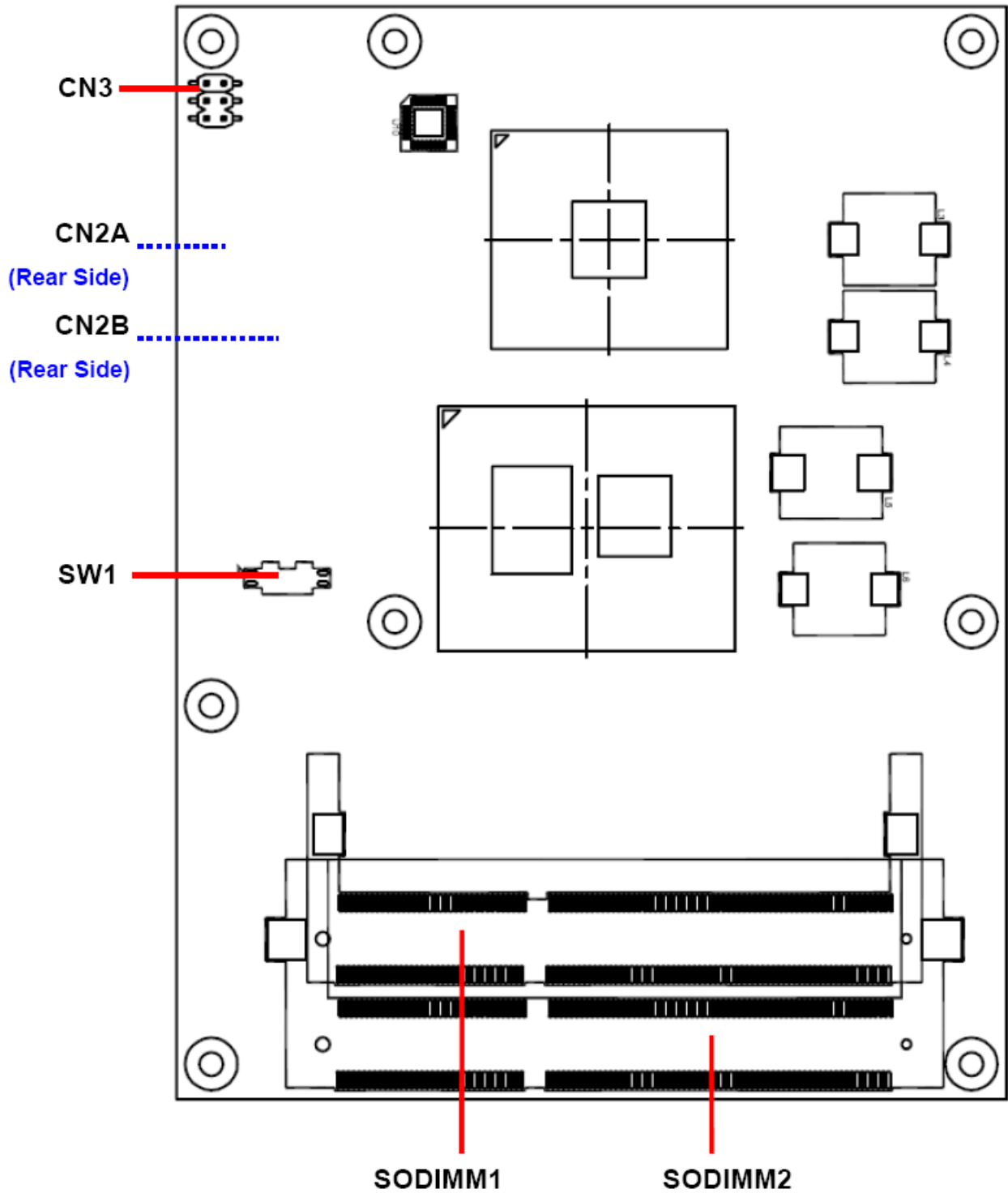
1.6 Architecture Overview – Block Diagram

The following block diagram shows the architecture and main components of ESM-QM57



2. Hardware Configuration

2.1 Product Overview



2.2 Installation Procedure

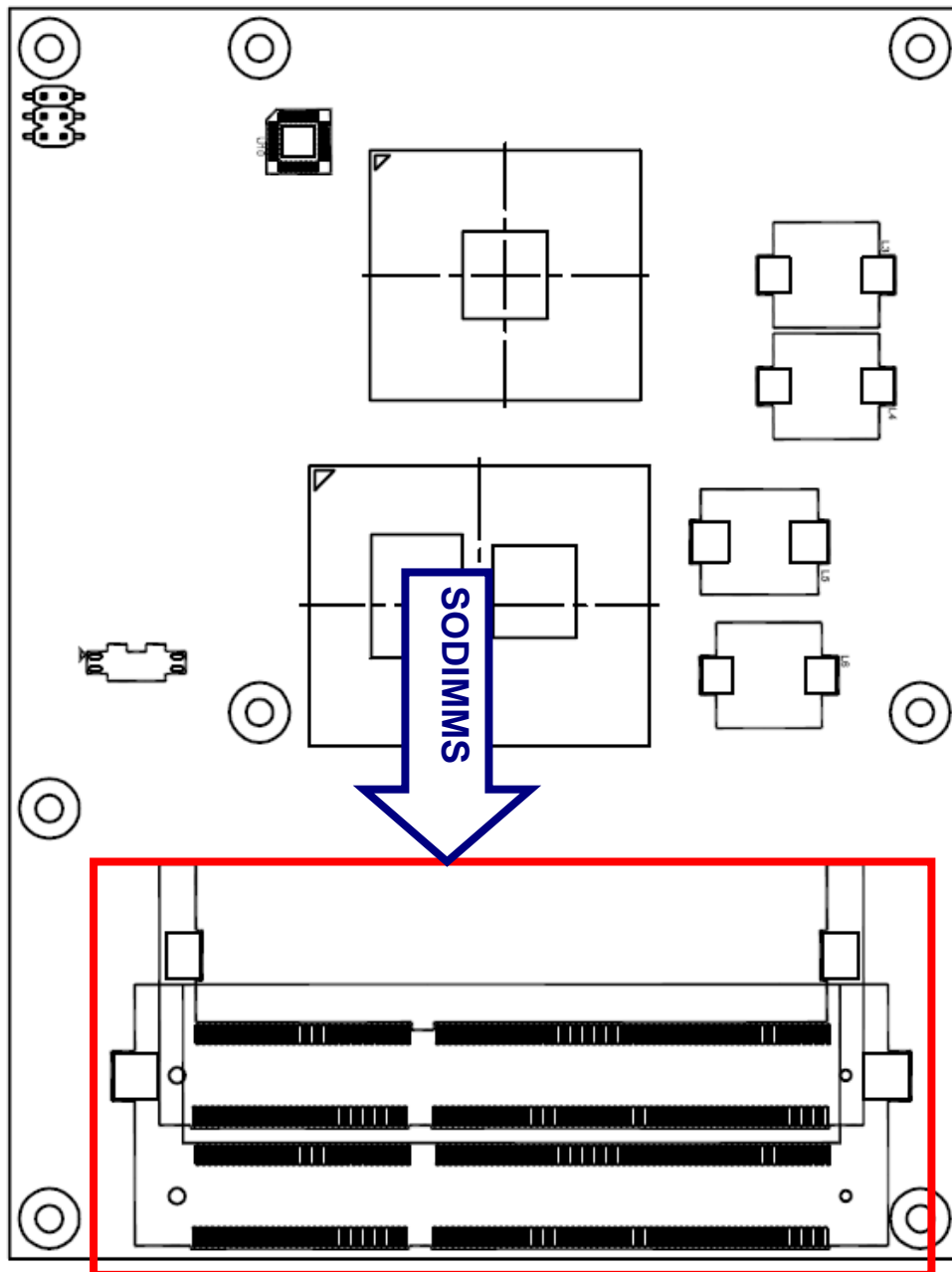
This chapter gives you the instructions on how to setup your system.

1. Turn off the power supply.
2. Insert the SODIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the ATXPWR.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. (more details on page 37)
7. If TFT panel display is to be utilized, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

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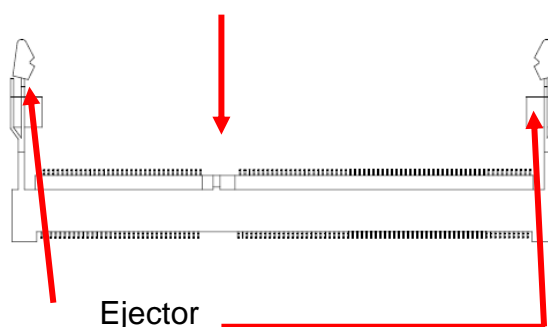
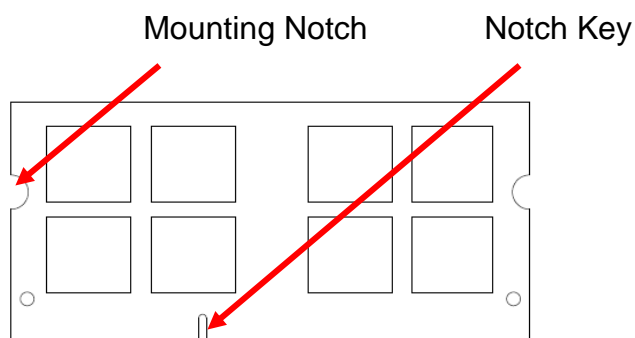
2.2.1 Main Memory

ESM-QM57 provides two 204-pin SODIMM sockets up to 8GB DDR3 800/1066 SDRAM



Make sure to unplug the power supply before adding or removing SODIMMs or other system components. Failure to do so may cause severe damage to both board and components.

- Locate the SODIMM socket on the board.
- Hold two edges of the SODIMM module carefully. Keep away from touching its connectors.
- Align the notch key on the module with the rib on the slot.
- Firmly press the module into the socket which automatically snaps into the mounting notch. Do not force the SODIMM module in with extra force as the SODIMM module only fits in one direction.



204-pin DDR3 SODIMM

- To remove the SODIMM modules, push the two ejector tabs on the slot outward simultaneously, and then pull out the SODIMM module.



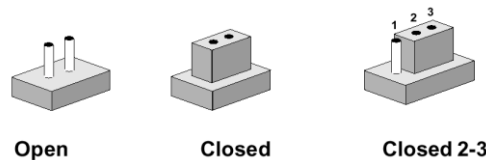
Note:

- (1) Please do not change any DDR3 SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.
- (2) Static electricity can damage the electronic components of the computer or optional boards. Before starting these procedures, ensure that you are discharged of static electricity by touching a grounded metal object briefly.

2.3 Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:



A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

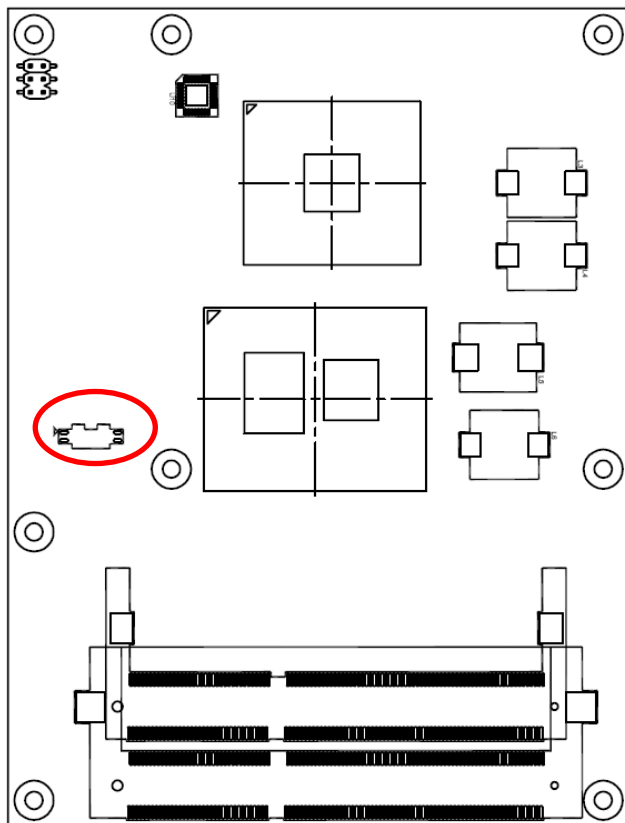
The following tables list the function of each of the board’s jumpers and connectors.

Connectors

Label	Function	Note
CN3	(Reserved for BIOS programming)	3 x 2 header, pitch 2.0mm
CN2A	COM Express connector 1	
CN2B	COM Express connector 2	
SODIMM1	204-pin DDR3 SDRAM DIMM socket	
SODIMM2	204-pin DDR3 SDRAM DIMM socket	
SW1	AT/ATX mode selector	

2.4 Setting Jumpers & Connectors

2.4.1 AT/ATX mode selector (SW1)



*Default

AT/ATX mode



AT mode

OFF	1	↔	ON
	2		

ATX mode*

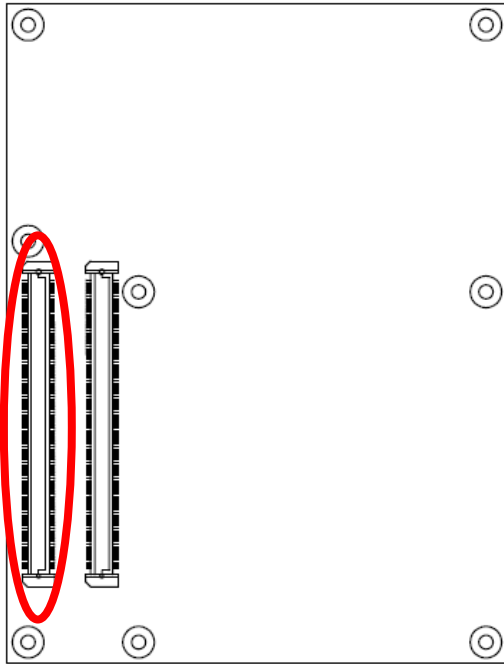
OFF	1	←	ON
	2		

2.4.1.1 Signal Description –AT/ATX mode selection

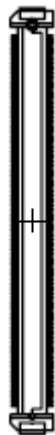
AT/ATX mode	Description
<p>AT mode</p>	This Mode supports AT power supply, no need to press Power button to enable power on/off
<p>ATX mode</p>	This Mode supports ATX power supply. Press the ATX power button to enable power on/off

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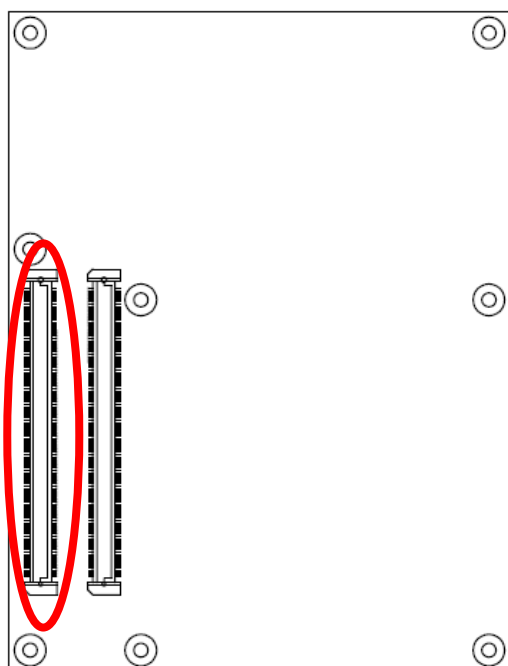
2.4.2 COM Express Connector 1 (CN2A)



(Rear side)



Signal	PIN	PIN	Signal
GND	A1	B1	GND
PCIE_MDI3-	A2	B2	PCIE_ACT#
PCIE_MDI3+	A3	B3	LPC_FRAME#
PCIE_LINK100#	A4	B4	LPC_AD0
PCIE_LINK1000#	A5	B5	LPC_AD1
PCIE_MDI2-	A6	B6	LPC_AD2
PCIE_MDI2+	A7	B7	LPC_AD3
PCIE_LINK#	A8	B8	LPC_DRQ0#
PCIE_MDI1-	A9	B9	LPC_DRQ1#
PCIE_MDI1+	A10	B10	CLK_LPC_33M
GND	A11	B11	GND
PCIE_MDI0-	A12	B12	PWRBTN#
PCIE_MDI0+	A13	B13	SMB_CLK
LAN_1.9V	A14	B14	SMB_DATA
SLP_S3#	A15	B15	LINKALERT#
SATAP0_TXP	A16	B16	SATAP1_TXP
SATAP0_TXN	A17	B17	SATAP1_TXN
SLP_S4#	A18	B18	PM_SUS_SATA#
SATAP0_RXP	A19	B19	SATAP1_RXP
SATAP0_RXN	A20	B20	SATAP1_RXN
GND	A21	B21	GND
SATAP2_TXP	A22	B22	SATAP3_TXP
SATAP2_TXN	A23	B23	SATAP3_TXN
SLP_S5#	A24	B24	POWER_OK
SATAP2_RXP	A25	B25	SATAP3_PXP
SATAP2_RXN	A26	B26	SATAP3_PXN
PM_BATLOW#	A27	B27	WDT
SATA_LED#	A28	B28	HAD_SDIN2
HAD_SYNC	A29	B29	HAD_SDIN1
HAD_RST#	A30	B30	HAD_SDIN0

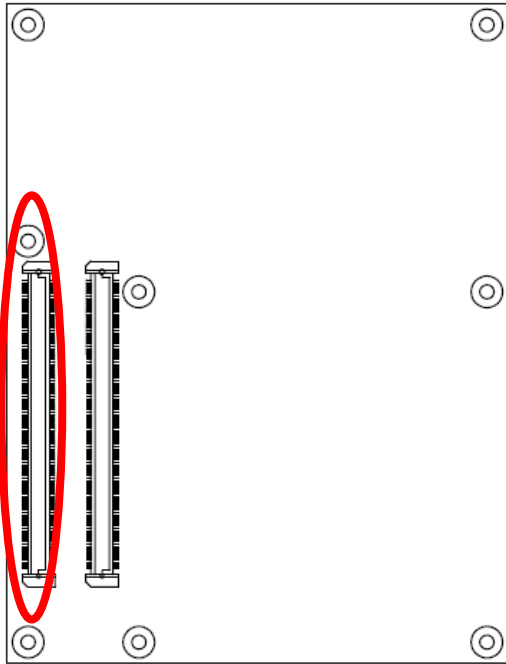


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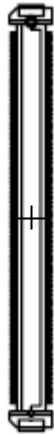


Signal	PIN	PIN	Signal
GND	A31	B31	GND
HAD_BIT_CLK	A32	B32	HAD_SPKR
HAD_SDOOUT	A33	B33	I2C_CLK
BIOS_DISABLE#	A34	B34	I2C_DAT
PM_THRMTRIP#	A35	B35	ETX_THRM#
USB_PN6	A36	B36	USB_PN7
USB_PP6	A37	B37	USB_PP7
USB_OC67#	A38	B38	USB_OC45#
USB_PN4	A39	B39	USB_PN5
USB_PP4	A40	B40	USB_PP5
GND	A41	B41	GND
USB_PN2	A42	B42	USB_PN3
USB_PP2	A43	B43	USB_PP3
USB_OC23#	A44	B44	USB_OC01#
USB_PN0	A45	B45	USB_PN1
USB_PP0	A46	B46	USB_PP1
RTC_VCC	A47	B47	PLTRST#
PLTRST#	A48	B48	EXCD1_CPPE#
EXCD0_CPPE#	A49	B49	PM_SYSRST#
PCI_SERIRQ	A50	B50	BU_PLTRST#
GND	A51	B51	GND
PCIE8_TX+	A52	B52	PCIE8_RX+
PCIE8_TX-	A53	B53	PCIE8_RX-
ETX_GPIO43	A54	B54	ETX_GPIO10
PCIE7_TX+	A55	B55	PCIE7_RX+
PCIE7_TX-	A56	B56	PCIE7_RX-
GND	A57	B57	ETX_GPIO2
PCIE4_TX+	A58	B58	PCIE4_RX+
PCIE4_TX-	A59	B59	PCIE4_RX-
GND	A60	B60	GND

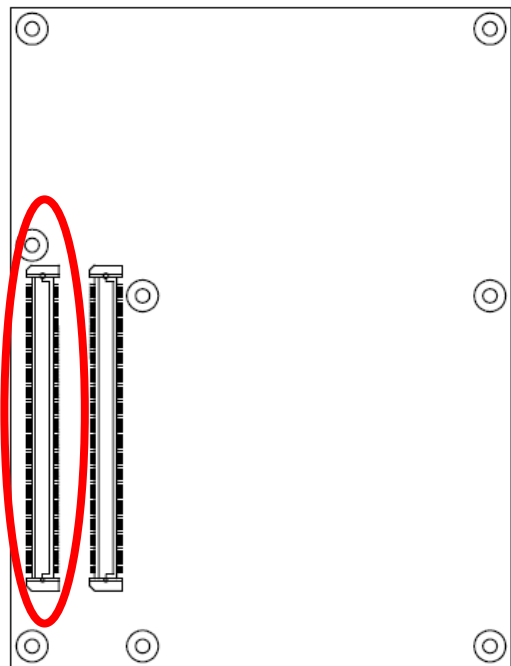
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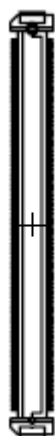
(Rear side)



Signal	PIN	PIN	Signal
PCIE3_TX+	A61	B61	PCIE3_RX+
PCIE3_TX-	A62	B62	PCIE3_RX-
ETX_GPIO45	A63	B63	ETX_GPIO15
PCIE2_TX+	A64	B64	PCIE2_RX+
PCIE2_TX-	A65	B65	PCIE2_RX-
GND	A66	B66	PCIE_WAKE#
ETX_GPIO46	A67	B67	PM_RI#
PCIE1_TX+	A68	B68	PCIE1_RX+
PCIE1_TX-	A69	B69	PCIE1_RX-
GND	A70	B70	GND
LVDSA_DATA0	A71	B71	LVDSB_DATA0
LVDSA_DATA#0	A72	B72	LVDSB_DATA#0
LVDSA_DATA1	A73	B73	LVDSB_DATA1
LVDSA_DATA#1	A74	B74	LVDSB_DATA#1
LVDSA_DATA2	A75	B75	LVDSB_DATA2
LVDSA_DATA#2	A76	B76	LVDSB_DATA#2
LVDS_VDD_EN	A77	B77	LVDSB_DATA3
LVDSA_DATA3	A78	B78	LVDSB_DATA#3
LVDSA_DATA#3	A79	B79	LVDS_BKLT_EN
GND	A80	B80	GND
LVDSA_CLK	A81	B81	LVDSB_CLK
LVDSA_CLK#	A82	B82	LVDSB_CLK#
LVDS_DDC_CLK	A83	B83	LVDS_BKLT_CTRL
LVDS_DDC_DATA	A84	B84	5VSB
ETX_GPIO7	A85	B85	5VSB
KBRST#	A86	B86	5VSB
H_A20GATE	A87	B87	5VSB
CLK_PCIE_ETX+	A88	B88	NC
CLK_PCIE_ETX-	A89	B89	CRT_RED
GND	A90	B90	GND



(Rear side)



Signal	PIN	PIN	Signal
CLK_PEG_A+	A91	B91	CRT_GREEN
CLK_PEG_A-	A92	B92	CRT_BLUE
ETX_GPIO09	A93	B93	CRT_HSYNC
GPIO06	A94	B94	CRT_VSYNC
GPIO07	A95	B95	CRT_DDC_CLK
GND	A96	B96	CRT_DDC_DATA
+12V	A97	B97	NC
+12V	A98	B98	NC
+12V	A99	B99	NC
GND	A100	B100	GND
+12V	A101	B101	+12V
+12V	A102	B102	+12V
+12V	A103	B103	+12V
+12V	A104	B104	+12V
+12V	A105	B105	+12V
+12V	A106	B106	+12V
+12V	A107	B107	+12V
+12V	A108	B108	+12V
+12V	A109	B109	+12V
GND	A110	B110	GND

2.4.2 Signal Description – COM Express Connector 1 (CN2A)

2.4.2.1 Audio Signals

Signal	Signal Description
AC_SYNC	48kHz fixed-rate, sample-synchronization signal to the CODEC(s)
AC_RST#	Reset output to AC97 CODEC, active low.
AC_SDIN[0:2]	Serial TDM data inputs from up to 3 CODECs.
AC_BITCLK	12.228 MHz serial data clock generated by the external CODEC(s)
AC_SDOUT	Serial TDM data output to the CODEC.

2.4.2.2 Gigabit Ethernet Signals

Signal	Signal Description																				
GBE0_MD[0:3] +/-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:																				
	<table border="1"> <thead> <tr> <th></th> <th>1000B-T</th> <th>100B-T</th> <th>10B-T</th> </tr> </thead> <tbody> <tr> <td>MDI[0] +/-</td> <td>B1_DA+/-</td> <td>TX+/-</td> <td>TX+/-</td> </tr> <tr> <td>MDI[1] +/-</td> <td>B1_DB+/-</td> <td>RX+/-</td> <td>RX+/-</td> </tr> <tr> <td>MDI[2] +/-</td> <td>B1_DC+/-</td> <td>X</td> <td>X</td> </tr> <tr> <td>MDI[3] +/-</td> <td>B1_DD+/-</td> <td>X</td> <td>X</td> </tr> </tbody> </table>		1000B-T	100B-T	10B-T	MDI[0] +/-	B1_DA+/-	TX+/-	TX+/-	MDI[1] +/-	B1_DB+/-	RX+/-	RX+/-	MDI[2] +/-	B1_DC+/-	X	X	MDI[3] +/-	B1_DD+/-	X	X
		1000B-T	100B-T	10B-T																	
	MDI[0] +/-	B1_DA+/-	TX+/-	TX+/-																	
	MDI[1] +/-	B1_DB+/-	RX+/-	RX+/-																	
MDI[2] +/-	B1_DC+/-	X	X																		
MDI[3] +/-	B1_DD+/-	X	X																		
GBE0_ACT#	Gigabit Ethernet Controller 0 activity indicator, active low.																				
GBE0_Link#	Gigabit Ethernet Controller 0 link indicator, active low.																				
GBE0_Link100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.																				
GBE0_Lin1000#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.																				

2.4.2.3 GPIO Signals

Signal	Signal Description
GPI[0:3]	General purpose input pins. Pulled high internally on the module.
GPO[0:3]	General purpose output pins. Upon a hardware reset, these outputs will be low.

2.4.2.4 Flat Panel LVDS Signals

Signal	Signal Description
BIASON	Controls panel contrast voltage.
DIGON	Controls panel digital power.
ENBKL#	Controls backlight power enable.
I ² C_DAT, I ² C_CLK	I ² C interface for panel parameter EEPROM. This EEPROM is mounted on the LVDS receiver. The data in the EEPROM allows the EXT module to automatically set the proper timing parameters for a specific LCD panel.

2.4.2.5 LPC Signals

Signal	Signal Description
LPC_FRAME#	LPC frame indicates the start of an LPC cycle
LPC_AD[0:3]	LPC multiplexed address, command and data bus
LPC_DRQ[0:1]#	LPC serial DMA request
LPC_CLK	LPC clock output - 33MHz nominal
LPC_SERIRQ	LPC serial interrupt

2.4.2.6 Miscellaneous Signals

Signal	Signal Description
I ² C_CK	General purpose I ² C port clock output
I ² C_DAT	General purpose I ² C port data I/O line
SPKR	Output for audio enunciator - the "speaker" in PC-AT systems
BIOS_DISABLE#	Module BIOS disable input. Pull low to disable module BIOS. Used to allow off-module BIOS implementations.
KB_RST#	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.
KB_A20GATE	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled low on the module.

2.4.2.7 PCI Express Signals

Signal	Signal Description
PCIE_TX[0:4] +/-	PCI Express Differential Transmit Pair 0-4
PCIE_RX[0:4] +/-	PCI Express Differential Receive Pair 0-4
PCIE0_CK_REF+/-	Reference clock output for PCI Express lanes 0-7 and for PCI Express Graphics lanes 0-15

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2.4.2.8 Power Signals

Signal	Signal Description
VCC_5V_SBY	Standby power input: +5.0V nominal. See Electrical Specifications for allowable input range. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) must be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.
VCC_RTC	Real-time clock circuit-power input. Nominally +3.0V. See Electrical Specifications section for details.

2.4.2.9 Power & System Management Signals

Signal	Signal Description
SUS_S3#	Indicates system is in Suspend to RAM state. Active low output.
SUS_S4#	Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.
BATLOW#	Indicates that external battery is low
PWRBTN#	Power button to bring system out of S5 (soft off), active on rising edge.
SMB_CK	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.
SMB_DTA	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.
SMB_ALERT#	System Management Bus Alert - input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.
SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices
PWR_OK	Power OK from main power supply
THRMTRIP#	Active low output indicating that the CPU has entered thermal shutdown.
THRM#	Input from off-module temp sensor indicating and over-temp situation.
SYS_RESET#	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release.
RSMRST#	Resume reset input, active low. Resets power plane logic. May be left open on carrier board if not used.
WAKE0#	PCI Express wake up signal
WAKE1#	General purpose wake up signal

2.4.2.10 SATA Signals

Signal	Signal Description
SATA[0:3]_TX +/-	Serial ATA Channel 0-3 transmit differential pair.
SATA[0:3]_RX +/-	Serial ATA Channel 0-3 receive differential pair.
ATA_ACT#	ATA (parallel and serial) activity indicator, active low.

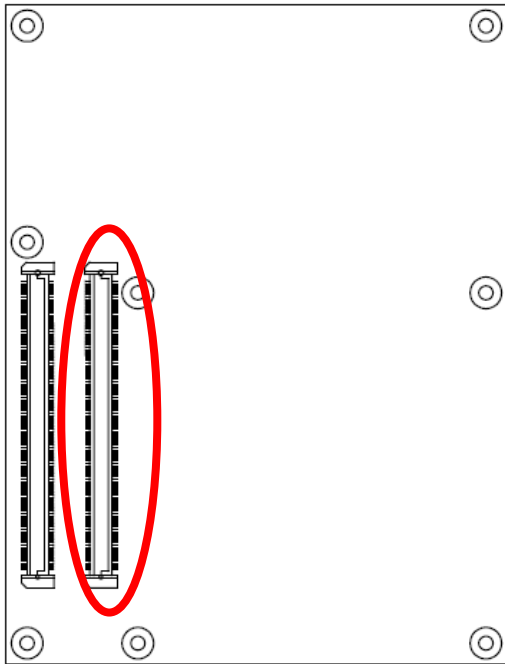
2.4.2.11 VGA Signals

Signal	Signal Description
VGA_RED	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.
VGA_GRN	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.
VGA_BLU	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.
VGA_HSYNC	Horizontal sync output to VGA monitor
VGA_VSYNC	Vertical sync output to VGA monitor
VGA_I ² C_CLK	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)
VGA_I ² C_DAT	DDC data line.

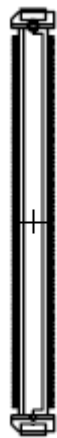
2.4.2.12 USB Signals

Signal	Signal Description
USB[0:7] +/-	USB differential pairs, channels 0 through 7
USB_0_1_OC#	USB over-current sense, USB channels 0 and 1
USB_2_3_OC#	USB over-current sense, USB channels 2 and 3
USB_4_5_OC#	USB over-current sense, USB channels 4 and 5
USB_6_7_OC#	USB over-current sense, USB channels 6 and 7

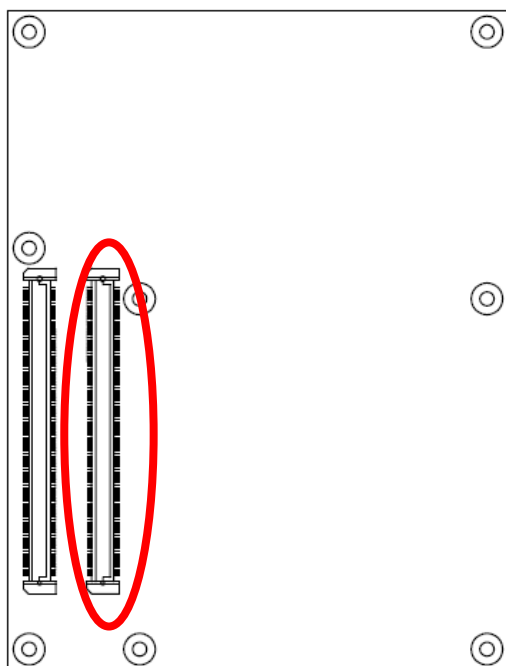
2.4.3 COM Express Connector 2 (CN2B)



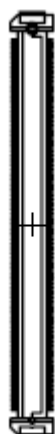
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Signal	PIN	PIN	Signal
GND	C1	D1	GND
IDE_PDD7	C2	D2	IDE_PDD5
IDE_PDD6	C3	D3	IDE_PDD10
IDE_PDD3	C4	D4	IDE_PDD11
IDE_PDD15	C5	D5	IDE_PDD12
IDE_PDD8	C6	D6	IDE_PDD4
IDE_PDD9	C7	D7	IDE_PDD0
IDE_PDD2	C8	D8	IDE_PDDREQ
IDE_PDD13	C9	D9	IDE_PDIOW#
IDE_PDD1	C10	D10	IDE_PDDACK#
GND	C11	D11	GND
IDE_PDD14	C12	D12	IDE_IRQ
IDE_PDIORDY	C13	D13	IDE_PDA0
IDE_PDIOR#	C14	D14	IDE_PDA1
PCI_PME#	C15	D15	IDE_PDA2
PCI_GNT#2	C16	D16	IDE_PDICS1#
PCI_REQ#2	C17	D17	IDE_PDICS3#
PCI_GNT#1	C18	D18	BUF_PLTRST#
PCI_REQ#1	C19	D19	PCI_GNT#3
PCI_GNT#0	C20	D20	PCI_REQ#3
GND	C21	D21	GND
PCI_REQ#0	C22	D22	PCI_AD1
PCIRST#	C23	D23	PCI_AD3
PCI_AD0	C24	D24	PCI_AD5
PCI_AD2	C25	D25	PCI_AD7
PCI_AD4	C26	D26	PCI_CBE#0
PCI_AD6	C27	D27	PCI_AD9
PCI_AD8	C28	D28	PCI_AD11
PCI_AD10	C29	D29	PCI_AD13
PCI_AD12	C30	D30	PCI_AD15

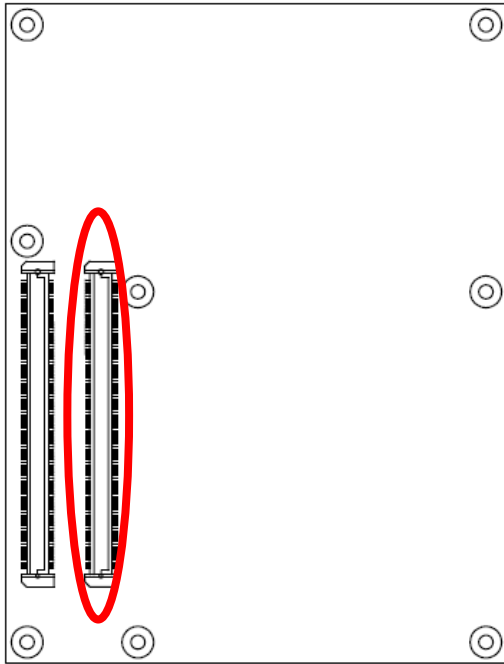


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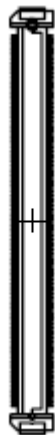


Signal	PIN	PIN	Signal
GND	C31	D31	GND
PCI_AD14	C32	D32	PCI_PAR
PCI_CBE#1	C33	D33	PCI_SERR#
PCI_PERR#	C34	D34	PCI_STOP#
PCI_LOCK#	C35	D35	PCI_TRDY#
PCI_DEVSEL#	C36	D36	PCI_FRAME#
PCI_IRDY#	C37	D37	PCI_AD16
PCU_CBE#2	C38	D38	PCI_AD18
PCI_AD17	C39	D39	PCI_AD20
PCI_AD19	C40	D40	PCI_AD22
GND	C41	D41	GND
PCI_AD21	C42	D42	PCI_AD24
PCI_AD23	C43	D43	PCI_AD26
PCU_CBE#3	C44	D44	PCI_AD28
PCI_AD25	C45	D45	PCI_AD30
PCI_AD27	C46	D46	INT_PIRQC#
PCI_AD29	C47	D47	INT_PIRQD#
PCI_AD31	C48	D48	PM_CLKRUN#
INT_PIRQA#	C49	D49	NC
INT_PIRQB#	C50	D50	CLK_PCI
GND	C51	D51	GND
PEG_RX0	C52	D52	PEG_TX0
PEG_RX#0	C53	D53	PEG_TX#0
NC	C54	D54	PEG_LAN_RV#
PEG_RX1	C55	D55	PEG_TX1
PEG_RX#1	C56	D56	PEG_TX#1
NC	C57	D57	NC
PEG_RX2	C58	D58	PEG_TX2
PEG_RX#2	C59	D59	PEG_TX#2
GND	C60	D60	GND

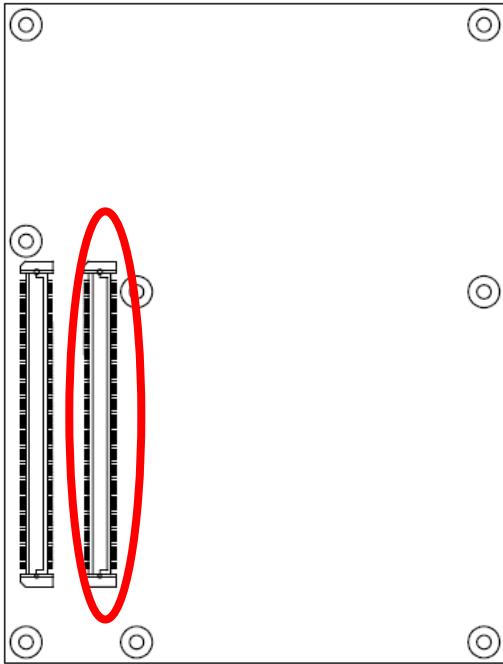
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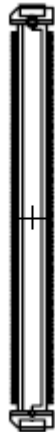
(Rear side)



Signal	PIN	PIN	Signal
PEG_RX3	C61	D61	PEG_TX3
PEG_RX#3	C62	D62	PEG_TX#3
DDPB_AUX+	C63	D63	DDPC_AUX+
DDPB_AUX-	C64	D64	DDPC_AUX-
PEG_RX4	C65	D65	PEG_TX4
PEG_RX#4	C66	D66	PEG_TX#4
HDMIC_CTRL_CLK	C67	D67	GND
PEG_RX5	C68	D68	PEG_TX5
PEG_RX#5	C69	D69	PEG_TX#5
GND	C70	D70	GND
PEG_RX6	C71	D71	PEG_TX6
PEG_RX#6	C72	D72	PEG_TX#6
SDVO/ HDMIB_CTRL_DATA	C73	D73	SDVO/ HDMIB_CTRL_CLK
PEG_RX7	C74	D74	PEG_TX7
PEG_RX#7	C75	D75	PEG_TX#7
GND	C76	D76	GND
HDMIC_CTRL_DATA	C77	D77	PDIAG_S
PEG_RX8	C78	D78	PEG_TX8
PEG_RX#8	C79	D79	PEG_TX#8
GND	C80	D80	GND
PEG_RX9	C81	D81	PEG_TX9
PEG_RX#9	C82	D82	PEG_TX#9
HDMIB_HPD	C83	D83	NC
GND	C84	D84	GND
PEG_RX10	C85	D85	PEG_TX10
PEG_RX#10	C86	D86	PEG_TX#10
GND	C87	D87	GND
PEG_RX11	C88	D88	PEG_TX11
PEG_RX#11	C89	D89	PEG_TX#11
GND	C90	D90	GND



(Rear side)



Signal	PIN	PIN	Signal
PEG_RX12	C91	D91	PEG_TX12
PEG_RX#12	C92	D92	PEG_TX#12
GND	C93	D93	GND
PEG_RX13	C94	D94	PEG_TX13
PEG_RX#13	C95	D95	PEG_TX#13
GND	C96	D96	GND
HDMIC_HPD	C97	D97	NC
PEG_RX14	C98	D98	PEG_TX14
PEG_RX#14	C99	D99	PEG_TX#14
GND	C100	D100	GND
PEG_RX15	C101	D101	PEG_TX15
PEG_RX#15	C102	D102	PEG_TX#15
GND	C103	D103	GND
+12V	C104	D104	+12V
+12V	C105	D105	+12V
+12V	C106	D106	+12V
+12V	C107	D107	+12V
+12V	C108	D108	+12V
+12V	C109	D109	+12V
GND	C110	D110	GND

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2.4.3 Signal Description – COM Express Connector 2 (CN2B)

2.4.3.1 IDE Signals

Signal	Signal Description
IDE_D[0:15]	Bidirectional data to / from IDE device.
IDE_A[0:2]	Address lines to IDE device.
IDE_REQ#	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.
IDE_IOW#	I/O writes line to IDE device. Data latched on trailing (rising) edge.
IDE_ACK#	IDE Device DMA Acknowledge.
IDE_IRQ	Interrupt request from IDE device.
IDE_IORDY	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.
IDE_IOR#	I/O read line to IDE device.
IDE_CS1#	IDE Device Chip Select for 1F0h to 1FFh range.
IDE_CS3#	IDE Device Chip Select for 3F0h to 3FFh range.
IDE_RESET#	Reset output to IDE device, active low.

2.4.3.2 HDMI Signals

Signal	Signal Description
SDVO/HDMIB_CTRL_DATA	SDVO or HDMI portB Control data
SDVO/HDMIB_CTRL_CLK	SDVO or HDMI portB Control clock
HDMIB_HPD	Reserved for HDMI portB hot plug detection (add a resistor on R544 to activate)
HDMIC_CTRL_DATA	Reserved for HDMI portC Control data (add a resistor on R180 to activate)
HDMIC_CTRL_CLK	Reserved for HDMI portC Control clock (add a resistor on R188 to activate)
HDMIC_HPD	Reserved for HDMI portC hot plug detection (add a resistor on R545 to activate)

2.4.3.3 PCI Signals

Signal	Signal Description
PCI_AD[0:31]	PCI bus multiplexed address and data lines
PCI_PME#	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.
PCI_GNT[0:3]#	PCI bus master grant output lines, active low.
PCI_REQ[0:3]#	PCI bus master request input lines, active low.
PCI_RESET#	PCI Reset output, active low.
PCI_CBE[0:3]	PCI bus byte enable lines, active low
PCI_PERR#	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.
PCI_LOCK#	PCI Lock control line, active low.
PCI_DEVSEL#	PCI bus Device Select, active low.
PCI_IRD Y#	PCI bus Initiator Ready control line, active low.
PCI_IRQ[A:D]	PCI interrupt request lines.
PCI_PAR	PCI bus parity
PCI_SERR#	System Error: SERR# can be pulsed active by any PCI device that detects a system error condition.
PCI_STOP#	PCI bus STOP control line, active low, driven by cycle initiator.
PCI_TRDY#	PCI bus Target Ready control line, active low.
PCI_FRAME#	PCI bus Frame control line, active low.
PCI_CLKRUN#	Bidirectional pin used to support PCI clock run protocol for mobile systems.
PCI_CLK	PCI 33MHz clock output.

2.4.3.4 PCI Express Graphics Signals

Signal	Signal Description
PEG_RX[0:15] +/-	PCI Express Graphics receive differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section).
PEG_TX[0:15] +/-	PCI Express Graphics transmit differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section).
TYPE[0:2]	
PEG_LANE_RV#	PCI Express Graphics lane reversal input strap. Pull low to reverse lane order. Pulled high on module.
SDVO_DATA	SDVO I ² C data line - to set up SDVO peripherals.
SDVO_CLK	SDVO I ² C clock line - to set up SDVO peripherals.

3. BIOS Setup

3.1 Introduction

The BIOS setup program allows users to modify the basic system configuration. In this following chapter will describe how to access the BIOS setup program and the configuration options that may be changed.

3.2 Starting Setup

The AMIBIOS™ is immediately activated when you first turn on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing immediately after switching the system on, or

By pressing the key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

Press F1 to Continue, DEL to enter SETUP

3.3 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Button	Description
↑↓	Select item
←	Select screen
+/-	Change Option /Field
Enter	Go to Sub Screen
PgUp key	Previous page
PgDn key	Next page
Home	Go to top of screen
End	Go to bottom of Screen
F2 , F3 key	Change colors
F7 key	Discard changes
F8 key	Load Failsafe Defaults
F9 key	Load Optimal Defaults
F10 key	Save and Exit
Esc key	Exit current page and return to Main Menu

- **Navigating Through The Menu Bar**

Use the left and right arrow keys to choose the menu you want to be in.



Note: Some of the navigation keys differ from one screen to another.

- **To Display a Sub Menu**

Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A “>” pointer marks all sub menus.

3.4 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

3.5 In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AMIBIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override function.

3.6 BIOS setup

Once you enter the AMIBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

Note that a brief description of each highlighted selection appears at the bottom of the screen.

3.6.1 Main Menu

This section allows you to record some basic hardware configurations on your computer and set the system clock.



3.6.1.1 System Language

This option allows choosing the system default language.

3.6.1.2 System Date

Use the system time option to set the system time. Manually enter hours, minutes and seconds.

3.6.1.3 System Time

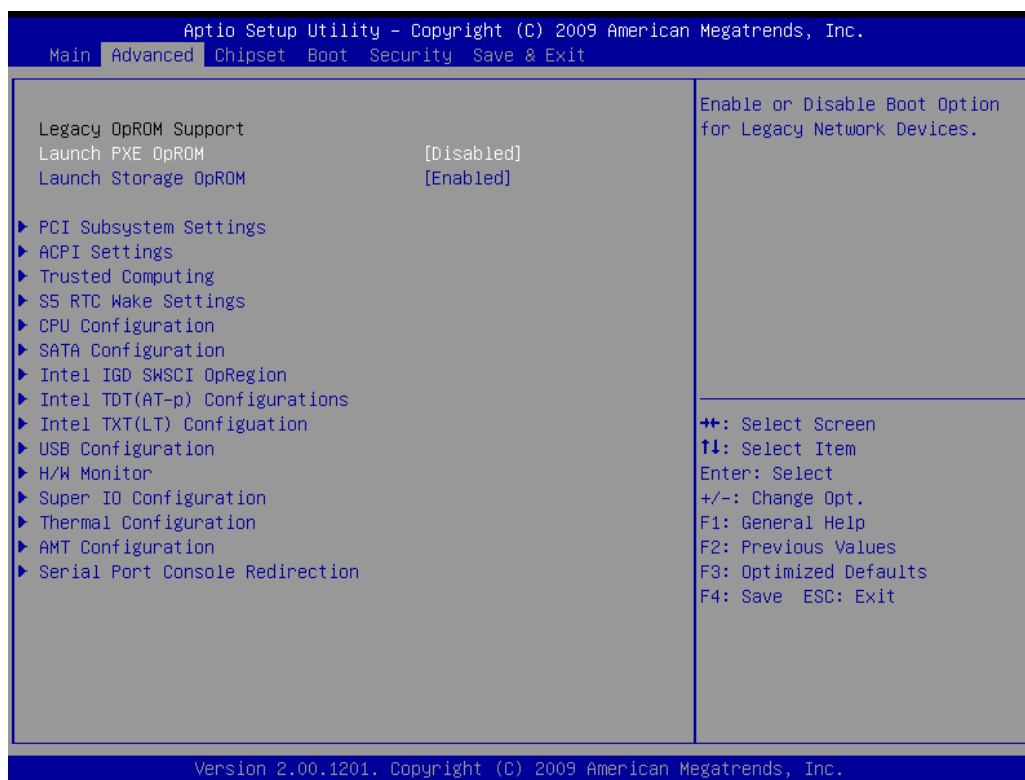
Use the system Date option to set the system date. Manually enter the day, month and year.



Note: The BIOS setup screens shown in this chapter are for reference purposes only, and may not exactly match what you see on your screen. Visit the Avalue website (www.avalue.com.tw) to download the latest product and BIOS information.

3.6.2 Advanced Menu

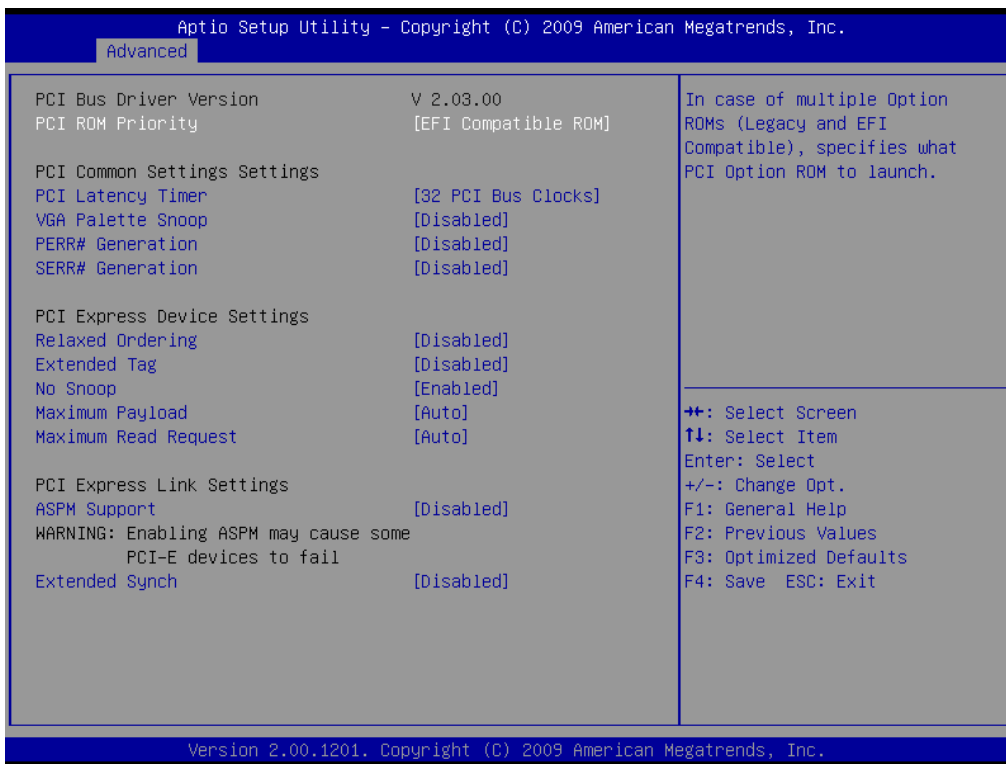
This section allows you to configure your CPU and other system devices for basic operation through the following sub-menus.



Item	Options	Description
Launch PXE OpROM	Disabled, Enabled	Enable or disable Boot Option for Legacy Network Devices
Launch Storage OpROM	Disabled, Enabled	Enable or disable Boot Option for Legacy Mass storage devices With Option ROM.

3.6.2.1 PCI Subsystem Settings

Use this item to configure PCI Subsystem



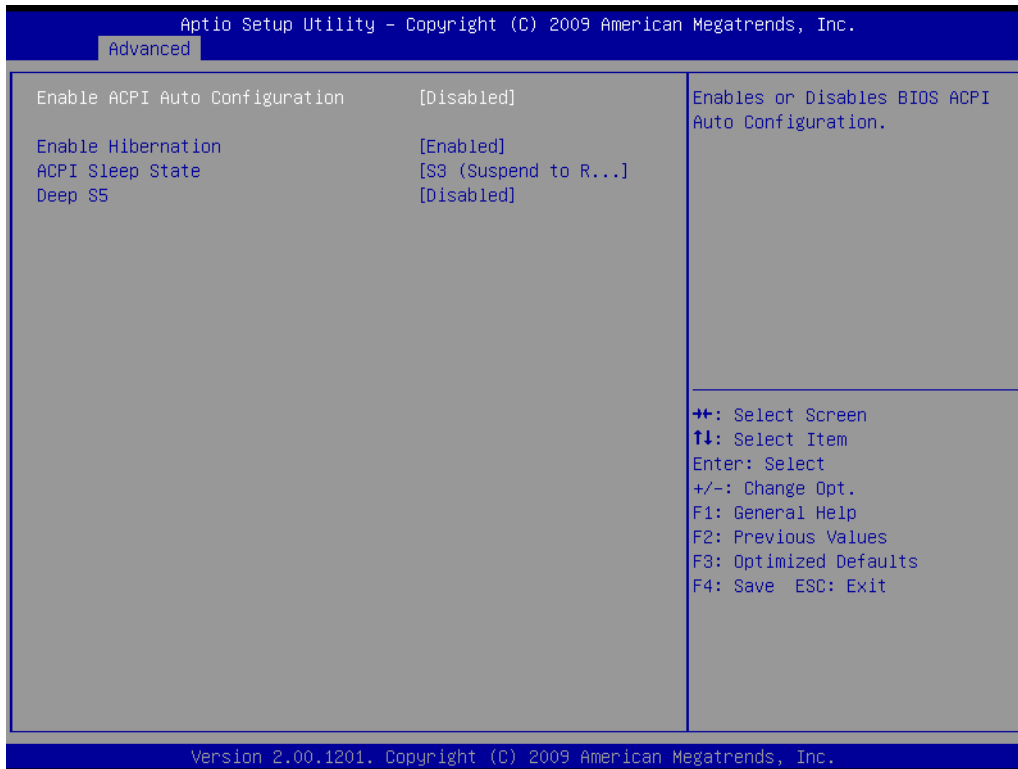
Item	Options	Description
PCI ROM Priority	Legacy ROM EFI Compatible ROM [Default]	Specifies what PCI Option ROM to launch in case of multiple Option ROMs
PCI Latency Timer	64/96/128/160/192/224/248	Value to be programmed into PCI Latency Timer Register.
VGA Palette Snoop	Enabled Disabled [Default]	Enable or disable VGA Palette Snooping
PERR# Generation	Enabled Disabled [Default]	Enable or disable PCI Device to Generate PERR#
SERR# Generation	Enabled Disabled [Default]	Enable or disable PCI Device to Generate SERR#
Relaxed Ordering	Enabled Disabled [Default]	Enable or disable PCI Express Device Relaxed ordering
Extended Tag	Enabled Disabled [Default]	If enabled, would allow Device to use 8-bit Tag field as a requester
No Snoop	Enabled [Default] Disabled	Enable or disable PCI Express Device No Snoop option.

Maximum Payload	Auto[Default] 128/256/512/1024/2048/4096 Bytes	Set Maximum Payload for PCI Express Device or allow System BIOS to select the value
Maximum Read Request	Auto[Default] 128/256/512/1024/2048/4096 Bytes	Set Maximum Read Request for PCI Express Device or allow System BIOS to select the value
ASPM Support	Disabled[Default] Auto Force L0	Set ASPM level
Extended Synch	Enabled Disabled[Default]	If Enabled, allows generation of Extended Synchronization patterns

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3.6.2.2 ACPI Settings

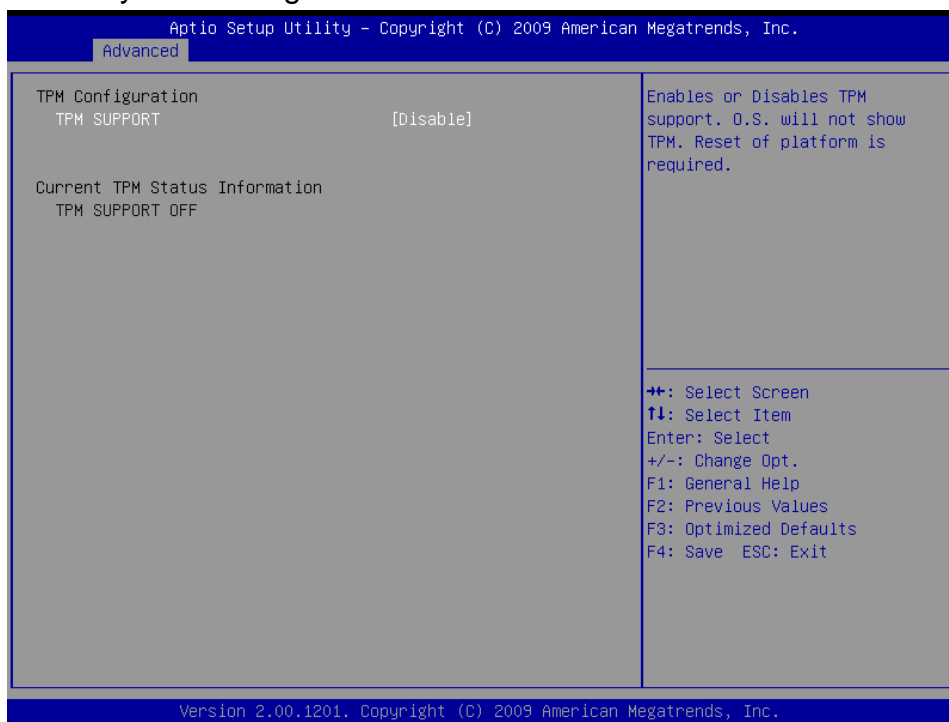
You can use this item to configure ACPI



Item	Options	Description
Enable ACPI Auto Configuration	Disabled [Default] Enabled	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled, Enabled [Default]	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disable, S1 (CUP Stop Clock), S3 (Suspend to RAM) [Default]	Select the highest ACPI sleep state the system will enter, when the SUSPEND button is pressed.
Deep S5	Disabled [Default] Enabled	Enables or Disables deep S5 function.

3.6.2.3 Trusted computing

This section allows you to configure Trusted Platform Module



Item	Options	Description
TPM Support	Disabled[Default] Enabled	Enables or Disables TPM support

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3.6.2.4 S5 RTC Wake Settings

Use the S5 RTC wake setting to set system wake in fixed time.



Item	Options	Description
Wake system with fixed time	Disabled[Default] Enabled	Enables or Disables wake on alarm event. When enabled, system will wake on the specified hr:min::sec.

3.6.2.5 CPU Configuration

Use the CPU configuration menu to view detailed CPU specification and configure the CPU.



Item	Options	Description
Hyper-threading	Disabled, Enabled[Default]	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.
Active Processor Cores	All[Default] 1, 2	Number of cores to enable in each processor package.
Limit CPUID Maximum	Disabled[Default] Enabled	Disabled for Windows XP.
Hardware Prefetcher	Disabled, Enabled[Default]	To turn on/ off the MLC streamer prefetcher.
Adjacent Cache Line Prefetch	Disabled, Enabled[Default]	To turn on/ off prefetching of adjacent cache lines.
Intel Virtualization Technology	Disabled, Enabled[Default]	When enables, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

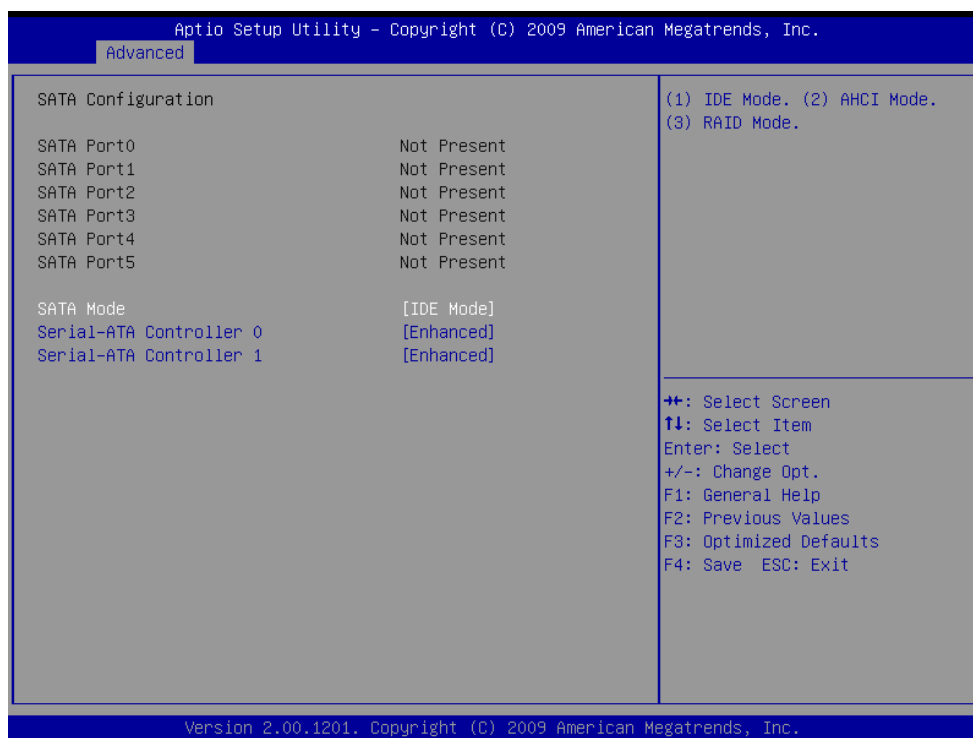
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Power Technology	Disabled, Energy Efficient [Default] Custom	Enable the power management features.
TDC Limit	0	Turbo-XE Mode Processor TDC Limit in 1/8 A granularity. 0 means using the factory-configured value.
TDP Limit	0	Turbo-XE Mode Processor TDP Limit in 1/8 W granularity. 0 means using the factory-configured value.

3.6.2.6 SATA Configuration

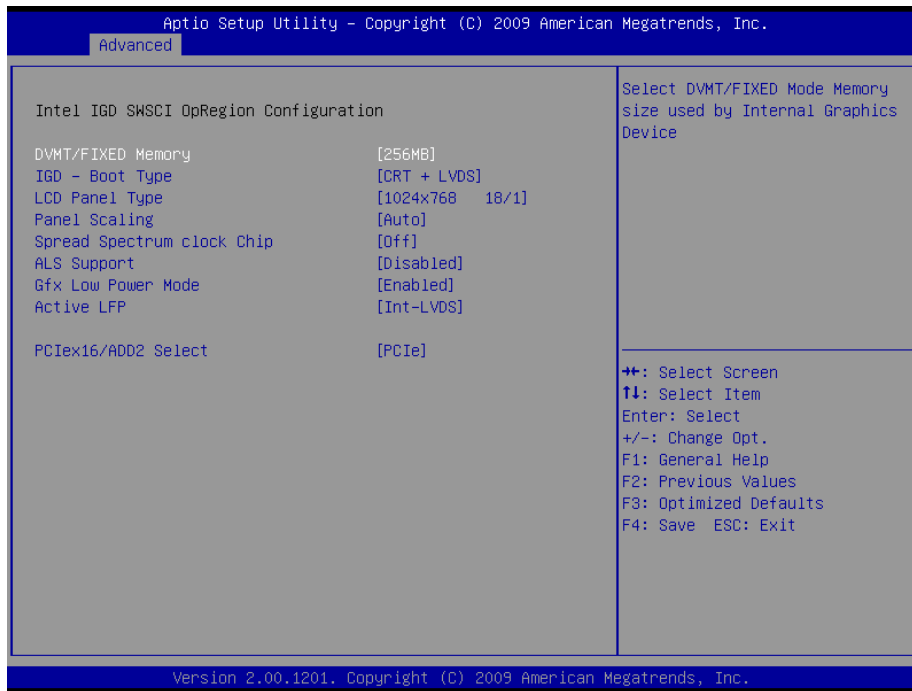
It allows you to select the operation mode for SATA controller.

The choices:



Item	Option	Description
SATA mode	Disabled, IDE mode, AHCI mode, RAID mode	It allows you to select the operation mode for SATA controller.
Serial-ATA Controller 0	Disabled, Enhanced [Default] Compatible	Enabled/ Disabled Serial ATA Controller 0.
Serial-ATA Controller 1	Disabled, Enhanced [Default]	Enabled/ Disabled Serial ATA Controller 0.

3.6.2.7 Intel IGD SWSCI OpRegion configuration



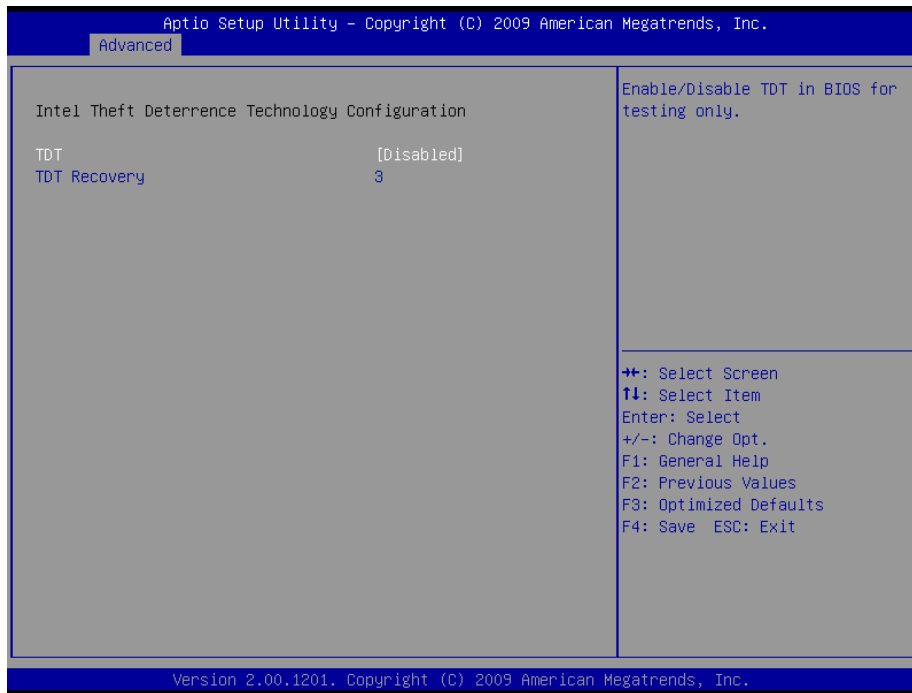
Item	Option	Description
DVMT/ Fixed Memory	256MB [Default] 128MB, Maximum	This feature allows you to select the memory size of DVMT/BOTH operating mode.
IGD – Boot Type	CRT+LVDS [Default] DVI(HDMI), CRT+DVI(HDMI)	This feature allows you to select the display device when you boot up the system.

<p>LCD Panel Type</p>	<p>VBIOS 640x480 18/1, 800x600 18/1, 1024x768 18/1 [Default] 1280x1024 24/2, 1024x600 18/2, 1400x900 24/2, 1600x1200 18/2, 1280x768 18/1, 1680x1050 24/2, 1920x1080 24/2, 1024x768 24/1, 1366x768 24/1, 800x400 18/1, 1280x800 18/1, 1280x720 24/1, 2048x1536 24/2</p>	<p>This feature allows you to select Panel Resolution that will be displayed depending on the LCD Panel.</p>
<p>Panel Scaling</p>	<p>Auto [Default] Force Scaling, Off, Maintain Aspect Ratio.</p>	<p>Select the LCD panel scaling option used by the Internal Graphics Device.</p>
<p>Spread Spectrum clock Chip</p>	<p>Off[Default] Hardware Software</p>	<p>Choose the control option for Spread Spectrum Clock</p>
<p>ALS Support</p>	<p>Enabled, Disabled[Default]</p>	<p>Valid only for ACPI. Legacy = ALS Support through the IGD INT10 function. ACPI = ALS support through an ACPI ALS Driver.</p>
<p>GFX Low Power Mode</p>	<p>Enabled [Default] Disabled</p>	<p>Option applicable for SFF only</p>
<p>Active LFP</p>	<p>No LVDS Int-LDVS [Default] SDVO LVDS eDP Port-A eDP Port-B</p>	<p>Active LFP configuration.</p>
<p>PCIex16/ADD2 Select</p>	<p>PCIe [Default] ADD2-SDVO/HDMI</p>	<p>Select Slot for PCIex16 or ADD2 card</p>

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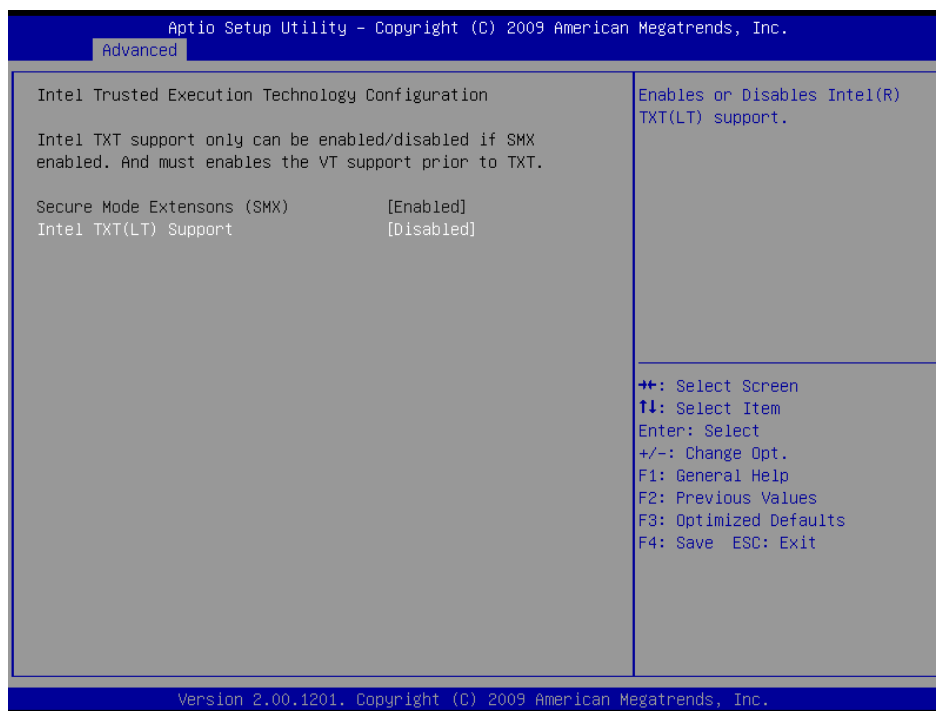
3.6.2.8 Intel TDT (AT-p) Configuration

This section allows you to configure Intel TDT (AT-p)



Item	Option	Description
TDT	Enabled, Disabled[Default]	Enable/ Disabled TDT in BIOS for testing only.
TDT Recovery	3	Set the number of times Recovery attempts will be allowed.

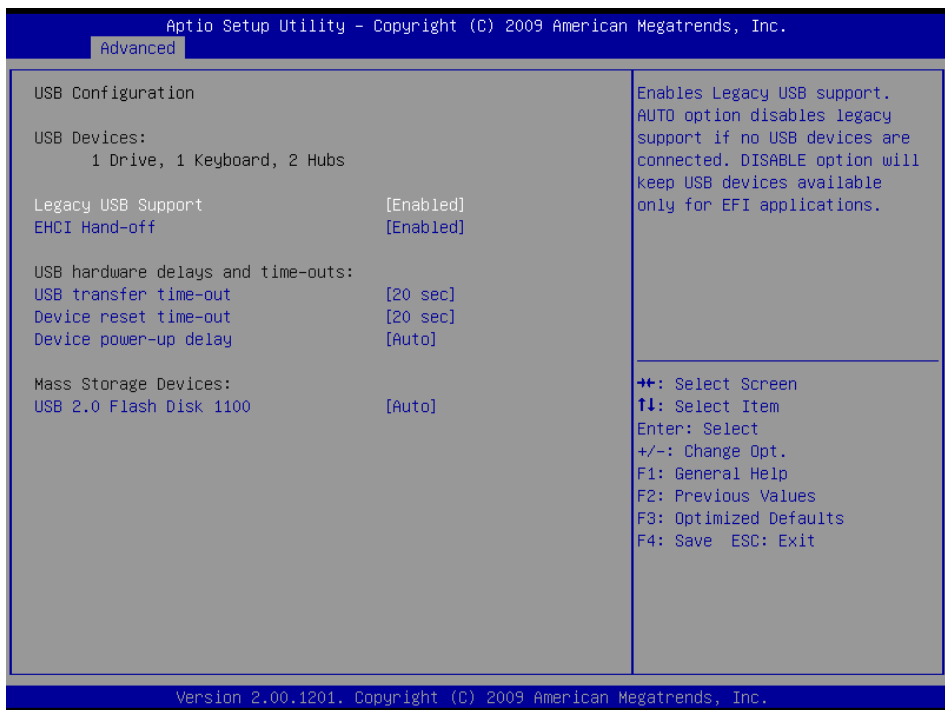
3.6.2.9 Intel TXT (LT) Configuration



Item	Option	Description
Secure Mode Extensions (SMX)	Enabled, Disabled [Default]	Interface for system software to support trust decisions by end user
Intel TXT (LT) Support	Enabled, Disabled [Default]	Hardware extension intended to provide a higher level of trust and control.

3.6.2.10 USB Configuration

The USB configuration menu is used to read USB configuration information and configure the USB setting.



3.6.2.10.1 Legacy USB support

Use the Legacy USB Support BIOS option to enable USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

Options: Enabled, Disabled, Auto

3.6.2.10.2 ECHI hand-off

This is a workaround for OSeS without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

Options: Enabled, Disabled

3.6.2.10.3 USB transfer timeout

Time-out value for Control, Bulk, and Interrupt transfers

Options 1, 5, 10, 20 Sec

3.6.2.10.4 Device Reset timeout

USB mass storage device start Unit command timeout.

Options: 10, 20, 30, 40 sec.

3.6.2.10.5 Device Power-up delay

This refers to the amount of Time taken by a device to properly report itself to the Host controller.

Options: Auto, Manual

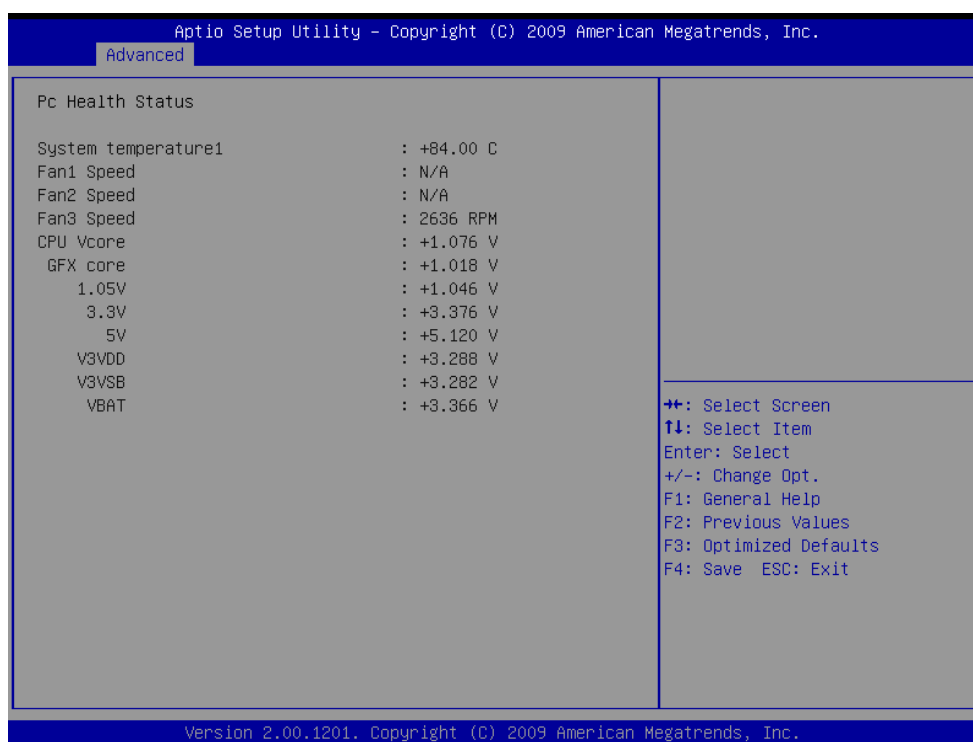
3.6.2.10.6 Mass Storage Devices

This item will show you the connected USB device at booting.

Example: USB 2.0 Flash Disk 1100.

3.6.2.11 H/W Monitor

The H/W Monitor shows the operating temperature, fan speeds and system voltages.



Temperature

- System temperature1

Fan1/2/3 speed

- Fan speed

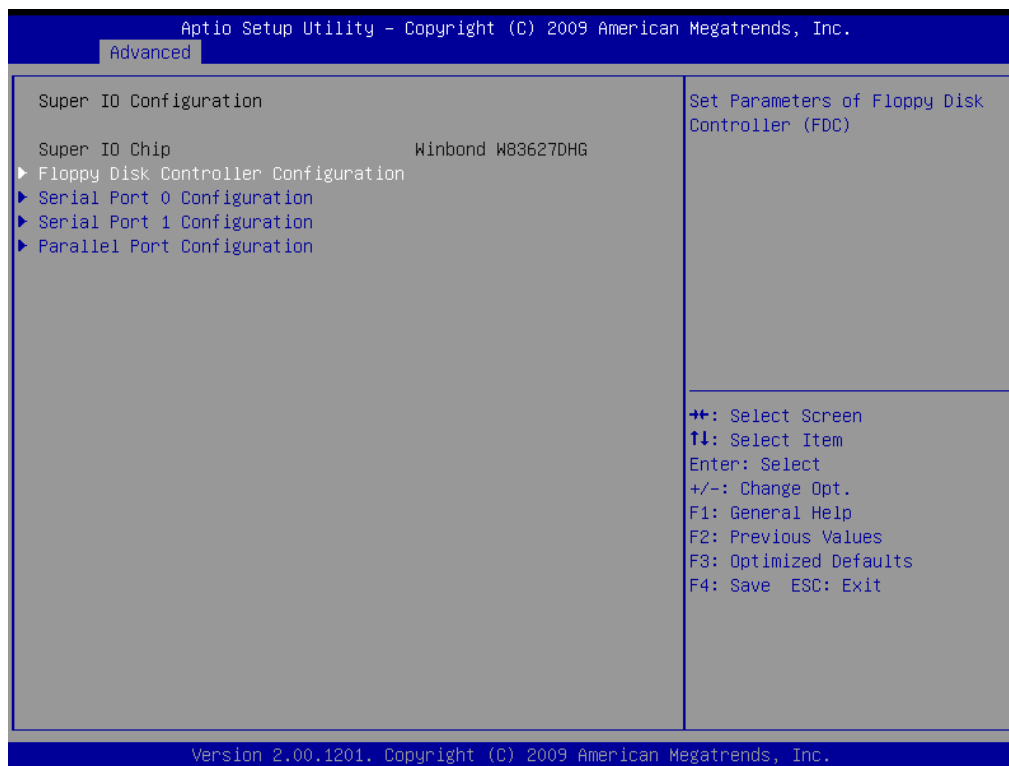
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Voltage

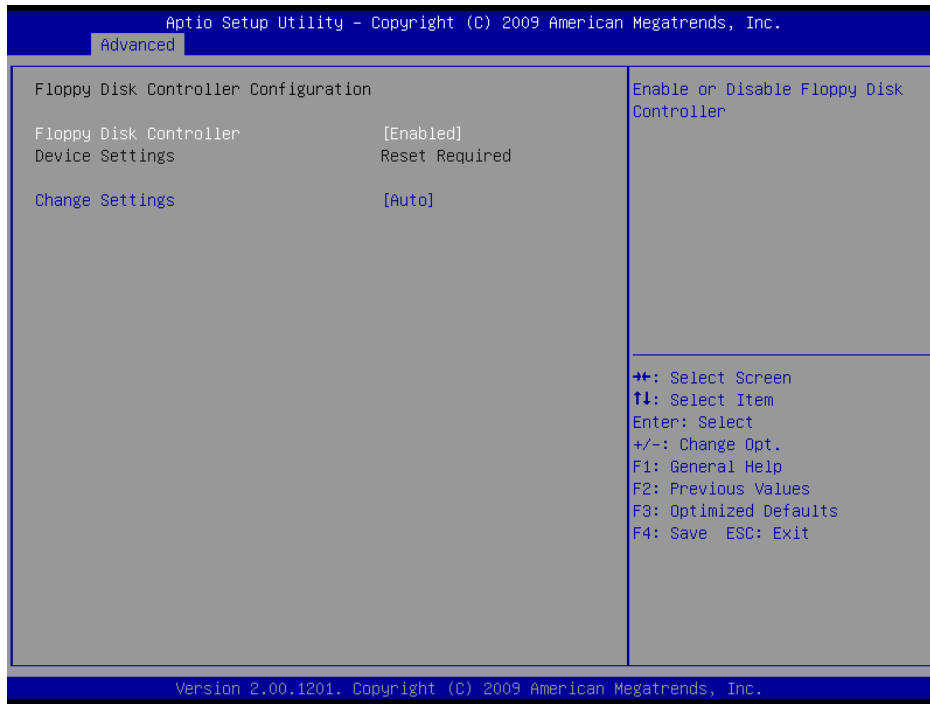
- CPUVCORE
- GFX core
- 1.05V
- 3.3V
- 5V
- V3VDD
- V3VSB
- VBAT

3.6.2.12 Super IO Configuration

You can use this item to set up or change the Super IO configuration for FDD controllers, parallel ports and serial ports.

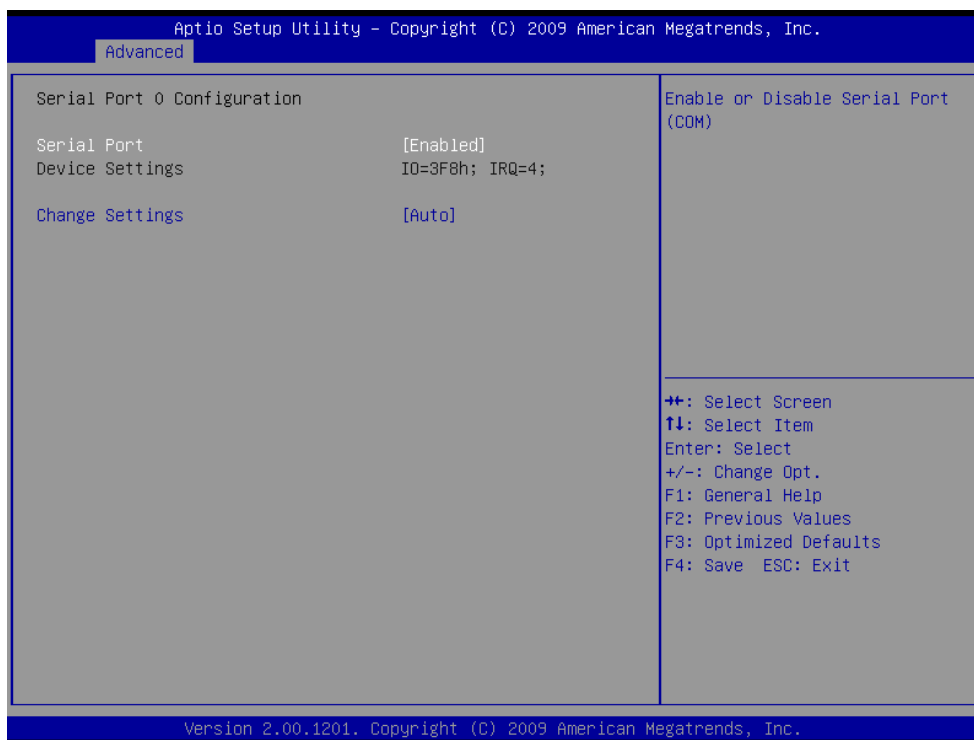


3.6.2.12.1 Floppy Disk Controller Configuration



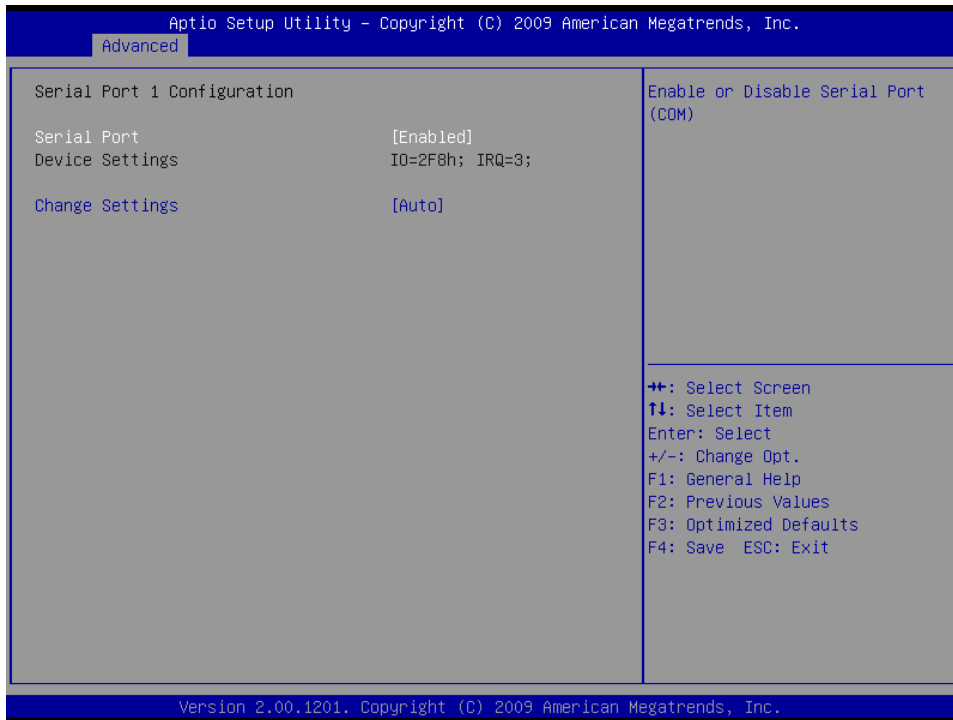
Item	Option	Description
Floppy Disk Controller	Enabled, Disabled	Enable or Disable Floppy Disk Controller.
Change settings	Auto IO=3F0h;IRQ=6;DMA=2; IO=3F0h;IRQ=3,4,5,6,7,10,11,12;DMA=2,3; IO=370h;IRQ=3,4,5,6,7,10,11,12;DMA=2,3;	Select an optimal setting for Super IO device.

3.6.2.12.2 Serial Port 0 Configuration



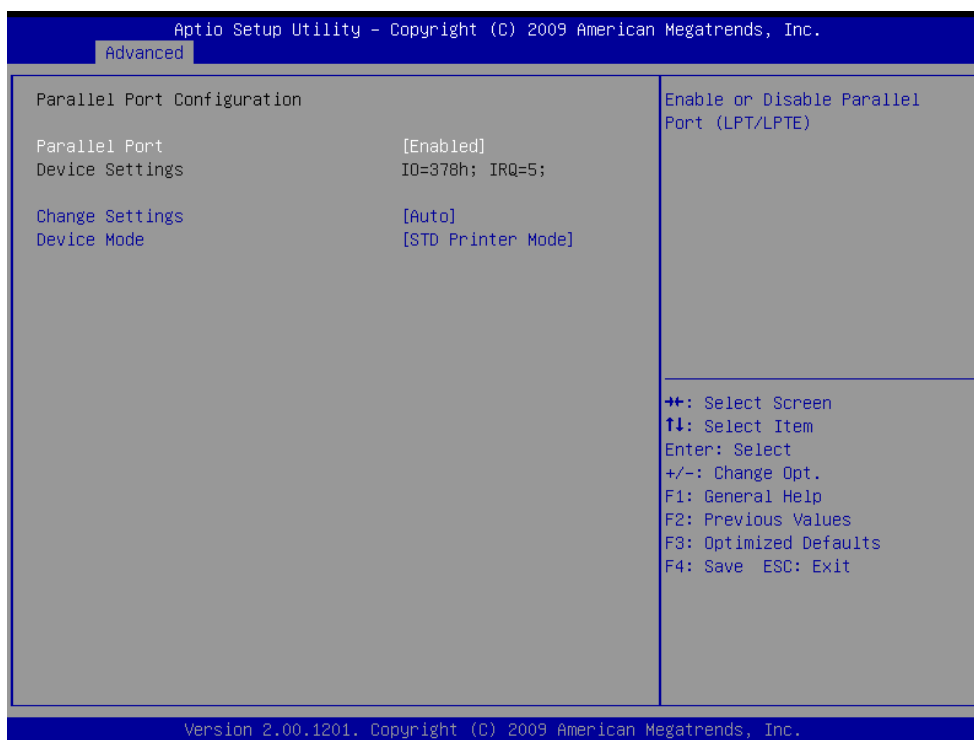
Item	Option	Description
Serial Port	Enabled, Disabled	Use the Serial port option to enable or disable the serial port.
Change Settings	IO=3F8h; IRQ=4, IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Use the change Settings option to change the serial port IO port address and interrupt address.

3.6.2.12.3 Serial Port 1 Configuration



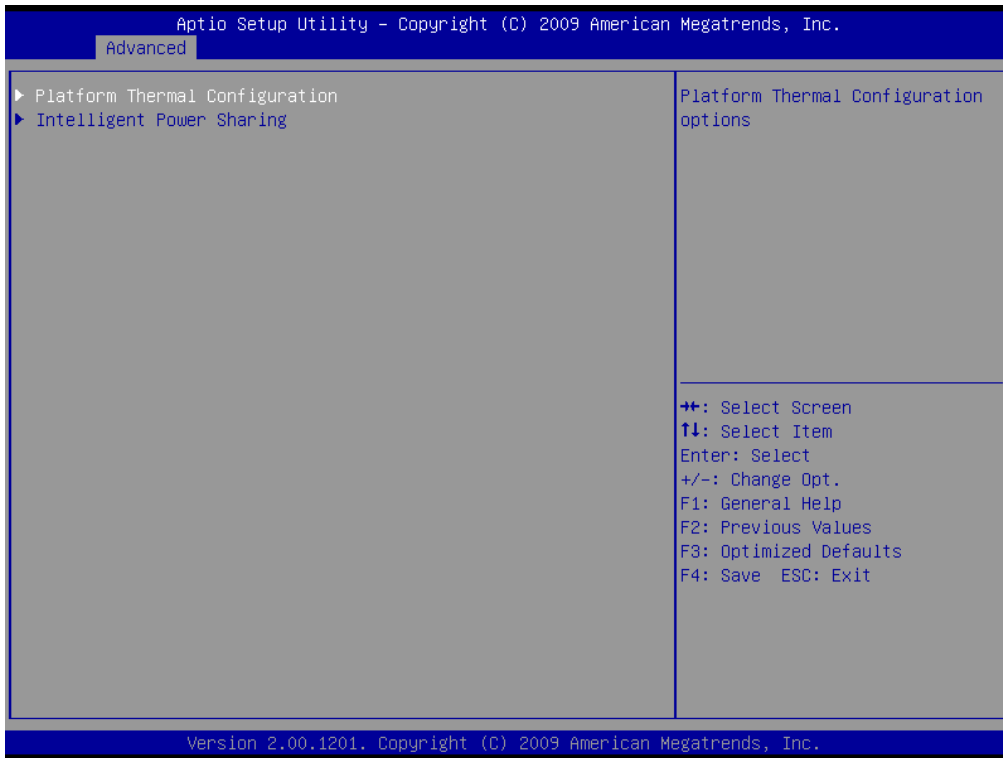
Item	Option	Description
Serial Port	Enabled, Disabled	Use the Serial port option to enable or disable the serial port.
Change Settings	IO=2F8h; IRQ=3, IO=3F8h; IRQ=3,4,5,6,7,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,10,11,12	Use the change Settings option to change the serial port IO port address and interrupt address.

3.6.2.12.4 Parallel Port Configuration

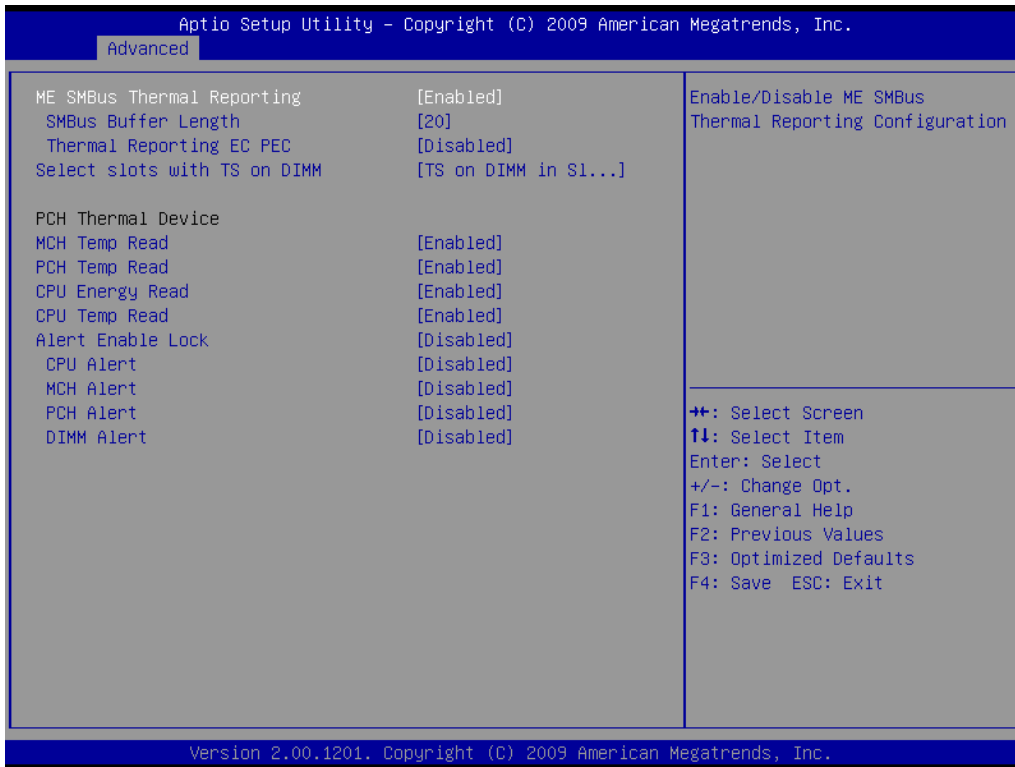


Item	Option	Description
Parallel Port	Enabled, Disabled	Enable or disable Parallel Port (LPT/LPTE)
Change Settings	Auto IO=3F8h; IRQ=5	Select Optimal setting for Super IO device
Device Mode	STD Printer Mode SPP Mode EPP-1.9 and SPP Mode EPP-1.7 and SPP Mode ECP Mode ECP Mode and EPP-1.9 ECP Mode and EPP-1.7	Change Printer port mode

3.6.2.13 Thermal Configuration



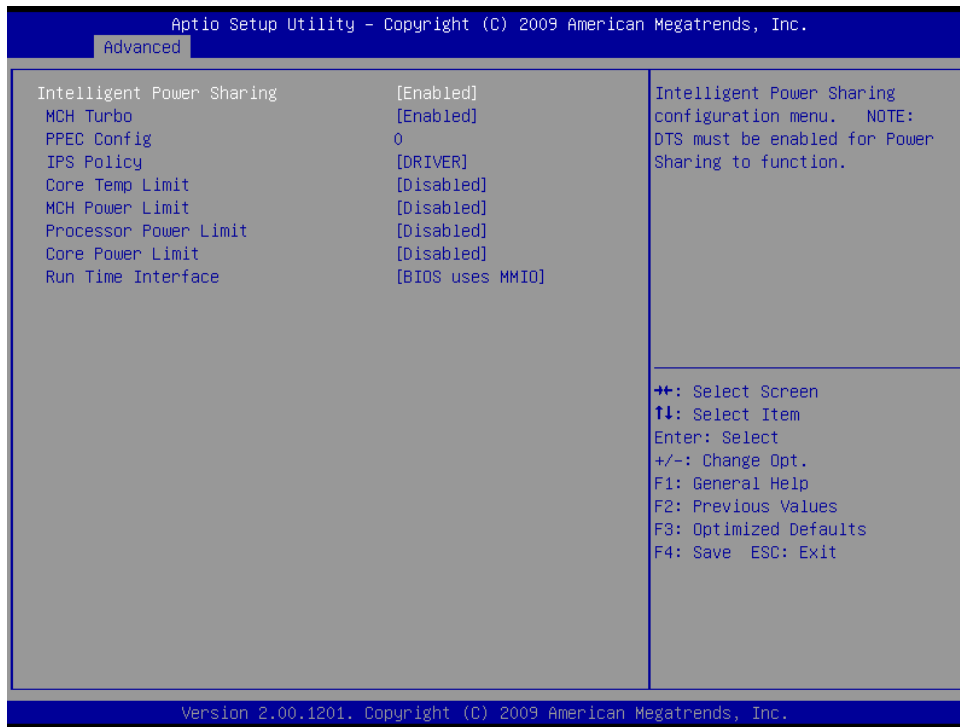
3.6.2.13.1 Platform thermal Configuration



Item	Option	Description
ME SMBus Thermal Reporting	Disabled, Enabled	Enabled/ Disabled ME SMBus Thermal Reporting Configuration.
SMBus Buffer Length	1, 2, 5, 9, 10, 14, 20	SMBus Block Read message length for EC.
Thermal Reporting EC PEC	Disabled, Enabled	Enable Packet Error Checking (PEC) for SMBus Block Read.
Select slots with TS on DIMM	No TS on DIMM, TS on DIMM in Slot SODIMM0, TS on DIMM in Slot SODIMM1, TS on DIMM in Slot SODIMM0 and SODIMM1	Enable temperature reporting for slots with TS on DIMM. NOTE: SODIMM0 is one of the one closer to CUP.
MCH Temp Read	Disabled, Enabled	MCH Temperature Read Enabled.
PCH Temp Read	Disabled, Enabled	PCH Temperature Read Enabled.
CPU Energy Read	Disabled, Enabled	CPU Energy Read Enabled.
CPU Temp Read	Disabled, Enabled	CPU Temperature Read Enabled.
Alert Enable Lock	Enabled, Disabled	Lock all Alert Enable settings.
CPU Alert	Enabled, Disabled	CPU Alert pin enabled.
MCH Alert	Enabled, Disabled	MCH Alert pin enabled..
PCH Alert	Enabled, Disabled	PCH Alert pin enabled.
DIMM Alert	Enabled, Disabled	DIMM Alert pin enabled.

3.6.2.13.2 Intelligent Power Sharing

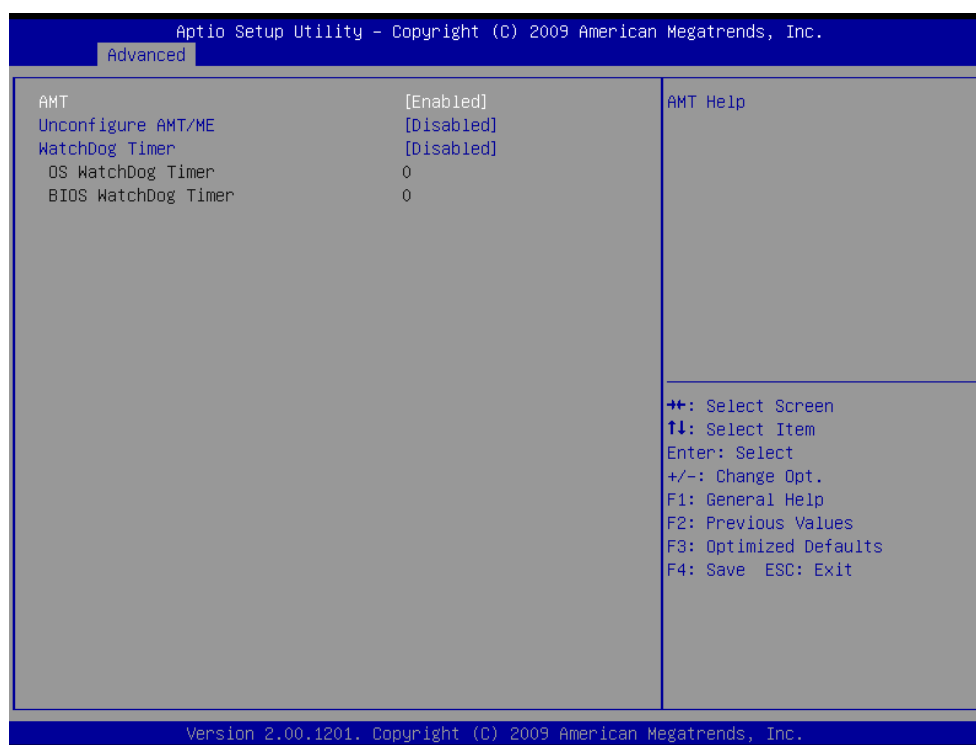
The section helps configure Intelligent Power Sharing.



Item	Option	Description
MCH Turbo	Enabled, Disabled	Enable or disable MCH Turbo.
PPEC Config	0	Processor Power Error Correction.
IPS Policy	DRIVER, PROCESSOR, BALANCED, GRAPHICS	Platform BIOS Policy Preference.
Core Temp Limit	Enabled, Disabled	Core temperature limit.
MCH Power Limit	Enabled, Disabled	Max MCH power clamp.
Processor Power Limit	Enabled, Disabled	Max processor power clamp.
Core Power Limit	Enabled, Disabled	Max core power clamp.
Run Time Interface	EC uses SMBus, BIOS uses MMIO	Choose runtime interface for PCH communication.

3.6.2.14 AMT Configuration

This item allows Advance Power Management configuration

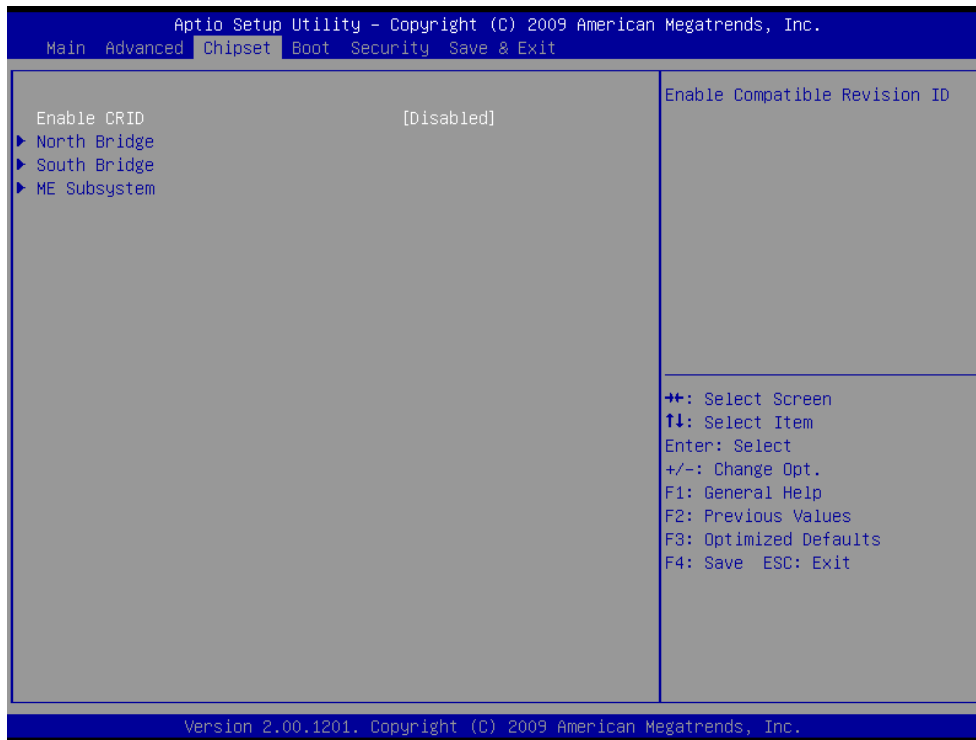


Item	Option	Description
AMT	Enabled, Disabled	Use AMT option to enable/disable the Intel® AMT function.
Unconfigure AMT/ME	Enabled, Disabled	You can use this item to perform AMT/ME unconfigure without password operation.
WatchDog Timer	Enabled, Disabled	This option will determine watch dog timer.

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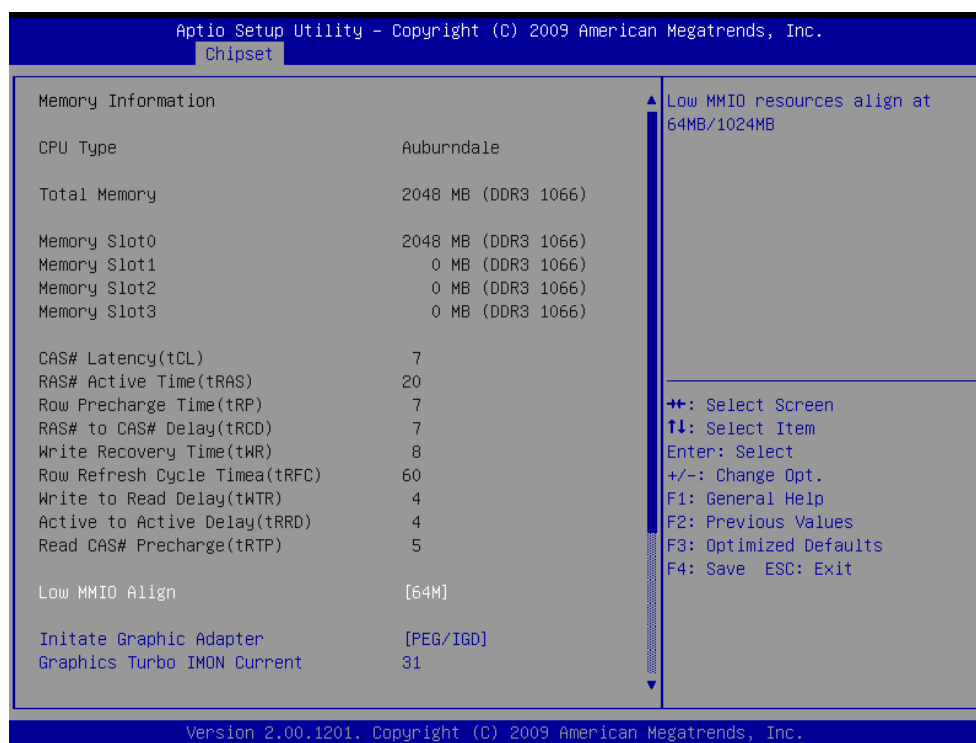
3.6.3 Advanced Chipset Features

This option configures the north bridge, south bridge and ME subsystem.



Item	Option	Description
Enable CRID	Enable Disabled	Enable/disabled Compatible Revision ID

3.6.3.1 North Bridge



3.6.3.1.1 CAS # Latency (tCL)

This item controls the time delay (in clock cycles - CLKs) that passes before the SDRAM starts to carry out a read command after receiving it. This also determines the number of CLKs for the completion of the first part of a burst transfer. In other words, the lower the latency, the faster the transaction.

3.6.3.1.2 RAS # Active Time (tRAS)

It allows controlling the memory bank's minimum row active time (tRAS). This constitutes the time when a row is activated until the time the same row can be deactivated. If the tRAS period is too long, it can reduce performance by unnecessarily delaying the deactivation of active rows. Reducing the tRAS period allows the active row to be deactivated earlier. If the tRAS period is too short, there may not be enough time to complete a burst transfer. This reduces performance and data may be lost or corrupted.

3.6.3.1.3 Row Precharge Time (tRP)

This option sets the number of cycles required for the RAS to accumulate its charge before the SDRAM refreshes.

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3.6.3.1.4 RAS# to CAS# Delay (tRCD)

This option allows you to insert a delay between the RAS (**Row Address Strobe**) and CAS (**Column Address Strobe**) signals. This delay occurs when the SDRAM is written to, read from or refreshed. Naturally, reducing the delay improves the performance of the SDRAM while increasing it reduces performance.

3.6.3.1.5 Write Recovery Time (tWR)

It shows the delay (in clocks cycles) that must elapse after the completion of a valid write operation. The shorter the delay, the earlier the bank can be precharged for another read/write operation.

3.6.3.1.6 Row Refresh Cycle (tRFC)

Determines the number of clock measured from a Refresh command (REF) until the first Activate command (ACT) to the same rank

3.6.3.1.7 Write to Read Delay (tWTR)

This constitutes the minimum number of clock cycles that must occur between the last valid write operation and the next read command to the same internal bank of the DDR device.

3.6.3.1.8 Active to Active (tRRD)

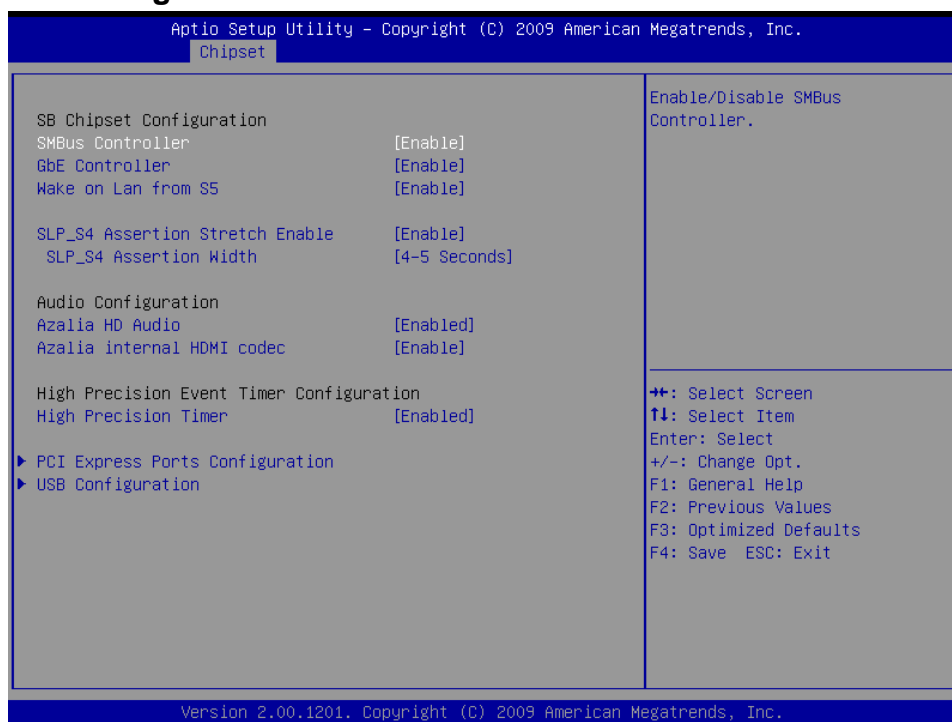
The minimum time interval between successive ACTIVE commands to the different banks is defined by tRRD.

3.6.3.1.9 Read CAS# Precharge (tRTP)

Number of clocks that are inserted between a read commands to a row pre-charge command to the same rank.

Item	Option	Description
Low MMIO Align	64M, 1024M	This option will determine Low MMIO resources align.
Initiate Graphic Adapter	IGD, PCI/IGD ; PCI/PEG, PEG/IGD ; PEG/PCI	This item allows you to select which graphics controller to use as the primary boot device.
Graphics Turbo IMON Current	Min= 14, Max= 31	Graphics turbo IMON current values supported.

3.6.3.2 South Bridge

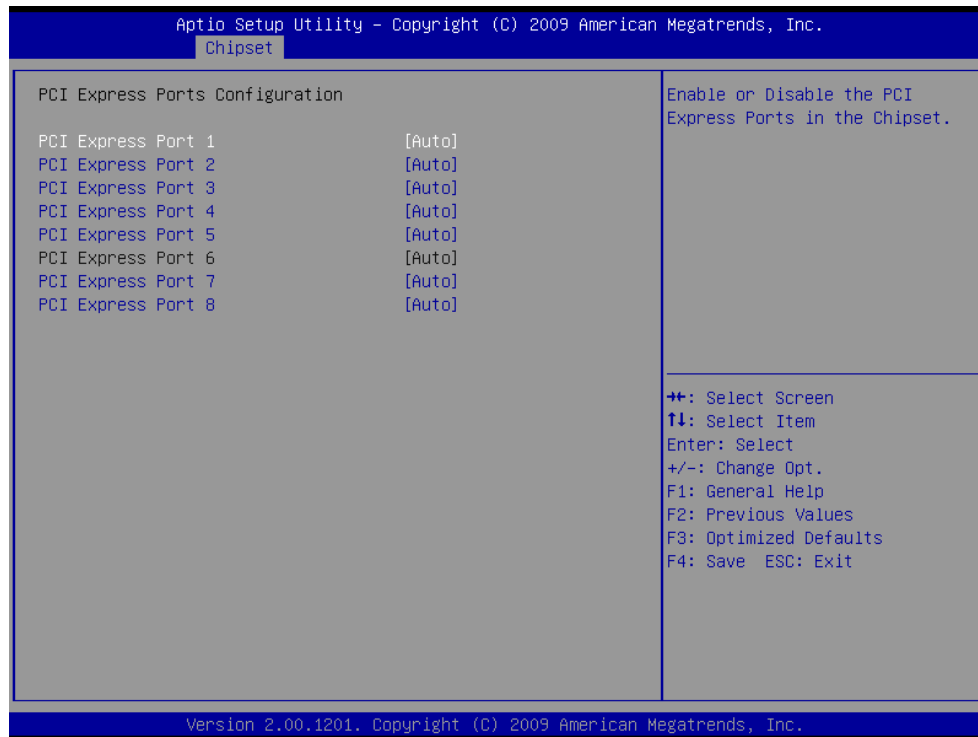


Item	Option	Description
SMBus Controller	Enabled, Disabled	SMBus Controller help.
GbE Controller	Enabled, Disabled	GbE Controller help.
Wake on Lan from S5	Enabled, Disabled	Wake on Lan from S5 help.
SLP_S4 Assertion Stretch Enable	Enabled, Disabled	Enable or Disable SLP_S4 Assertion Stretch
SLP_S4 Assertion Width	1-2 seconds 2-3 seconds 3-4 seconds 4-5 seconds	Select a minimum assertion width of the SLP_S4 signal
Azalia HD Audio	Enabled, Disabled	Use the Azalia HD Audio option to enable or disable the High Definition Audio controller.
Azalia internal HDMI codec	Enabled, Disabled	Enable/ Disable internal HDMI codec for Azalia.
High Precision Timer	Enable, Disabled	This item helps to enable or disable high precision timer.

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3.6.3.2.1 PCI Express Ports Configuration

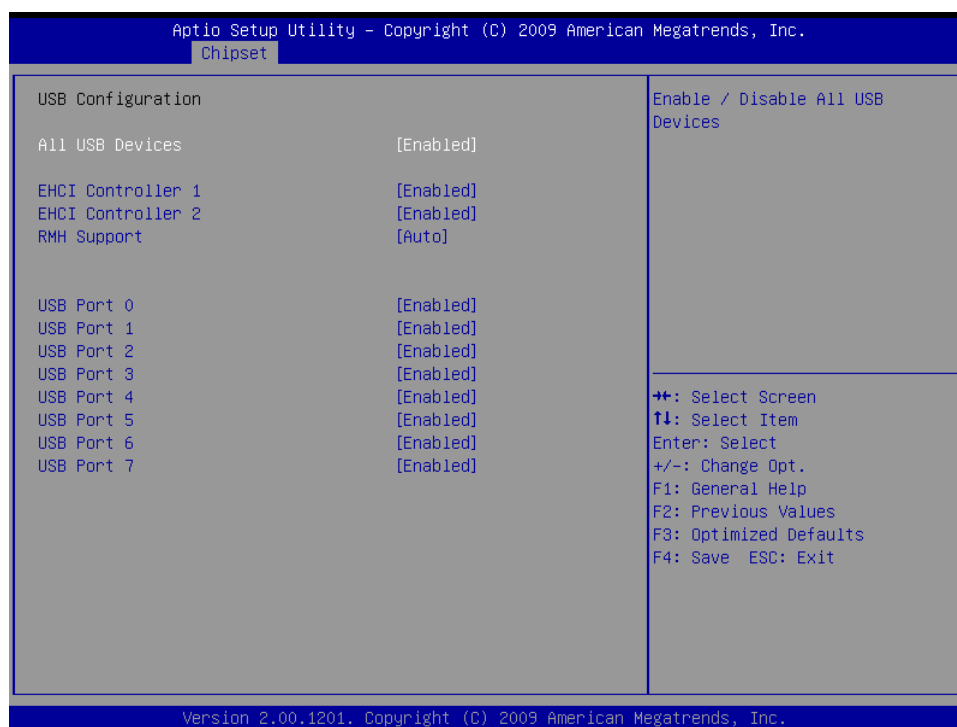
For the PCI Express root ports, the assignment of a function number to a root port is not fixed. This item allows you to re-assign the function numbers on a port by port basis. You can disable/hide any root port and still have functions 0 thru N-1 where N is the total number of enabled root ports.



Options: Disable, Enabled, Auto.

3.6.3.2.2 USB Configuration

The USB Configuration menu is used to read USB configuration information and configure the USB settings.

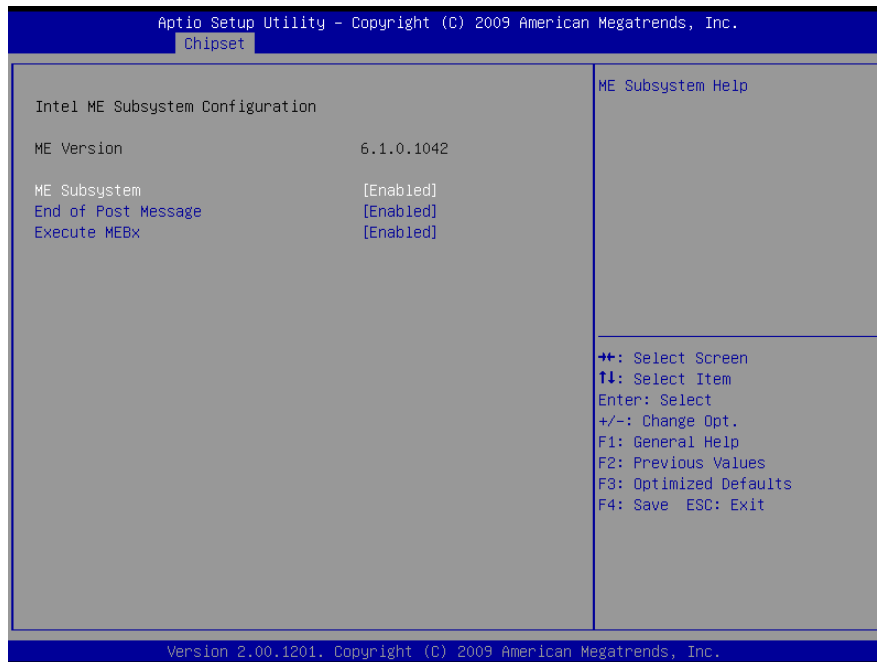


Item	Option	Description
EHCI controller 1/2	Enabled	Enabled/Disabled USB 2.0 (EHCI)
	Disabled	
RMH support	Enabled	Enabled/Disabled RMH Support; AUTO: Enable RMH support on Ibex Peak Bx stepping or above
	Disabled	
	Auto	
USB Port	Enabled	To enable or disable USB Ports
	Disabled	

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3.6.3.3 ME Subsystem

Use the ME Subsystem menu to configure the Intel® Management Engine (ME) configuration options.



Item	Option	Description
ME Subsystem	Enabled, Disabled	Use the ME Subsystem option to enable or disable the Intel® ME subsystem.
End of Post Message	Enabled, Disabled	Use the End of Post Message option to enable or disable the end of post message of the ME Subsystem.
Execute MEBx	Enabled, Disabled	Use the Execute MEBx option to enable or disable the Intel® Management Engine BIOS extension (MEBx).

3.6.4 Boot

Use Boot menu to set system boot options.

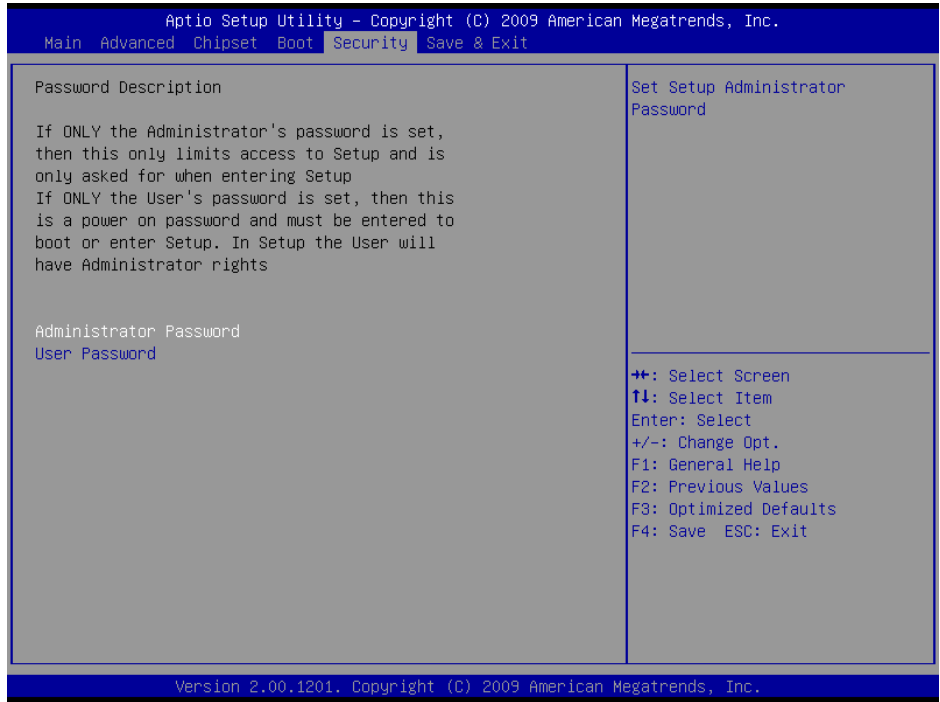


Item	Option	Description
Quiet Boot	Enabled, Disabled	This item can help to select the screen display when the system boots.
Fast Boot	Enabled, Disabled	Enabled/ Disabled boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
Setup Prompt Timeout	1	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	On, Off	Select the keyboard NumLock state.
GateA20 Active	Upon Request, Always	UPON REQUEST – GA20 can be disabled using BIOS services. ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Option ROM Messages	Force BIOS, Keep Current	Set display mode for Option ROM.
Interrupt 19 Capture	Enabled, Disabled	Enabled: Allows Option ROMs to trap int 19.

<p>Boot option 1/2/3</p>	<p>These settings specify the boot priority of hard drive devices. The highest priority device is displayed on the main Boot Option Priorities list.</p>
<p>Hard drive BBS priorities</p>	<p>Use this setting to access the Hard Drive BBS Priorities submenu to re-order or disable bootable hard drive devices.</p>

3.6.5 Security

Use the Security menu to set system and user password.



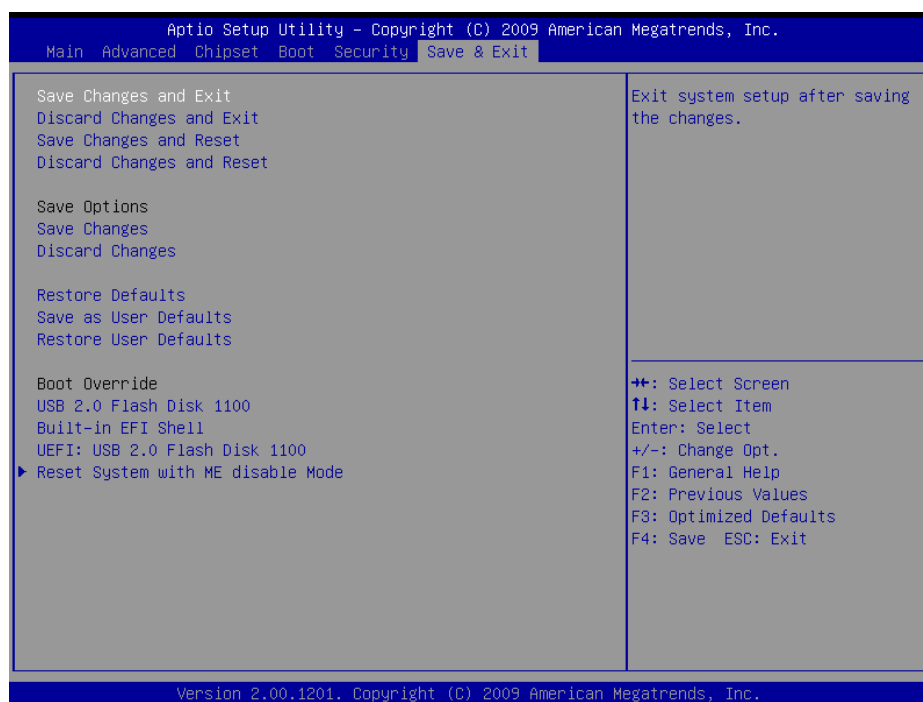
3.6.5.1 Administrator Password

This setting specifies a password that must be entered to access the BIOS Setup Utility. If only the Administrator's password is set, then this only limits access to the BIOS setup program and is only asked for when entering the BIOS setup program. By default, no password is specified.

3.6.5.2 User Password

This setting specifies a password that must be entered to access the BIOS Setup Utility or to boot the system. If only the User's password is set, then this is a power on password and must be entered to boot or enter the BIOS setup program. In the BIOS setup program, the User will have Administrator rights. By default, no password is specified.

3.6.6 Save & Exit



3.6.6.1 Save Changes and Exit

Use the save changes and reset option to save the changes made to the BIOS options and to exit the BIOS configuration setup program.

3.6.6.2 Discard Changes and Exit

Use the Discard changes and Exit option to exit the system without saving the changes made to the BIOS configuration setup program.

3.6.6.3 Save Changes and Reset

Any changes made to BIOS settings are stored in NVRAM. The setup program then exits and reboots the controller.

3.6.6.4 Discard Changes and Reset

Any changes made to BIOS settings during this session of the BIOS setup program are discarded. The setup program then exits and reboots the controller.

3.6.6.5 Save Changes

Changes made to BIOS settings during this session are committed to NVRAM. The setup program remains active, allowing further changes.

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3.6.6.6 Discard Changes

Any changes made to BIOS settings during this session of the BIOS setup program are discarded. The BIOS setup continues to be active.

3.6.6.7 Restore Defaults

This option restores all BIOS settings to the factory default. This option is useful if the controller exhibits unpredictable behavior due to an incorrect or inappropriate BIOS setting.

3.6.6.8 Save as user defaults

This option saves a copy of the current BIOS settings as the User Defaults. This option is useful for preserving custom BIOS setup configurations.

3.6.6.9 Restore as user defaults

This option restores all BIOS settings to the user defaults. This option is useful for restoring previously preserved custom BIOS setup configurations.

3.6.6.10 Boot override

This option lists all possible bootable devices and allows the user to override the **Boot Option Priorities** list for the current boot. If no changes have been made to the BIOS setup options, the system will continue booting to the selected device without first rebooting. If BIOS setup options have been changed and saved, a reboot will be required and the boot override selection will not be valid.

3.6.6.11 Reset system with ME disable mode

This option allows or prevents firmware local update in the field. When the “Enabled” option is selected, the IT-admin is able to update the ME locally via the local Management Engine interface or via the local secure interface.. Once the local update is complete, this setting is automatically set to “Disabled”. This option must be set to “Enabled” when a local update is needed.

4. Drivers Installation



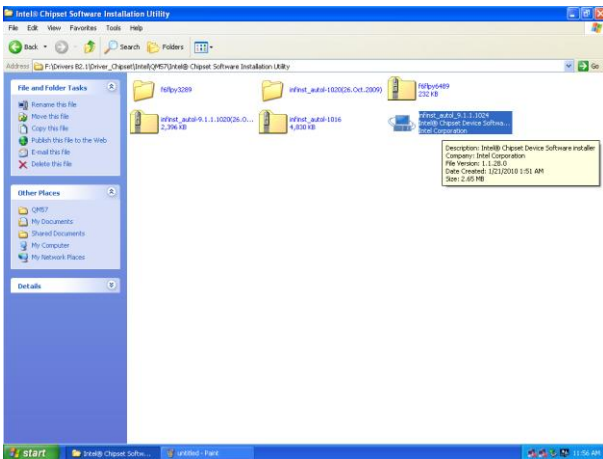
Note: Installation procedures and screen shots in this section are for your reference and may not be exactly the same as shown on your screen.

4.1 Install Chipset Driver (For Intel QM57)

Insert the Supporting DVD-ROM to DVD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to \Driver_Chipset\Intel\ QM57.



Note: The installation procedures and screen shots in this section are based on Windows XP operation system. If the warning message appears while the installation process, click Continue to go on.



Step1. Locate 「\Driver_Chipset\Intel\ QM57\ \infinst_autol.exe」 .



Step 2. Click **Next**.



Step 3. Click **Next**.



Step 4. Click **Finish** to complete setup.

4.2 Install Display Driver (For Intel QM57)

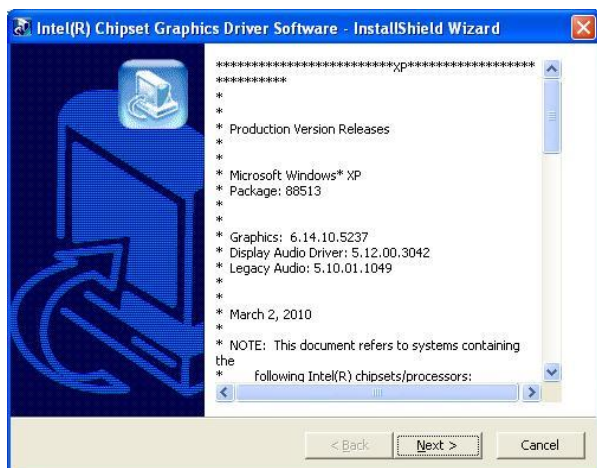
Insert the Supporting DVD-ROM to DVD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to \Driver_Video\Intel\QM57.



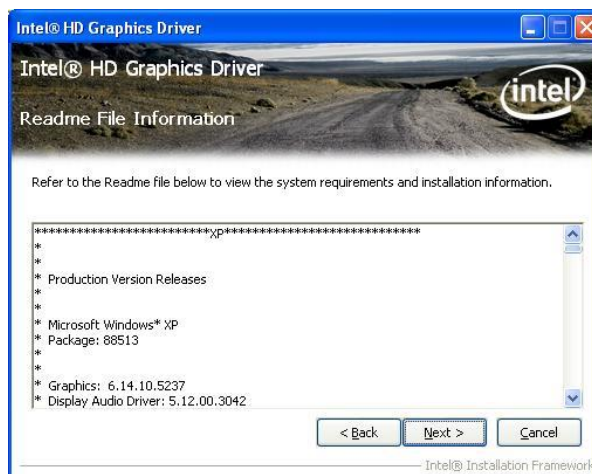
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



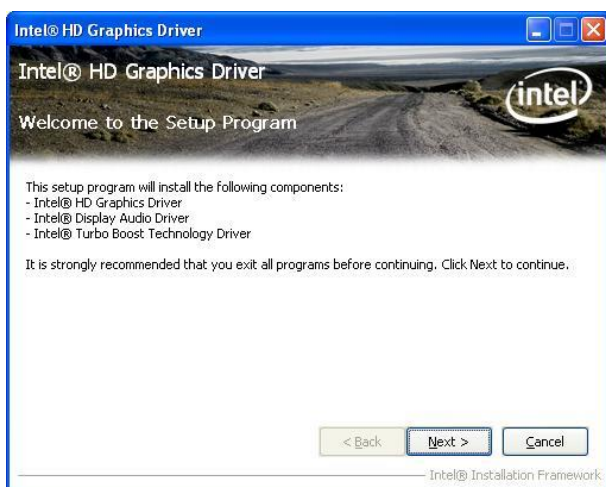
Step 3. Click **Yes**.



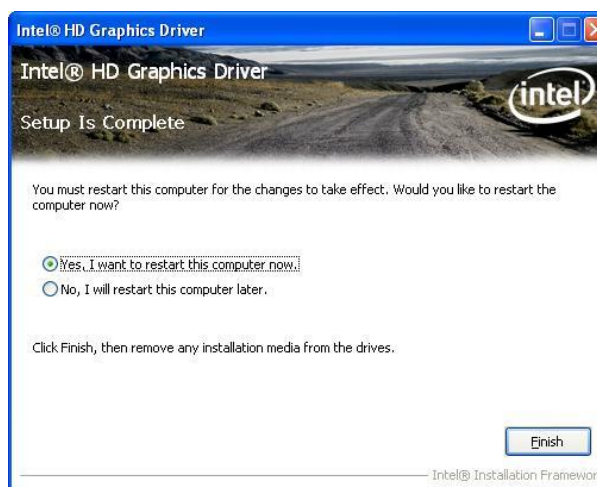
Step 1. Locate 「Driver_Video\Intel\QM57\Setup.exe」. Click **Next**



Step 4. Click **Next**.



Step 2. Click **Next**.



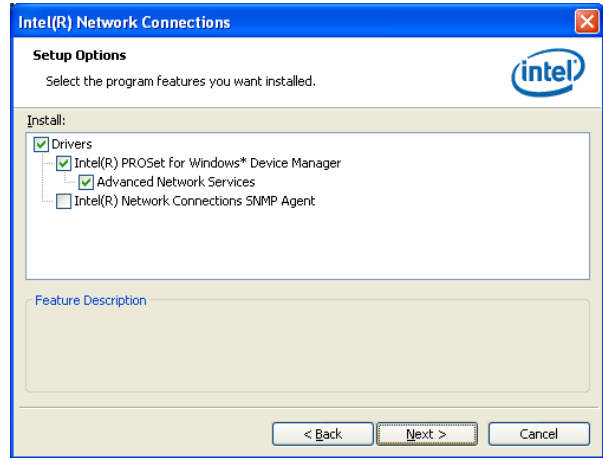
Step 5. Click **Finish** to complete setup.

4.3 Install Ethernet Driver (For Intel 82574L/ 82577LM)

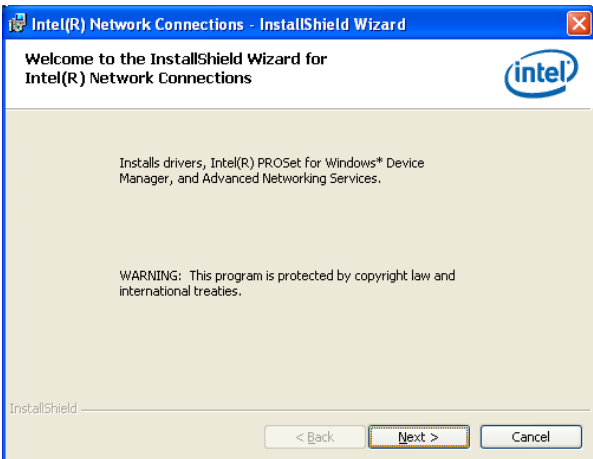
Insert the Supporting DVD-ROM to DVD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **D:\Driver_Gigabit\Intel\ 82574L or 82577LM**.



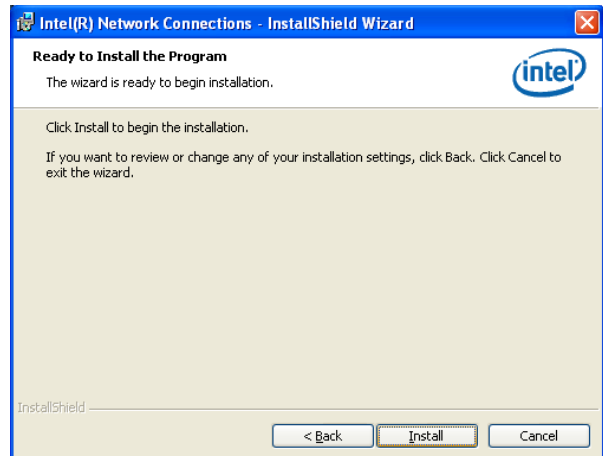
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



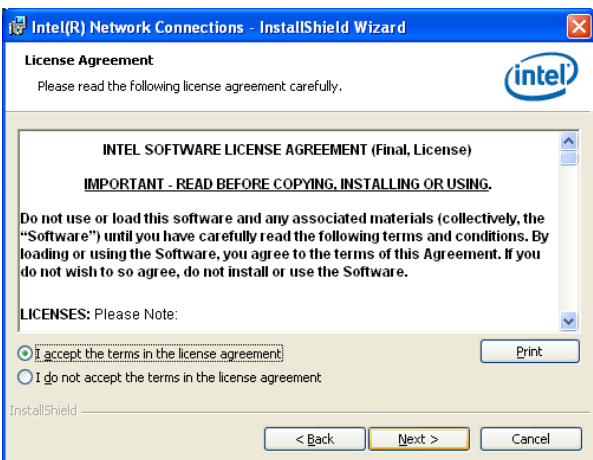
Step 3. Click Next.



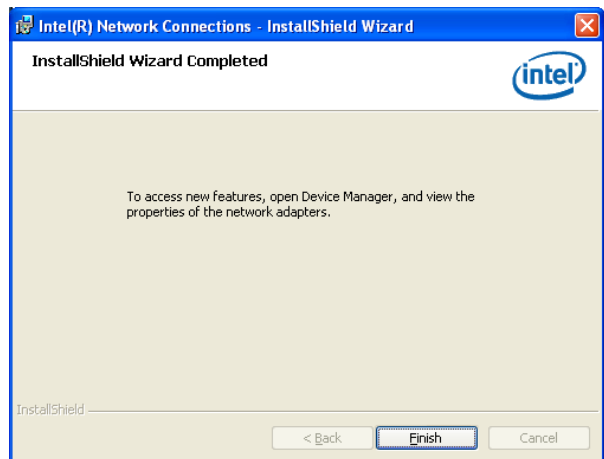
Step 1. Locate 「 \Driver_Gigabit\Intel\ 82574L or 82577LM 」 and Click Next



Step 4. Click Install to next step.



Step 2. Click Accept to continue.

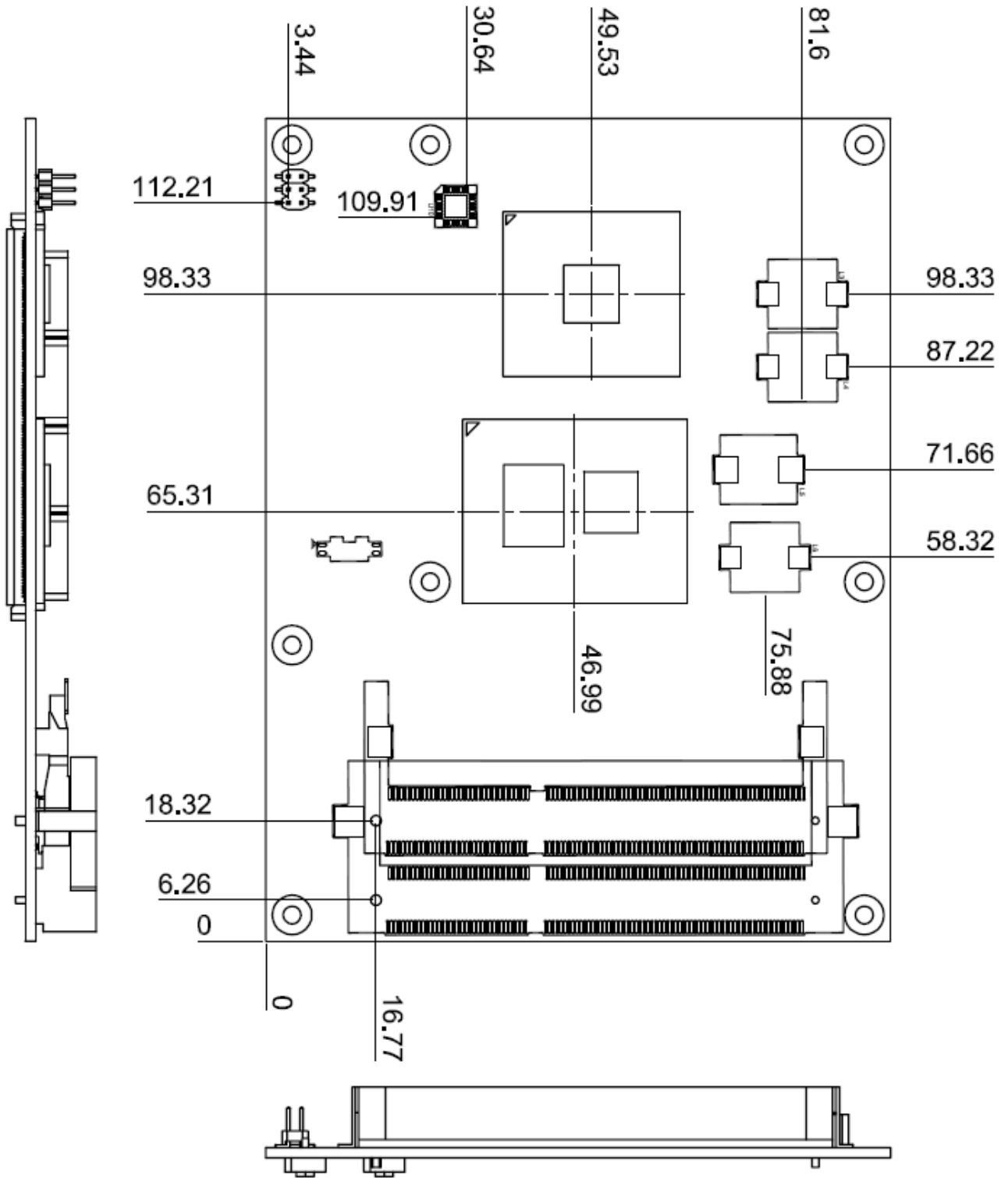


Step 5. Click Finish to complete the setup.

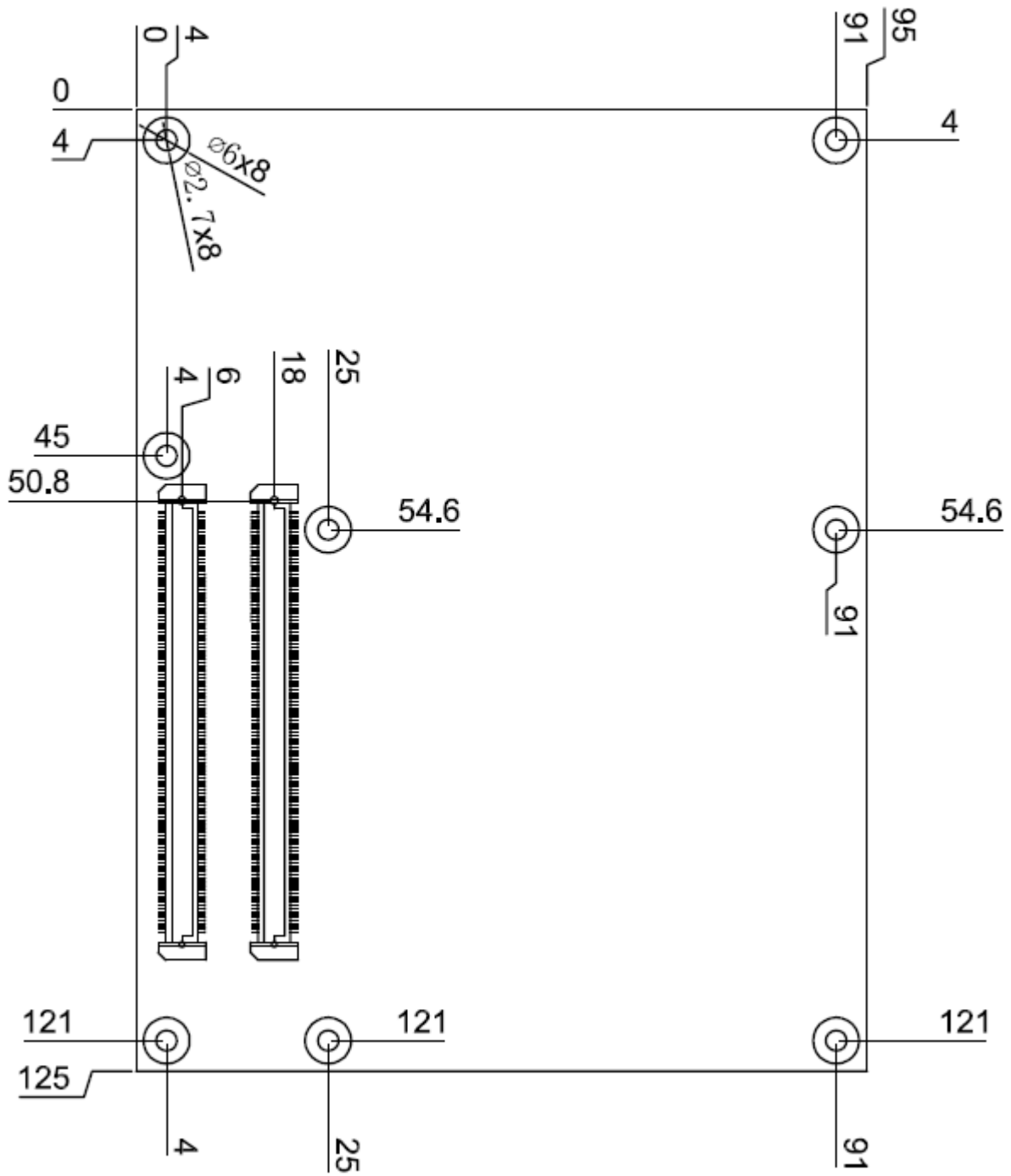
5. Mechanical Drawing



ESM-QM57



Unit: mm



Unit: mm