ESM-CN700 Series

Onboard VIA Eden V4 1 GHz SOM-ETX CPU Module

User's Manual

1st Ed – 26 October 2006

Part No. 2047274100R

FCC Statement

THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

THESE LIMITS ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINTST HARMFUL INTERFERENCE WHEN THE EQUIPMENT IS OPERATED IN A COMMERCIAL ENVIRONMENT. THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTATLLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE HARMFUL INTERFERENCE TO RADIO COMMUNICATIONS.

OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE HARMFUL INTERFERENCE IN WHICH CASE THE USER WILL BE REQUIRED TO CORRECT THE INTERFERENCE AT HIS OWN EXPENSE.

Notice

This guide is designed for experienced users to setup the system within the shortest time. For detailed information, please always refer to the electronic user's manual.

Copyright Notice

Trademark Acknowledgement

Brand and product names are trademarks or registered trademarks of their respective owners.

Disclaimer

Evalue Technology Inc. reserves the right to make changes, without notice, to any product, including circuits and/or software described or contained in this manual in order to improve design and/or performance. Evalue Technology assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright, or masks work rights to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described in this manual are for illustration purposes only. Evalue Technology Inc. makes no representation or warranty that such application will be suitable for the specified use without further testing or modification.

Life Support Policy

Evalue Technology's PRODUCTS ARE NOT FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE PRIOR WRITTEN APPROVAL OF Evalue Technology Inc.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

A Message to the Customer

Evalue Customer Services

Each and every Evalue's product is built to the most exacting specifications to ensure reliable performance in the harsh and demanding conditions typical of industrial environments. Whether your new Evalue device is destined for the laboratory or the factory floor, you can be assured that your product will provide the reliability and ease of operation for which the name Evalue has come to be known.

Your satisfaction is our primary concern. Here is a guide to Evalue's customer services. To ensure you get the full benefit of our services, please follow the instructions below carefully.

Technical Support

We want you to get the maximum performance from your products. So if you run into technical difficulties, we are here to help. For the most frequently asked questions, you can easily find answers in your product documentation. These answers are normally a lot more detailed than the ones we can give over the phone. So please consult the user's manual first.

To receive the latest version of the user's manual; please visit our Web site at:
http://www.evalue-tech.com/

If you still cannot find the answer, gather all the information or questions that apply to your problem, and with the product close at hand, call your dealer. Our dealers are well trained and ready to give you the support you need to get the most from your Evalue's products. In fact, most problems reported are minor and are able to be easily solved over the phone.
In addition, free technical support is available from Evalue's engineers every business day. We are always ready to give advice on application requirements or specific information on the installation and operation of any of our products. Please do not hesitate to call or e-mail us.

Headquarters
Evalue Technology Inc.
7F, 228, Lian-cheng Road,
Chung Ho City, Taipei,
Taiwan
Tel : +886-2-8226-2345
Fax : +886-2-8226-2777
http://www.evalue-tech.com
E-mail: service@evalue-tech.com

Europe Branch Office
Evalue Europe A/S
Stenholtsvej 13,
3480 Fredensborg,
Denmark
Tel : +45-7025-0310
Fax : +45-4975-5026
http://www.evalue-tech.com
E-mail: service.europe@evalue-tech.com

China Branch Office
Evalue Technology Shanghai Inc.
Room 909, 9F, Section B, No.900,
Yisan Road, Caohejing Hi-tech Park,
Shanghai 200233, China
Tel : +86-21-5423-4170
Fax : +86-21-5423-4171
http://www.evalue-tech.com
E-mail: service.china@evalue-tech.com

US Branch Office
Evalue Technology Inc.
Suite 210, 200 Tornillo Way,
Tinton Falls, NJ 07712
USA
Tel: +1-732-578-0200
Fax: +1-732-578-0250
http://www.evalue-tech.com
E-mail: service.usa@evalue-tech.com

Product Warranty

Evalue warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Evalue, or which have been subject to misuse, abuse, accident or improper installation. Evalue assumes no liability under the terms of this warranty as a consequence of such events. Because of Evalue's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If any of Evalue's products is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details. If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU type and speed, Evalue's products model name, hardware & BIOS revision number, other hardware and software used, etc.) Note anything abnormal and list any on-screen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information available.
3. If your product is diagnosed as defective, obtain an RMA (return material authorization) number from your dealer. This allows us to process your good return more quickly.
4. Carefully pack the defective product, a complete Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Contents

1. Getting started

1.1 Safety Precautions

Warning!

Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!

Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

1.2 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 x ESM-CN700 Onboard VIA Eden V4 1 GHz SOM-ETX CPU Module
- 1 x Quick Installation Guide
- 1 x CD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - VGA drivers and utilities
  - Audio drivers and utilities
  - Ethernet driver and utilities

If any of the above items is damaged or missing, contact your retailer.

1.3 Document Amendment History

Revision	Date	By	Comment
1st	Oct. 2006	Lingo Tsai	Initial Release

1.4 Manual Objectives

This manual describes in detail the Evalue Technology ESM-CN700 SOM-ETX CPU Module.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with ESM-CN700 or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

1.5 System Specifications

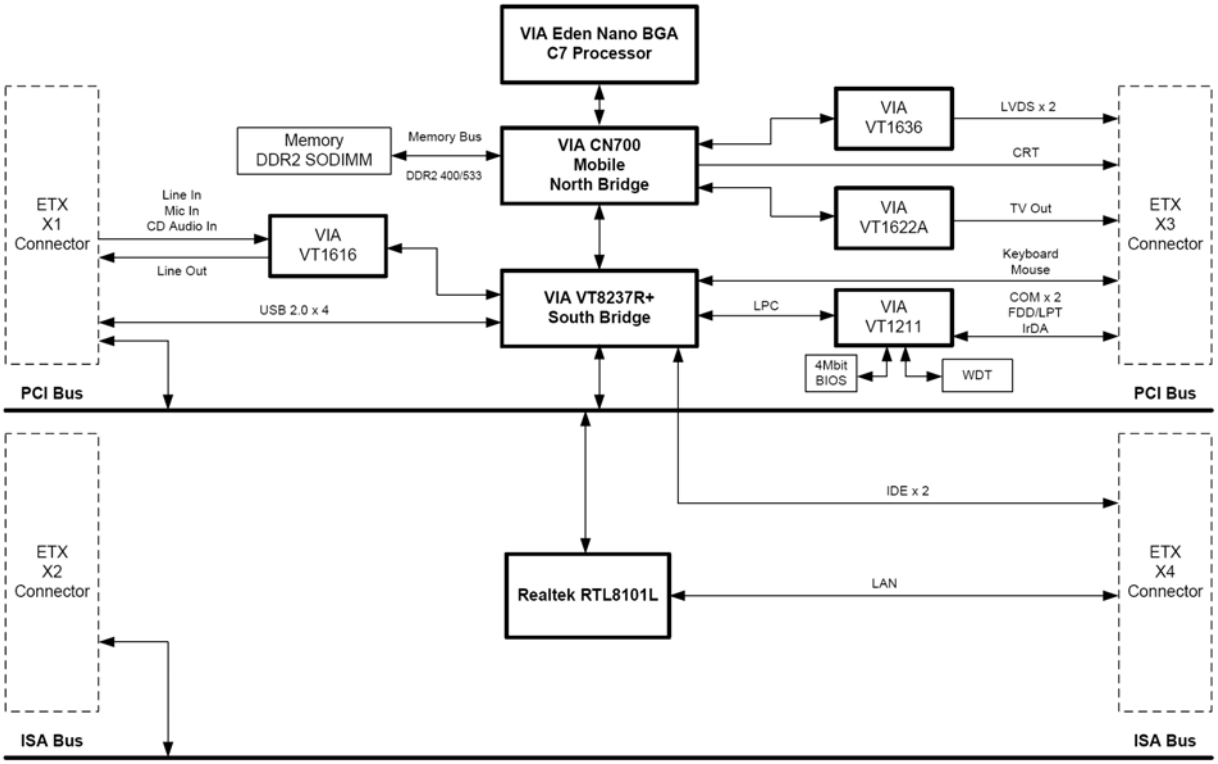
System	
CPU	Onboard VIA Eden V4 1 GHz
BIOS	Award 512 KB Flash BIOS
System Chipset	VIA CN700/VT8237R+
I/O Chip	VIA VT1211
System Memory	One 200-pin SODIMM socket supports up to 1 GB DDR2 400/533 SDRAM
Watchdog Timer	Reset: 1 sec.~255 min. and 1 sec. or 1 min./step
Expansion	Four PCI bus, ISA bus, SIRQ
I/O	
MIO	4 x EIDE (Ultra DMA 100), 2 x SATA II, 1 x FDD/LPT, 2 x TTL serial, 1 x K/B, 1 x Mouse
IrDA	115k bps, IrDA 1.0 compliant
USB	4 x USB 2.0 ports
Display	
Chipset	VIA ProSavage CN700 with integrated UniChrome Pro IGP Graphics Core supporting Chromotion CE Video Display engine & MPEG-2 decoder
Display Memory	16/32/64 MB frame buffer using system memory
Resolution	CRT mode: 1600 x 1200 @ 32 bpp (60 Hz) LCD/Simultaneous mode: 1600 x 1200 @ 16 bpp (60 Hz)
Dual Independent Display	CRT + LVDS, or TV out + LVDS, or CRT + TV out
VGA/LCD Interface	AGP 8x VGA/LCD interface
LVDS	Dual-channel 18/24-bit LVDS
TV-Out	VIA VT1622A TV encoder supports both NTSC/PAL Supports both S-video and composite video

Audio	
Chipset	VIA VT8237R+
AC97 Codec	VIA VT1616 supports 2 CH Audio
Audio Interface	Mic in, Line in, Line out
Ethernet	
Chipset	Realtek RTL8101L
Ethernet Interface	100Base-Tx Fast Ethernet compatible
Mechanical & Environmental	
Power Requirement	
Power Type	AT/ATX
Operation Temperature	0~60° C (32~140° F)
Operating Humidity	0%~90% relative humidity, non-condensing
Size (L x W)	4.5" x 3.7" (114 mm x 95 mm)
Weight	0.22 lbs (0.1 Kg)

1.6 Architecture Overview

1.6.1 Block Diagram

The following block diagram shows the architecture and main components of ESM-CN700.



The following sections provide detail information about the functions provided onboard.

1.6.2 VIA CN700 and VT8237R+

The CN700 supports 533 / 400 MHz FSB VIA C7 processor. The CN700 implements a deep In-Order Queue to improve system performance for multi-threaded software applications. DBI and V4 bus protocol are supported which effectively reduce overall system power consumption. The AGP controller is AGP v3.5 compliant with up to 2.1GB/second data transfer rate. It supports pseudo-synchronous AGP and CPU interface to maximize system performance. Deep read and write (256 bytes each) FIFO are integrated for optimal bus utilization and minimum data transfer latency.

The CN700 supports 64-bit memory data bus access and up to 2 double-sided DDR2 533 / 400 or DDR 400 / 333 / 266 SDRAM DIMMs for 2 GB maximum physical memory. The DDR DRAM interface allows zero wait-state data transfer bursting between the DRAM and memory controller's data buffers. The different banks of DRAM can be composed of an arbitrary mixture of 64 / 128 / 256 / 512 / 1024 Mb SDRAM in x 8 or x16 configurations. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus. The CN700 North Bridge interfaces to the South Bridge through a high speed (up to 533 MB/sec) 8x 66 MHz Data Transfer interconnect bus called V-Link interface. Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and V-Link operation. The combined CN700 North Bridge and VT8237R Plus South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master and CPU write-back merged with PCI post-write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction mechanism is also implemented for further improvement of overall system performance.

- System Power Management

For sophisticated power management, the CN700 supports dynamic CKE control to minimize DDR SDRAM power consumption during normal system state (S0). A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. The CN700 graphics controller implements dynamic clock gating for inactive functions to achieve maximum power saving. The system can be switched to standby or suspend states to further reduce power consumption when idle. VESA DPMS (Display Power Management Signaling) CRT power-down is supported. Coupled with the VT8237R Plus South Bridge chip, a complete power conscious PC main board can be implemented with no external glue logic.

- 3D Graphics Engine

Featuring an integrated 128-bit 3D graphics engine, the CN700 North Bridge utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, anisotropic filtering, and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides realistic user experiences in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

- 2D Graphics Engine

The CN700 North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths.

- MPEG Video Playback

The CN700 North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG playback, the integrated video accelerator offloads the CPU by performing the motion compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback

- LCD, DVI Monitor and TV Output Display Support

The CN700 provides three "Digital Video Port" interfaces: FPDP, GDVP1, and DVP0. The Flat Panel Display Port (FPDP) implements a 24-bit / dual 12-bit interface which is designed to drive a Flat Panel Display via an external LVDS transmitter chip (such as the VIA VT1622A). The CN700 can be connected to the external LVDS transmitter chip in either 24-bit or dual-12-bit modes. A wide variety of LCD panels are supported including VGA, SVGA, XGA, SXGA+ and up to UXGA-resolution TFT color panels, in either SDR (1 pixel / clock) or DDR (2 pixels / clock) modes. UXGA and higher resolutions require dual-edge data transfer (DDR) mode, which is supported by the VIA VT1631 LVDS transmitter chip. Two 12-bit "Display Port" interfaces are provided (through multiplexing with AGP interface) plus a dedicated 12-bit display port interface. Multiplexing display functions with the AGP bus allows embedded systems to support an external AGP connector for future performance upgrade through the external graphics controller. It also allows add-in cards to be designed with an AGP-compatible connector for implementing the display interface logic to reduce cost in the base (CRT-only) configuration. In the value system configurations, the external AGP upgrade capability is not normally required by the system, allowing all the AGP pins to be used for implementing very flexible display functions.

1.6.3 VIA VT1616 Audio Codec

Features

- AC'97 2.2 S/PDIF extension compliant codec
- 18-bit, 6 channel DAC outputs
- 1Hz resolution VSR on all channels
- Integrated IEC958 line driver for S/PDIF
- S/PDIF compressed digital or LPCM audio out
- Hardware downmixoption to 2 channels
- 3D stereo expansion for simulated surround
- 18-bit independent rate stereo ADC
- 4 stereo, 2 mono analog line-level inputs
- Second line-level output with volume control
- External Audio Amplifier Control
- Low Power consumption mode
- Exceeds MicrosoftR WHQL logo requirements
- 3.3V digital, 3.3 or 5V analog power supply
- 48-pin LQFP small footprint package

Description

VIA Technologies' VT1616 18-bit ∑Δ audio codec conforms to the AC'97 2.2 and S/PDIF Output specifications. The VT1616 integrates Sample Rate Converters on all channels and can be adjusted in 1Hz increments. There is a provision in hardware for down-mixing the 6 channels into stereo when only two end points are available. The analog mixer circuitry integrates a stereo enhancement to provide a pleasing 3D surround sound effect for stereo media. This codec is designed with aggressive power management to achieve low power consumption. When used with a 3.3V analog supply, power consumption is further reduced. The primary applications for this part are desktop and portable personal computers multimedia subsystems. However, it is suitable for any system requiring 6-channel audio output for home theater systems at competitive prices.

1.6.4 VIA VT1636 LVDS Transmitter

- Supports Single / Dual LVDS Transmitter Function
- Compatible with TIA/EIA-644 LVDS Standard
- Supports LVDS 18-bit and 24-bit Output
- Supports Dual Channel UXGA Panel Display
- Supports 2D Dither for 18-bit Panel
- Supports Option for 24-bit Color Mappings with Conventional (LSB) or Non-Conventional (MSB) Format Output
- Supports DVO Input Mode with 25 to 165 MHz Input Clock
- Programmable Input Clock and Strobe Select
- Narrow Bus Reduces Cable Size and Cost
- PLL Requires No External Components
- Two-Wire Serial Communication
- Panel Protection and Power Down Sequencing
- Panel Power Sequencing Control
- Supply Voltage 2.25 - 2.75V
- 64-pin LQFP Package (10x10x1.4 mm)

1.6.5 VIA VT1622A TV Encoder

The VT1622 and VT1622M are digital television encoders that accept various RGB pixel data formats or YCrCb (compatible with CCIR656 or CCIR601) pixel data format from a VGA controller or MPEG decoder. These two TV encoder chips can support any input resolution from 320x200 up to 1024x768 and will or will not perform non-interlace to interlace conversion to generate high quality flicker-free composite video, S-video, component interlaced or progressive scan output signals. Both VT1622 and VT1622M use the newest VIA ProScale® engine that provides the most advanced vertical and horizontal scaling technology. Using the programmable CRTC and the scaling factor, these two TV encoder chips can zoom an image in or out to any size. These two TV encoder chips use an adaptive deflicker filter that checks the graphics on a pixel-by-pixel basis to maintain a flicker-free display. The VT1622 and VT1622M can support various worldwide video standards, including NTSC-M (North America, Taiwan) NTSC-J (Japan), PAL-B, D, G, H, I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay) and PAL-Nc (Argentina). Because there are 4 DACs, these two TV encoder chips can simultaneously output composite video, S-video, component YCbCr, or RGB signals and output an analog progressive scan signal in YPbPr or RGB format. The VT1622M can output video with the Macrovision 7.1 anticopy video signal or the Macrovision 1.0 AGC copy protection with 525p progressive scan output. The Macrovision anticopy process provides a means to deter the unauthorized copying of copy protected analog video signals onto a videocassette. All features are software programmable through a serial bus interface that provides read/write access to all registers.

1.6.6 Ethernet

1.6.6.1 Realtek RTL8101L Ethernet Controller

The Realtek RTL8101L is a highly integrated and cost-effective single-chip Fast Ethernet controller. Featuring an MC'97 interface, the device is able to provide a combo-solution for LAN and software modem applications. It is equipped with a PCI and Boot ROM share interface (Realtek patent pending) for both EPROM and Flash Memory to provide maximum network security and ease of management.

The RTL8101L offers an ACPI (Advanced Configuration Power Interface) management function to provide efficient power management for advanced operating systems with OSPM (Operating System Directed Power Management). A remote wake-up function is also provided by support to Magic Packet, Link Change, and Wake-up Frame to increase cost-efficiency in network maintenance and management. In addition, it supports analog Auto Power-down and provides an auxiliary power auto-detect function to further save power.

1.6.7 VIA VT1211 LPC Super I/O

The VT1211 is a full function Super I/O chip that provides the most commonly used legacy Super I/O functionality plus the latest Hardware monitor initiatives. The device uses an LPC interface that complies with .LPC Interface Specification Revision 1.0.

The VT1211 contains a Floppy Disk Controller, an IEEE-1284 Parallel Port interface, two 16C550-UART-based serial port interfaces, a VFIR (Very Fast IR) Controller, a game port which supports 2 joysticks, a MIDI interface, and a 4M Flash-ROM interface. The integrated Hardware Monitor Controller controls the speed of 2 fans, monitors 2 fan tachometers, and has a Pentium II thermal diode and 5 Universal analog inputs for measuring voltage or temperature (by connecting external thermistors).

The VT1211 meets the "Microsoft PC98 & PC99 system design guide" requirements and is ACPI ready. The device requires a 48 MHz clock input and operates at 3.3V power supply.

The VT1211 consists of following logical devices. One high-performance 2.88MB floppy disk controller, with digital data separator, which supports one 360K / 720K / 1.2M / 1.44M / 2.88M floppy disk drive; One multi-mode high-performance parallel port featuring support for bi-directional Standard Parallel Port (SPP), Enhanced Parallel Port (EPP v1.7 and v1.9), and IEEE1284 compliant Extended Capabilities Port (ECP) protocols; Two 16C550 standard compatible enhanced UARTs perform asynchronous communication; One VFIR interface compliant with IrDA; One MIDI interface; One game port with built-in 558 and buffer chips to support direct connect of 2 joysticks; One Hardware Monitor; and Seven GPIO ports (56 GPIO pins).

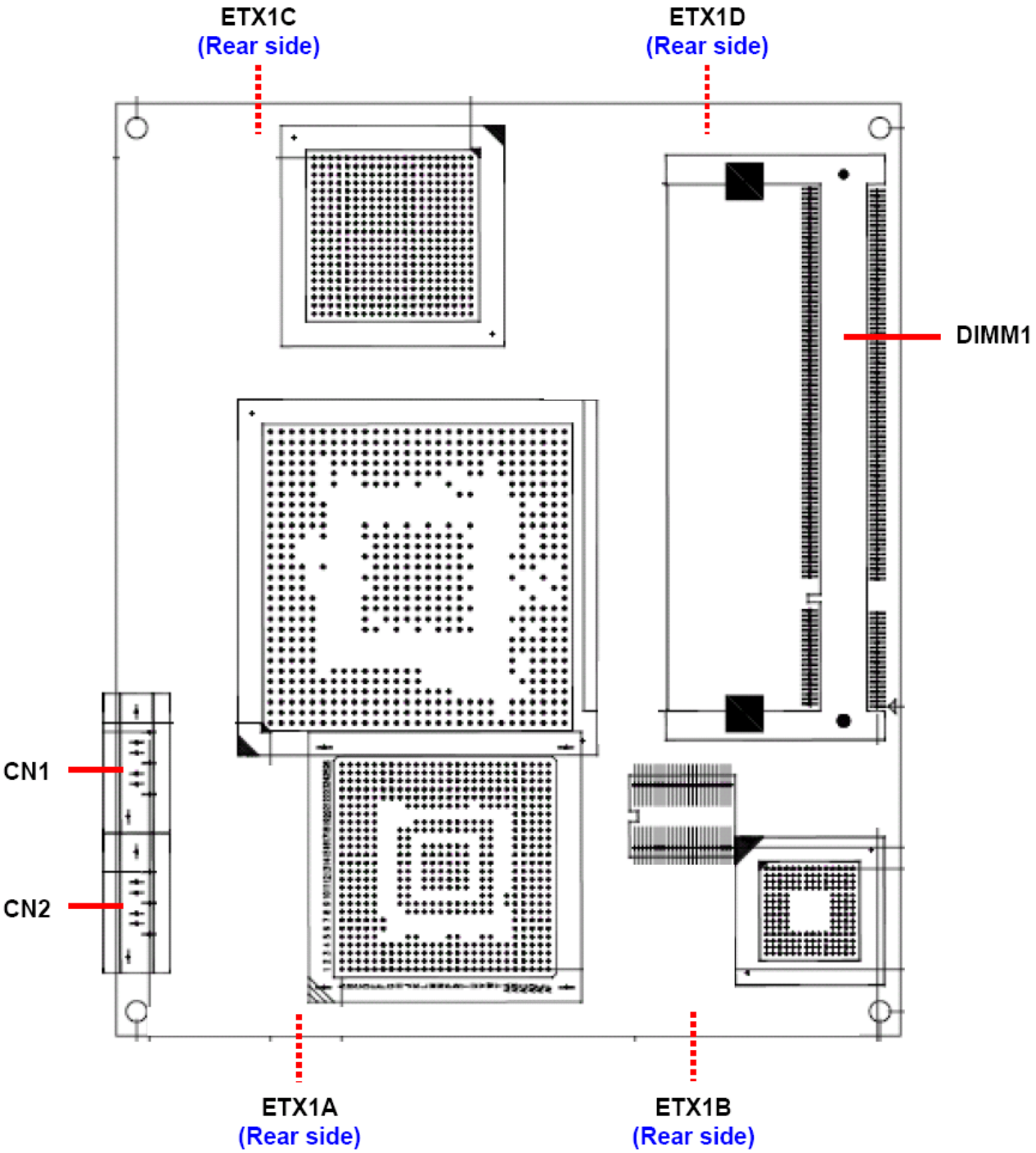
A hardware monitor engine is built in to monitor system health. An enhanced 8 bit ADC is built inside. This is exploited to simultaneously monitor 8 analog voltages or thermal inputs. The thermal inputs can be defined independently as thermistor or PentiumTM II thermal diode. Besides the ADC, the Hardware Monitor subsystem is also equipped with one chassis-open detection and 5 VID inputs for PentiumTM II Vcore identification.
All logical devices can be individually enabled or disabled via software configuration registers.

1.6.8 ITE IT8888G PCI to ISA Bridge

The IT8888G is a PCI to ISA bridge single function device. The IT8888G serves as a bridge between the PCI bus and ISA bus. The IT8888G's 32-bit PCI bus interface is compliant with PCI Specification V2.1 and supports both PCI Bus Master & Slave. The PCI interface supports both programmable positive and full subtractive decoding schemes.
The IT8888G also integrates two enhanced DMA Slave controllers for achieving PCI DMA cycles: PC/PCI DMA Slave Controller & Distributed DMA Slave Controllers.
The IT8888G also implements the optional fast positive decode of F, E, D, C memory segments. This special feature can provide a direct connection to an FALSH boot ROM.
The NOGO function, which is also implemented in the IT8888G for enabling or disabling subtractive decode of PCI interface, could be a software controlled output pin from other host controlled devices. The Serial IRQ is also implemented in the device for sending and receiving ISA IRQs & IOCHCK#. The device includes an ISA interface which supports full ISA compatible functions.
The IT8888G is available in 160-pin TFBGA package.

2. Hardware Configuration

2.1 Product Overview



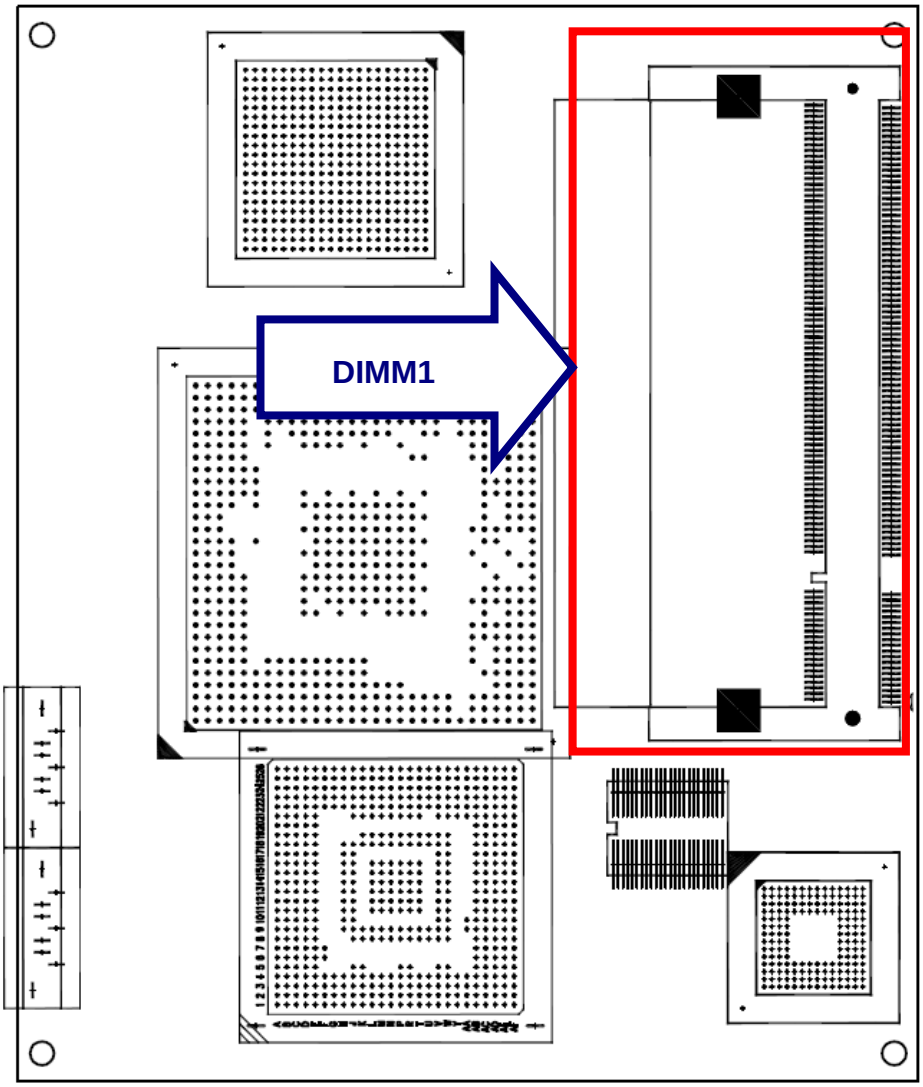
2.2 Installation Procedure

This chapter explains you the instructions of how to setup your system.

1. Turn off the power supply.
2. Insert the DIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the ATXPWR.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the "LOAD BIOS DEFAULTS" feature. The ***Integrated Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilized, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

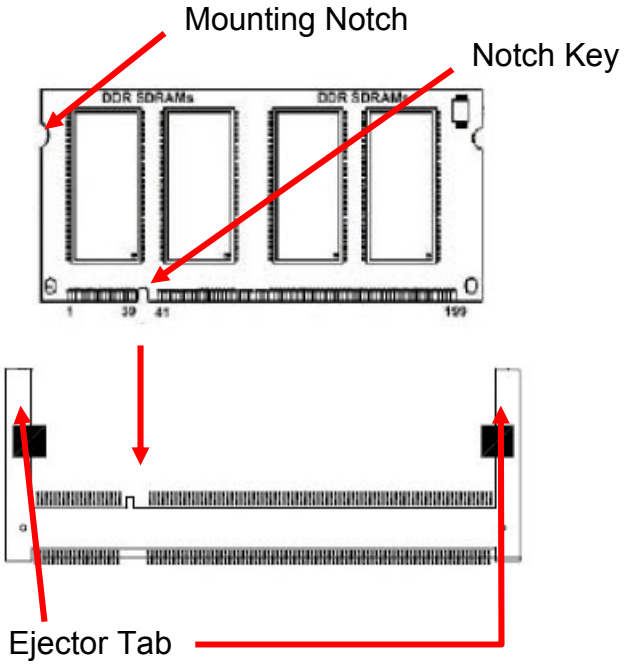
2.1.1 Main Memory

ESM-CN700 provides one 200-pin SODIMM sockets to support DDR2 SDRAM. The total maximum memory size is 1GB.



Make sure to unplug the power supply before adding or removing SODIMMs or other system components. Failure to do so may cause severe damage to both the board and the components.

- Locate the DIMM socket on the board.
- Hold two edges of the DIMM module carefully. Keep away of touching its connectors.
- Align the notch key on the module with the rib on the slot.
- Firmly press the modules into the socket automatically snaps into the mounting notch. Do not force the DIMM module in with extra force as the DIMM module only fit in one direction.



200-pin SODIMM

- To remove the DIMM modules, push the two ejector tabs on the slot outward simultaneously, and then pull out the DIMM module.

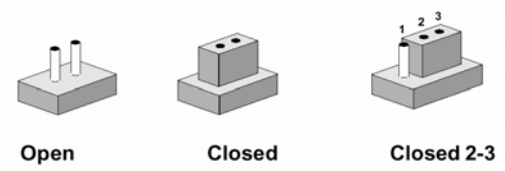
Note: (1) Please do not change any DDR SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.

(2) Static electricity can damage the electronic components of the computer or optional boards. Before starting these procedures, ensure that you are discharged of static electricity by touching a grounded metal object briefly.

2.3 Jumper and Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:

A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

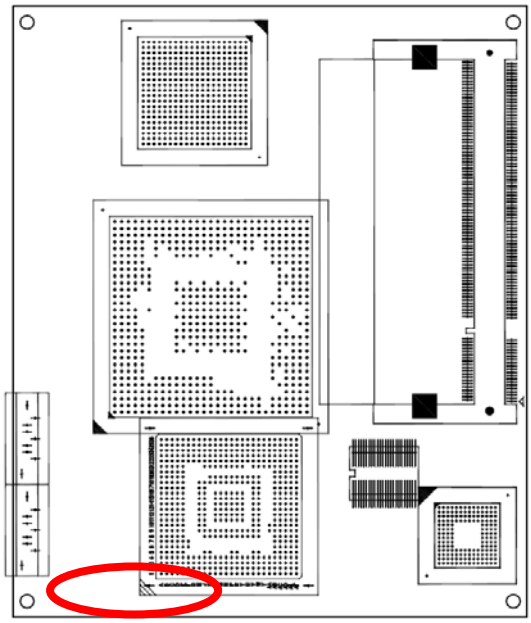
The following tables list the function of each of the board's jumpers and connectors.

Connectors

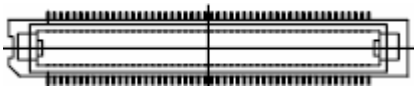
Label	Function	Note
CN1	Serial ATA connector 2	
CN2	Serial ATA connector 1	
DIMM1	200-pin DDR2 SODIMM socket	
ETX1A	ETX connector X1	HIROSE FX8-100P-SV
ETX1B	ETX connector X2	HIROSE FX8-100P-SV
ETX1C	ETX connector X3	HIROSE FX8-100P-SV
ETX1D	ETX connector X4	HIROSE FX8-100P-SV

2.4 Setting Jumpers & Connectors

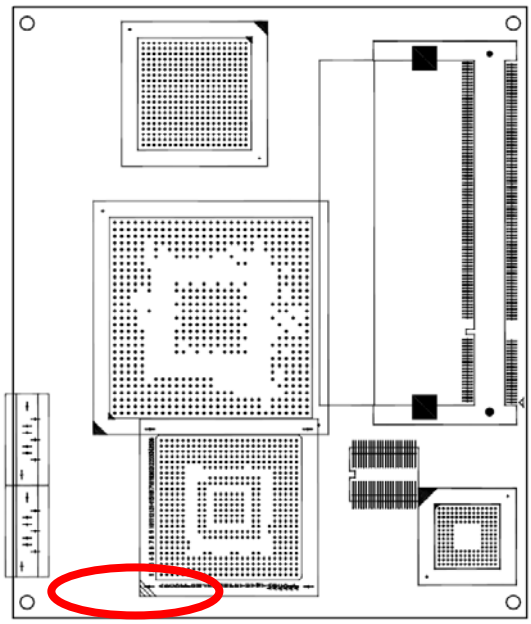
2.4.1 Pin Definition – ETX Connecter X1 (ETX1A)



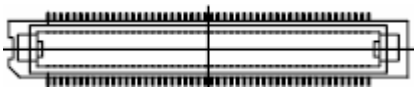
(Rear side)



Signal	PIN	PIN	Signal
GND	1	2	GND
PCICLK3	3	4	PCICLK4
GND	5	6	GND
PCICLK1	7	8	PCICLK2
REQ3#	9	10	GNT3#
GNT2#	11	12	+3.3V
REQ2#	13	14	GTN1#
REQ1#	15	16	+3.3V
GNT0#	17	18	NC
+5V	19	20	+5V
SERIRQ	21	22	REQ0#
AD0	23	24	+3.3V
AD1	25	26	AD2
AD4	27	28	AD3
AD6	29	30	AD5
CBE0#	31	32	AD7
AD8	33	34	AD9
GND	35	36	GND
AD10	37	38	AUXAL
AD11	39	40	MIC
AD12	41	42	AUXAR
AD13	43	44	ASVCC
AD14	45	46	SNDL
AD15	47	48	ASGND
CBE1#	49	50	SNDR



(Rear side)



Signal	PIN	PIN	Signal
+5V	51	52	+5V
PAR	53	54	SERR#
GPERR#	55	56	NC
PME#	57	58	USB2#
LOCK#	59	60	DEVSEL#
TRDY#	61	62	USB3-
IRDY#	63	64	STOP#
FRAME#	65	66	USB2
GND	67	68	GND
AD16	69	70	CBE2#
AD17	71	72	USB3
AD19	73	74	AD18
AD20	75	76	USB0#
AD22	77	78	AD21
AD23	79	80	USB1#
AD24	81	82	CBE3#
+5V	83	84	+5V
AD25	85	86	AD26
AD28	87	88	USB0
AD27	89	90	AD29
AD30	91	92	USB1
PCIRST#	93	94	AD31
INTC#	95	96	INTD#
INTA#	97	98	INTB#
GND	99	100	GND

2.4.2 Signal Description – ETX Connector X1 (ETX1A)

2.4.2.1 PCI Signals

Signal	Signal Description
PCICLK [1:4]	PCI clock outputs for up to 4 external PCI slots or devices. The baseboard designer should route these clocks for 1300pS total delay from the ETX connector pin to the clock pin of the PCI device. See the ETX Design Guide for typical route length calculations.
REQ [0:3]#	Bus Request signals for up to 4 external bus mastering PCI devices. When asserted, a PCI device is requesting PCI bus ownership from the arbiter.
GNT [0:3]#	Grant signals to PCI Masters. When asserted by the arbiter, the PCI master has been granted ownership of the PCI bus.
AD [0:31]	PCI Address and Data Bus Lines. These lines carry the address and data information for PCI transactions.
CBE [0:3]#	PCI Bus Command and Byte Enables. Bus command and byte enables are multiplexed in these lines for address and data phases, respectively.
PAR	Parity bit for the PCI bus. Generated as even parity across AD [31:0] and CBE [3:0]#.
SERIRQ	Serial interrupt request. This pin is used to support the serial interrupt protocol.
SERR#	System Error. Asserted for hardware error conditions such as parity errors detected in DRAM.
GPERR#	Parity Error. For PCI operation per exception granted by PCI 2.1 Specification.
PME#	Power management event.
LOCK#	Lock Resource Signal. This pin indicates that either the PCI master or the bridge intends to run exclusive transfers.
DEVSEL#	Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.
TRDY#	Target Ready. This pin indicates that the target is ready to complete the current data phase of a transaction.
IRDY#	Initiator Ready. This signal indicates that the initiator is ready to complete the current data phase of a transaction.
STOP#	Stop. This signal indicates that the target is requesting that the master stop the current transaction.
FRAME#	Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. The access will be either an output driven by the Northbridge on behalf of the CPU, or an input during PCI master access.

Signal	Signal Description
PCIRST#	PCI Bus Reset. This is an output signal to reset the entire PCI Bus. This signal is asserted during system reset.
INTA#, INTB#, INTC#, INTD#	PCI interrupts. These interrupts are sharable and are typically wired in rotation to PCI slots or devices.
IDSEL	This pin is not present on the ESM-2646 module connector, but it is present on each PCI slot connector or device. IDSEL is an input to the device that is used to set the device's configuration address for PCI configuration cycles. The IDSEL pin of each device is typically connected to one of the AD lines in order to set a unique configuration address. In ETX systems, the four external bus slots or devices are assumed to use AD[19:22] for IDSEL connections.

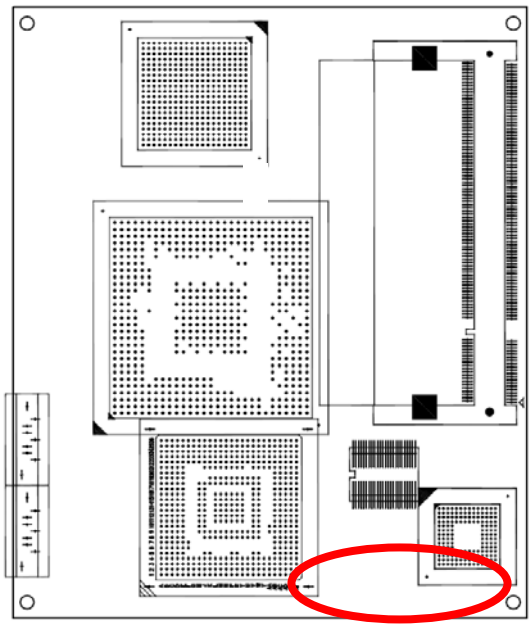
2.4.2.2 USB Signals

Signal	Signal Description
USB [0:3]	Universal Serial Bus Port [0:3] positive signal. These are the serial data pairs for USB Port N-and Port N#.
USB [0:3]#	Universal Serial Bus Port [0:3] negative signal. These are the serial data pairs for USB Port N-and Port N#.

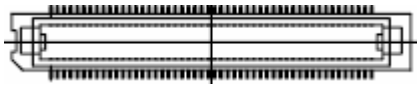
2.4.2.3 Audio Signals

Signal	Signal Description
SNDL/ SNDR	Line-level stereo output left/ right. These outputs have a nominal level of 1 volt RMS into a 10K impedance load. These outputs cannot drive low-impedance speakers directly.
AUXAL/ AUXAR	Auxiliary A input left/ right. Normally intended for connection to an internal or external CDROM analog output or a similar line-level audio source. Minimum input impedance is 5KOhm. Nominal input level is 1 volt RMS.
MIC	Microphone input. Minimum input impedance is 5KOhm, max. Input voltage is 0.15 Vp-p.
ASGND	Analog ground for sound controller. Use this signal ground for an external amplifier in order to achieve lowest audio noise levels.
ASVCC	Analog supply voltage for sound controller. This is an output which is used for production test only. Do not make external connections to this pin.

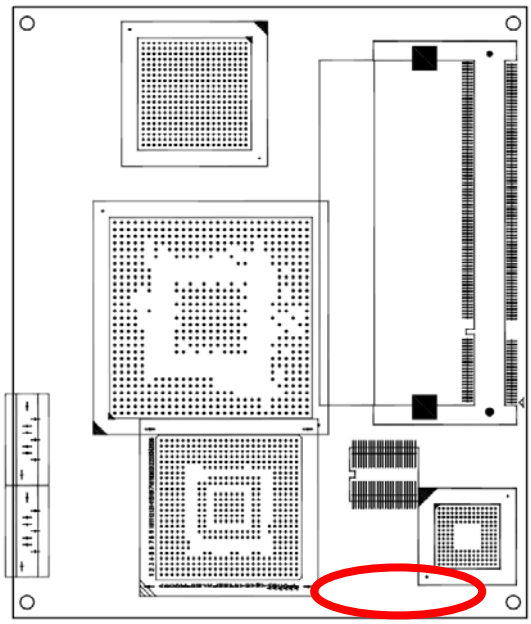
2.4.3 ETX Connector X2 (ETX1B)



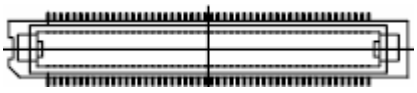
(Rear side)



Signal	PIN	PIN	Signal
GND	1	2	GND
SD14	3	4	SD15
SD13	5	6	MASTER#
SD12	7	8	DREQ7
SD11	9	10	DACK7#
SD10	11	12	DREQ6
SD9	13	14	DACK6#
SD8	15	16	DREQ5
MEMW#	17	18	DACK5#
MEMR#	19	20	DREQ0
LA17	21	22	DACK0#
LA18	23	24	IRQ14
LA19	25	26	IRQ15
LA20	27	28	IRQ12
LA21	29	30	IRQ11
LA22	31	32	IRQ10
LA23	33	34	IO16#
GND	35	36	GND
SBHE#	37	38	M16#
SA0	39	40	OSC
SA1	41	42	BALE
SA2	43	44	TC
SA3	45	46	DACK2#
SA4	47	48	IRQ3
SA5	49	50	IRQ4



(Rear side)



Signal	PIN	PIN	Signal
+5V	51	52	+5V
SA6	53	54	IRQ5
SA7	55	56	IRQ6
SA8	57	58	IRQ7
SA9	59	60	SYSCLK
SA10	61	62	REFSH#
SA11	63	64	DREQ1
SA12	65	66	DACK1#
GND	67	68	GND
SA13	69	70	DREQ3
SA14	71	72	DACK3#
SA15	73	74	IOR#
SA16	75	76	IOW#
SA18	77	78	SA17
SA19	79	80	SMEMR#
IOCHRDY	81	82	AEN
+5V	83	84	+5V
SD0	85	86	SMEMW#
SD2	87	88	SD1
SD3	89	90	NOWS#
DREQ2	91	92	SD4
SD5	93	94	IRQ9
SD6	95	96	SD7
IOCHK#	97	98	RSTDRV
GND	99	100	GND

2.4.4 Signal Description – ETX Connector X2 (ETX1B)

2.4.4.1 ISA Signals

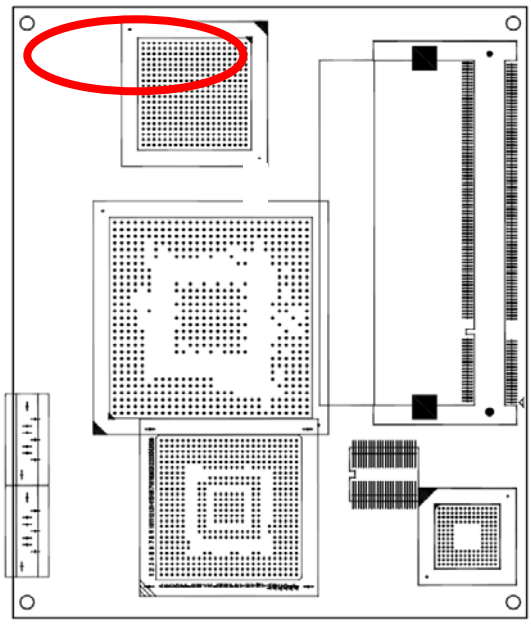
Signal	Signal Description
SD[0:15]	These signals provide data bus bits 0 to 15 for any peripheral devices. All 8-bit devices use SD[0:7] for data transfers. 16-bit devices use SD[0:15]. To support 8-bit devices, the data on SD[8:15] is gated to SD[0:7] during 8-bit transfers to these devices. 16-bit CPU cycles will be automatically converted into two 8-bit cycles for 8-bit peripherals.
SA[0:19]	Address bits 0 through 15 are used to address I/O devices. Address bits 0 through 19 are used to address memory within the system. These 20 address lines, in addition to LA[17:23] allow access of up to 16MB of memory. SA[0:19] are gated on the ISA-bus when BALE is high and latched on to the falling edge of BALE.
SBHE#	*Bus High Enable* indicates a data transfer on the upper byte of the data bus SD[8:15]. 16-bit I/O devices use SBHE# to enable data bus buffers on SD[8:15].
BALE	BALE is an active-high pulse generated at the beginning of any bus cycle initiated by a CPU module. It indicates when the SA[0:19], LA17.23, AEN, and SBHE# signals are valid.
AEN	AEN is an active-high output that indicates a DMA transfer cycle. Only resources with a active DACK# signal should respond to the command lines when AEN is high.
MEMR#	MEMR# instructs memory devices to drive data onto the data bus. MEMR# is active for all memory read cycles.
SMEMR#	SMEMR# instructs memory devices to drive data onto the data bus. SMEMR# is active for memory read cycles to addresses below 1MB.
MEMW#	MEMW# instructs memory devices to store the data present on the data bus. MEMW# is active for all memory write cycles.
SMEMW#	SMEMW# instructs memory devices to store the data present on the data bus. SMEMW# is active for all memory write cycles to address below 1MB.
IOR#	I/O read instructs an I/O device to drive its data onto the data bus. It may be driven by the CPU or by the DMA controller. IOR# is inactive (high) during refresh cycles.

Signal	Signal Description
IOW#	I/O write instructs an I/O device to store the data present on the data bus. It may be driven by the CPU or by the DMA controller. IOW# is inactive (high) during refresh cycles.
IOCHK#	IOCHK# is an active-low input signal that indicates that an error has occurred on the module bus. If I/O checking is enabled on the CPU module, an IOCHK# assertion by a peripheral device sends a NMI to the processor.
IOCHRDY	The I/O Channel Ready is pulled low in order to extend the read or write cycles of any bus access when required. The CPU, DMA controllers or refresh controller can initiate the cycle. Any peripheral that cannot present read data or strobe in write data within this amount of time use IOCHRDY to extend these cycles. This signal should not be held low for more than 2.5 µs for normal operation. Any extension to more than 2.5 µs does not guarantee proper DRAM memory content due to the fact that memory refresh is disabled while IOCHRDY is low.
M16#	The M16# signal determines when a 16-bit to 8-bit conversion is needed for memory bus cycles. A conversion is done any time the CPU module requests a 16-bit memory cycle while the M16# line is high. If M16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If M16# is low, an access to peripherals is done 16 bits wide.
IO16#	The IO16# signal determines when a 16-bit to 8-bit conversion is needed for I/O bus cycles. A conversion is done any time the CPU module requests a 16-bit I/O cycle while the IO16# line is high. If IO16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If IO16# is low, an access to peripherals is done at 16 bit width.
REFSH#	REFSH# is pulled low whenever a refresh cycle is initiated. A refresh cycle is activated every 15.6 us in order to prevent loss of DRAM data.

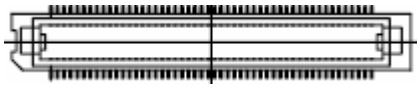
Signal	Signal Description
NOWS#	The Zero wait state signal tells the CPU to complete the current bus cycle without inserting the default wait states. By default the CPU inserts 4 wait states for 8-bit transfers and 1 wait state for 16-bit transfers.
MASTER#	This signal is used with a DRQ line to gain control of the system bus. A processor or a DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DACK#. Upon receiving the DACK#, a bus master may pull MASTER# low, which will allow it to control the system address, data and control lines. After MASTER# is low, the bus master must wait one system clock period before driving the address and data lines, and two clock periods before issuing a read or write command. If this signal is held low for more than 15 us, system memory may be lost as memory refresh is disabled during this process.
SYSCLK	SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with a duty cycle of 40-60 percent. The frequency supplied by different CPU modules may vary. This signal is supplied at all times except when the CPU module is in sleep mode.
OSC	OSC is supplied by the CPU module. It has a nominal frequency of 14.31818 MHz and a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.
RESETDRV	This active-high output is system reset generated from CPU modules. It is responsible for resetting external devices.
DREQ [0, 1, 2, 3, 5, 6, 7]	The asynchronous DMA request inputs are used by external devices to indicate when they need service from the CPU modules DAM controllers. DREQ0..3 are used for transfers between 8-bit I/O adapters and system memory. DREQ5..7 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pull-up resistors on the CPU modules.
DACK [0, 1, 2, 3, 5, 6, 7]#	DMA acknowledge 0..3 and 5.7 are used to acknowledge DMA requests. They are active-low.

Signal	Signal Description
TC	The active-high output TC indicates that one of the DMA channels has transferred all data.
IRQ [3:7, 9, 15]	These are the asynchronous interrupt request lines. IRQ0, 1, 2 and 8 are not available as external interrupts because they are used internally on the CPU module. All IRQ signals are active-high. The interrupt requests are prioritized. IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest). IRQ3 through IRQ7 have the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt service routine).

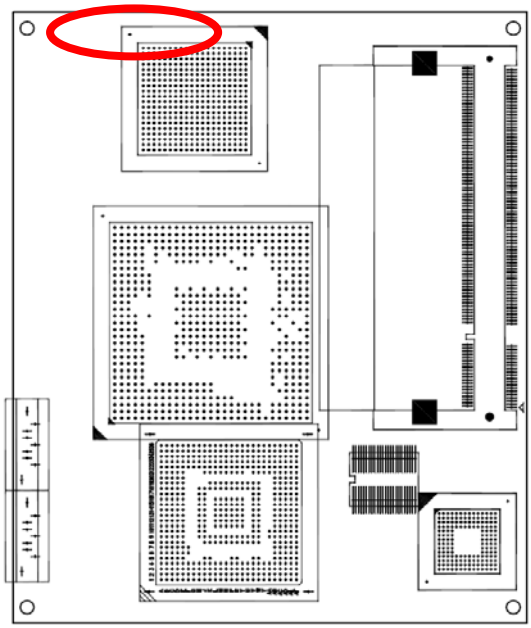
2.4.5 ETX Connector X3 (ETX1C)



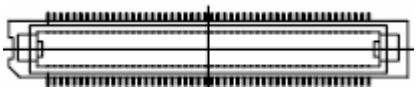
(Rear side)



Signal	PIN	PIN	Signal
GND	1	2	GND
R	3	4	B
HSY	5	6	G
VSY	7	8	DDCK
NC	9	10	DDDA
E_Txclk#	11	12	E_Txout3#
E_Txclk	13	14	E_Txout3
GND	15	16	GND
E_Txout1	17	18	E_Txout2
E_Txout1#	19	20	E_Txout2#
GND	21	22	GND
Txout3#	23	24	E_Txout0
Txout3	25	26	E_Txout0#
GND	27	28	GND
Txout2#	29	30	Txclk
Txout2	31	32	Txclk#
GND	33	34	GND
Txout0	35	36	Txout1
Txout0#	37	38	Txout1#
+5V	39	40	+5V
I^2C_DAT	41	42	NC
I^2C _CLK	43	44	ENBKL#
BIASON	45	46	DIGON
SYNC	47	48	Y
NC	49	50	C



(Rear side)



Signal	PIN	PIN	Signal
NC	51	52	NC
+5V	53	54	GND
STB#	55	56	AFD#
NC	57	58	PD7
IRRX	59	60	ERR#
IRTX	61	62	PD6
RXD2	63	64	INIT#
GND	65	66	GND
RTS2#	67	68	PD5
DTR2#	69	70	SLIN#
DCD2#	71	72	PD4
DSR2#	73	74	PD3
CTS2#	75	76	PD2
TXD2#	77	78	PD1
RI2#	79	80	PD0
+5V	81	82	+5V
RXD1	83	84	ACK#
RTS1#	85	86	BUSY#
DTR1#	87	88	PE
DCD1#	89	90	SLCT#
DSR1#	91	92	MSCLK
CTS1#	93	94	MSDAT
TXD1	95	96	KBCLK
RI1#	97	98	KBDAT
GND	99	100	GND

2.4.6 Signal Description – ETX Connector X3 (ETX1C)

2.4.6.1 VGA Signals

Signal	Signal Description
HSY	Horizontal Sync: This output supplies the horizontal synchronization pulse to the CRT monitor.
VSY	Vertical Sync: This output supplies the vertical synchronization pulse to the CRT monitor.
R, G, B	Red, green and blue analog video output signals for CRT monitors. These lines should be terminated with 75 ohms to ground at the video connector.
DDCK, DDDA	These two pins can be used for a DDC interface between the graphics controller chip and the CRT monitor.

2.4.6.2 LVDS Flat Panel Interface Signals

Signal	Signal Description
BIASON	**Controls panel contrast voltage.**
DIGON	**Controls panel digital power.**
ENBKL#	**Controls backlight power enable.**

2.4.6.3 Serial Port Signals

Signal	Signal Description
DTR1#, DTR2#	Active-low data terminal ready outputs for the serial port. Handshake output signal notifies the modem that the UART is ready to establish a data communication link.
RI1#, RI2#	Active-low input is for the serial port. Handshake signals notify the UART when a telephone ring signal is detected by the modem.
TXD1, TXD2	Transmitter serial data output from serial port.
RXD1, RXD2	Receiver serial data input.
CTS1#, CTS2#	Active-low input for serial ports. Handshake signals notify the UART when the modem is ready to receive data.
RTS1#, RTS2#	Active-low output for serial port. Handshake signals notify the modem when the UART is ready to transmit data.
DCD1#, DCD2#	Active-low input for serial port. Handshake signals notify the UART when a carrier signal is detected by the modem.
DSR1#, DSR2#	This active-low input is for serial port. Handshake signals are use to notify the UART that the modem is ready to establish the communication link.

2.4.6.4 PS/2 Keyboard & Mouse Signals

Signal	Signal Description
KBDAT	Bi-directional keyboard data signal.
KBCLK	Keyboard clock signal.
MSDAT	Bi-directional mouse data signal.
MSCLK	Mouse clock signal.

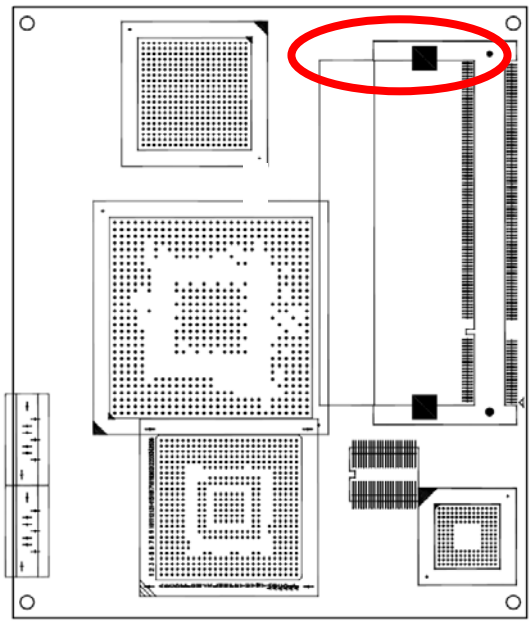
2.4.6.5 IrDA (SIR) Signals

Signal	Signal Description
IRTX, IRRX	Infrared transmit and receive pins.

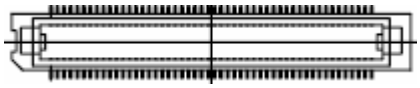
2.4.6.6 Parallel Port Signals

Signal	Signal Description
LPT/FLPY#	This ETX input signal selects whether the parallel port pins will implement parallel port or floppy support functionality. There is an internal pull-up on this signal. If this signal is high or unconnected, the following parallel port pin functions are in effect:
STB#	This active-low signal is used to strobe the printer data into the printer.
AFD#	This active-low output tells the printer to automatically feed the next single line after each preceding line has been printed.
PD[0:7]	This bi-directional parallel data bus is used to transfer information between the CPU and the peripherals.
ERR#	This active-low signal indicates an error situation has occurred at the printer.
INIT#	This active-low signal is used to initiate the printer when low.
SLIN#	This active-low signal selects the printer.
ACK#	This active-low output from the printer indicates that it has received the previous data and that it is ready to receive new data.

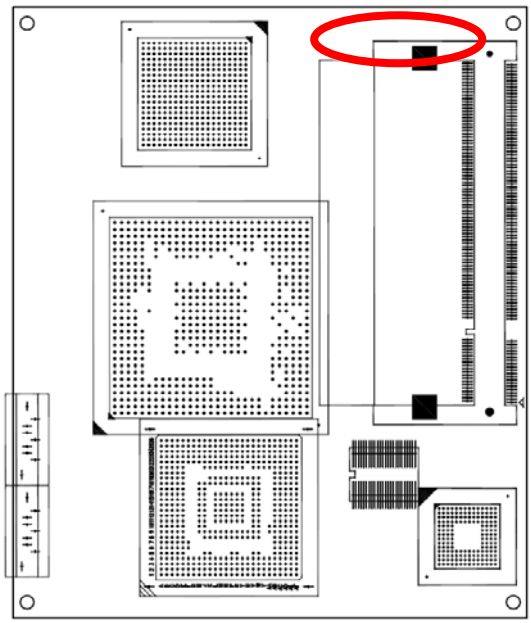
2.4.7 ETX Connector X4 (ETX1D)



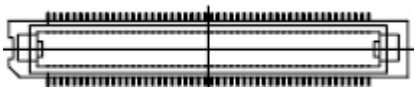
(Rear side)



Signal	PIN	PIN	Signal
GND	1	2	GND
5V_SB	3	4	PWGIN
PS_ON	5	6	SPEAKER
PWRBTN#	7	8	BATT
KBINH	9	10	LILED
RSMRST#	11	12	ACTLED
NC	13	14	SPEEDLED
NC	15	16	I2CLK
+5V	17	18	+5V
OVCR#	19	20	INC
EXTSMI#	21	22	I2DAT
SMBCLK	23	24	SMBDATA
SIDE_CS3#	25	26	SMBALRT#
SIDE_CS1#	27	28	NCDASP_S
SIDE_A2	29	30	PIDE_CS3#
SIDE_A0	31	32	PIDE_CS1#
GND	33	34	GND
PDIAG_S	35	36	PIDE_A2
SIDE_A1	37	38	PIDE_A0
SIDE_INTRQ	39	40	PIDE_A1
NC	41	42	NC
SIDE_AK#	43	44	PIDE_INTRQ
SIDE_RDY	45	46	PIDE_AK#
SIDE_IOR#	47	48	PIDE_RDY
+5V	49	50	+5V



(Rear side)



Signal	PIN	PIN	Signal
SIDE_IOW#	51	52	PIDE_IOR#
SIDE_DRQ	53	54	PIDE_IOW#
SIDE_D15	55	56	PIDE_DRQ
SIDE_D0	57	58	PIDE_D15
SIDE_D14	59	60	P IDE_D0
SIDE_D1	61	62	PIDE_D14
SIDE_D13	63	64	PIDE_D1
GND	65	66	GND
SIDE_D2	67	68	PIDE_D13
SID E_D12	69	70	PIDE_D2
SIDE_D3	71	72	PIDE_D12
SIDE_D11	73	74	PIDE_D3
SIDE_D4	75	76	PIDE_D11
SIDE_D10	77	78	PIDE_D4
SIDE_D5	79	80	PIDE_D10
+5V	81	82	+5V
SIDE_D9	83	84	PIDE_D5
SIDE_D6	85	86	PIDE_D9
SIDE_D8	87	88	PIDE_D6
GPE2#	89	90	NC
RXD#	91	92	PIDE_D8
RXD	93	94	SIDE_D7
TXD#	95	96	PIDE_D7
TXD	97	98	HDRST#
GND	99	100	GND

2.4.8 Signal Description – ETX Connector X4 (ETX1D)

2.4.8.1 IDE Signals

Signal	Signal Description
PIDE_D[0:15]/ SIDE_D[0:15]	IDE Data Bus.
PIDE_A[0:2]/ SIDE_A[0:2]	IDE Address Bus.
PIDE_CS1#/ SIDE_CS1#	IDE Chip Select 1. This is the Chip Select 1 command output pin that enables the IDE device to watch the Read/Write Command.
PIDE_CS3#/ SIDE_CS3#	IDE Chip Select 3. This is the Chip Select 3 command output pin that enables the IDE device to watch the Read/Write Command.
PIDE_DRQ/ SIDE_DRQ	IDE DMA Request for IDE Master. This signal is asserted by an IDE device. It will be active-high in DMA or Ultra-33 mode and always be inactive-low in PIO mode.
PIDED_AK#/ SIDED_AK#	IDE DACK# for IDE Master. This signal grants the IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.
PIDE_RDY/ SIDE_RDY	IDE Ready. This is the input pin from the IDE Channel. It indicates that the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions.
PIDE_IOR#/ SIDE_IOR#	IDE IOR# Command. This is the IOR# command output pin used to tell the IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.
PIDE_IOW#/ SIDE_IOW#	IDE IOW# Command. This is the IOW# command output pin used to notify the IDE device that the available Write Data is already asserted by the IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.
PIDE_INTRQ/ SIDE_INTRQ	Interrupt request signal from the IDE device.
HDRST#	Low-active hardware reset (RSTDRV inverted).

2.4.8.2 Ethernet Signals

Signal	Signal Description
TXD#, TXD	Ethernet Transmit Differential Pair. These pins transmit the serial bit stream on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.
RXD#, RXD	Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer. The bit stream can be transmitted in either two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.
ACTLED	The Activity LED pin indicates either transmitted or received data activity on the Ethernet port. This pin is asserted low when activity is detected. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.
LILED	The Link Integrity LED pin indicates link integrity. This pin is asserted low when the link is valid. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.
SPEEDLED	The Speed LED pin indicates high speed operation. This LED is not supported by all ETX boards. This pin is asserted low when a 100Mbps link is detected, and is not asserted for a 10Mbps link. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.

2.4.8.3 Power Management Signals

Signal	Signal Description
RSMRST#	*Resume Reset input*. This input may be driven low by external circuitry in order to reset the power management logic on the ETX module.
EXTSMI	System management interrupt input. May be driven low by external circuitry to initiate an SMI.

3 BIOS Setup

Note: Installation procedures and screen shots in this section are for your reference and may not be exactly the same as shown on your screen.

3.1 Starting Setup

The AwardBIOS™ is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing <Del> immediately after switching the system on, or

By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

Press F1 to Continue, DEL to enter SETUP

3.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Button	Description
↑	Move to previous item
↓	Move to next item
←	Move to the item in the left hand
→	Move to the item in the right hand
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

- **Navigating Through The Menu Bar**

  Use the left and right arrow keys to choose the menu you want to be in.

Note: Some of the navigation keys differ from one screen to another.

- **To Display a Sub Menu**
  Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A "➢" pointer marks all sub menus.

3.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

3.4 In Case of Problems

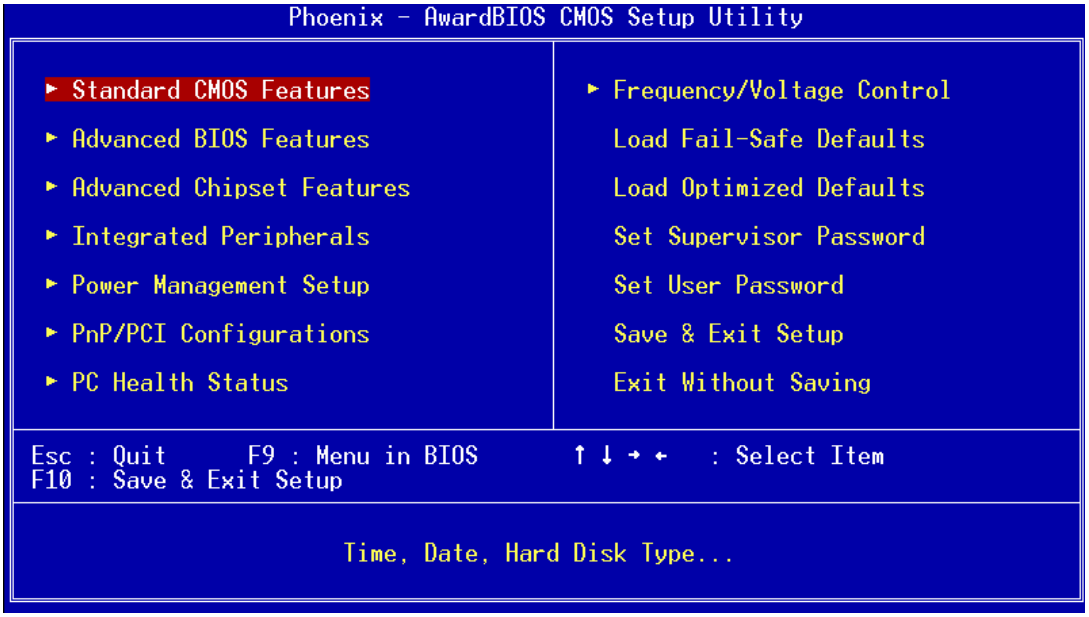
If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

3.5 Main Menu

Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

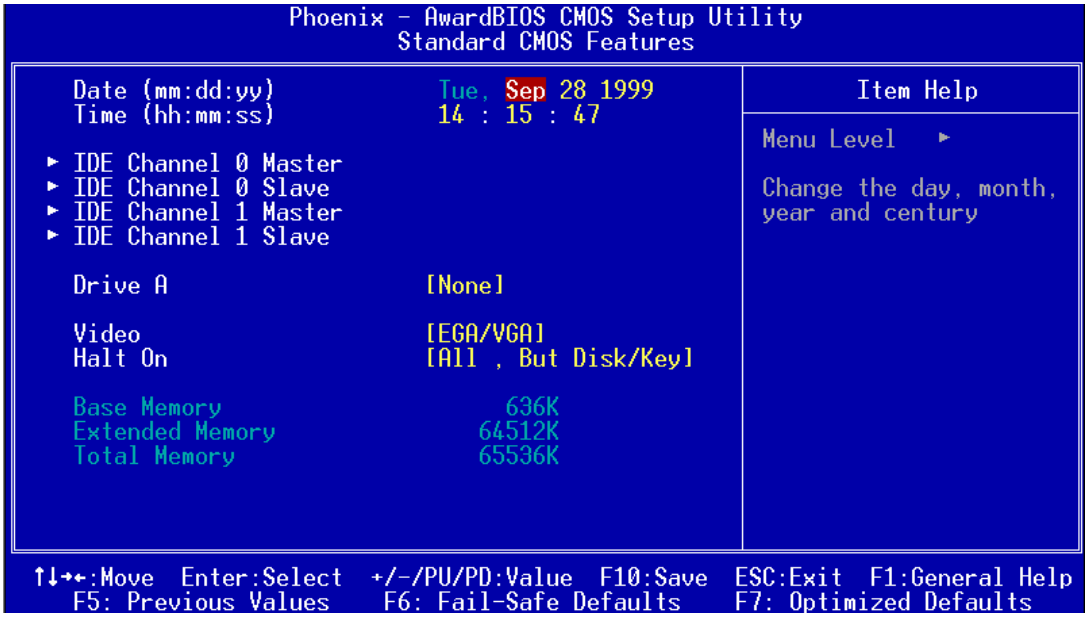
Note that a brief description of each highlighted selection appears at the bottom of the screen.



Note: The BIOS setup screens shown in this chapter are for reference purposes only, and may not exactly match what you see on your screen.
Visit the Evalue website (www.evalue-tech.com) to download the latest product and BIOS information.

3.5.1 Standard CMOS Features

The items in Standard CMOS Setup Menu are divided into few categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.



3.5.1.1 Main Menu Selection

This table shows the selections that you can make on the Main Menu.

Item	Options	Description
Date	MM DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
IDE Channel 0 Master IDE Channel 0 Slave IDE Channel 1 Master IDE Channel 1 Slave	Options are in its sub menu	Press <Enter> to enter the sub menu of detailed options
Drive A	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you

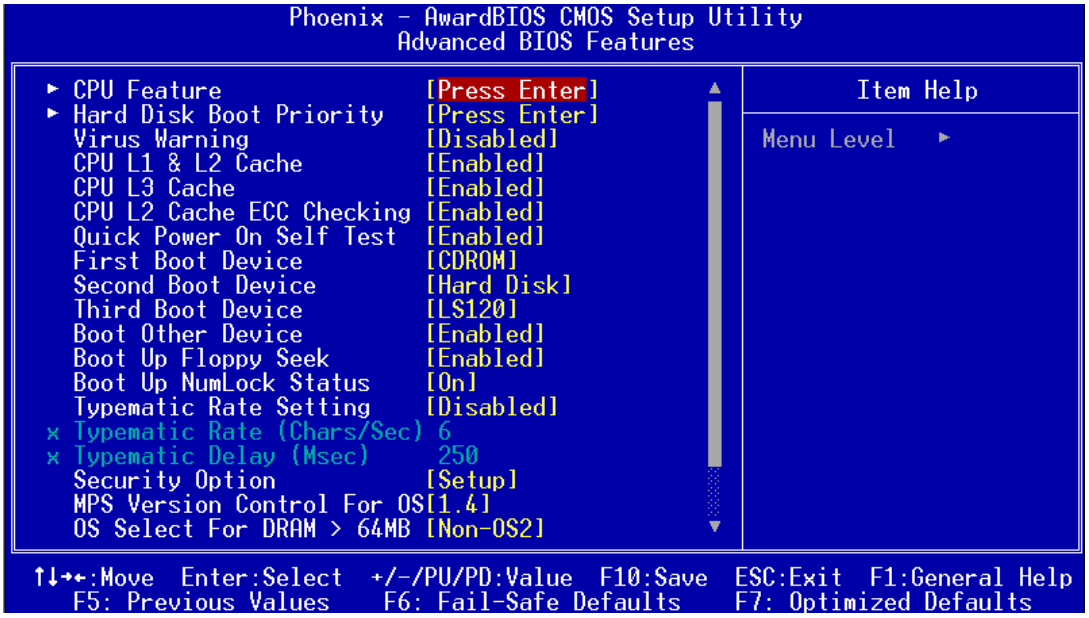
3.5.1.2 IDE Adapter Setup

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive. Use the following table to configure the hard disk.

Item	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Channel 0 Master IDE Channel 0 Slave, IDE Channel 1 Master, IDE Channel 1 Slave	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Access Mode	CHS LBA Large Auto	Choose the access mode for this hard disk
Capacity	Auto Display your disk drive size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
The following options are selectable only if the 'IDE Channel …' item is set to 'Manual'		
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** **Warning**: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

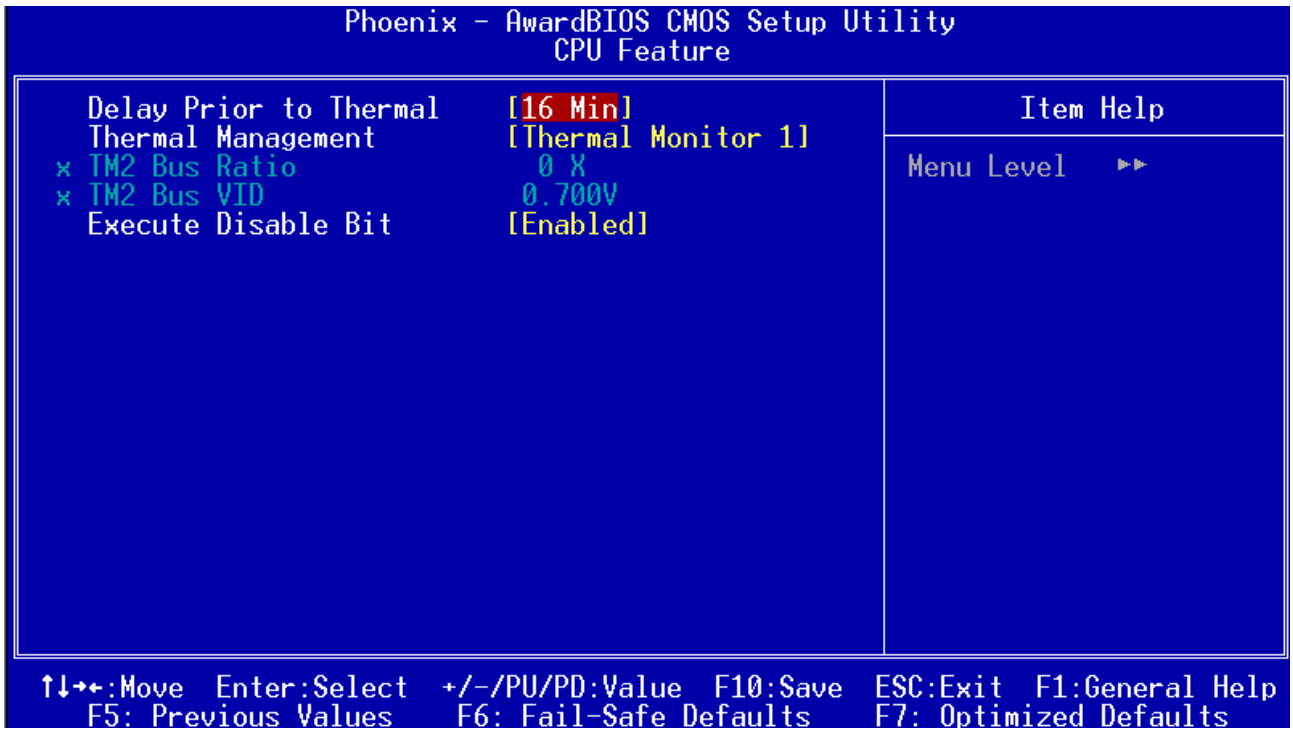
3.5.2 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



3.5.2.1 CPU Feature

This item allows you to select the CPU feature.

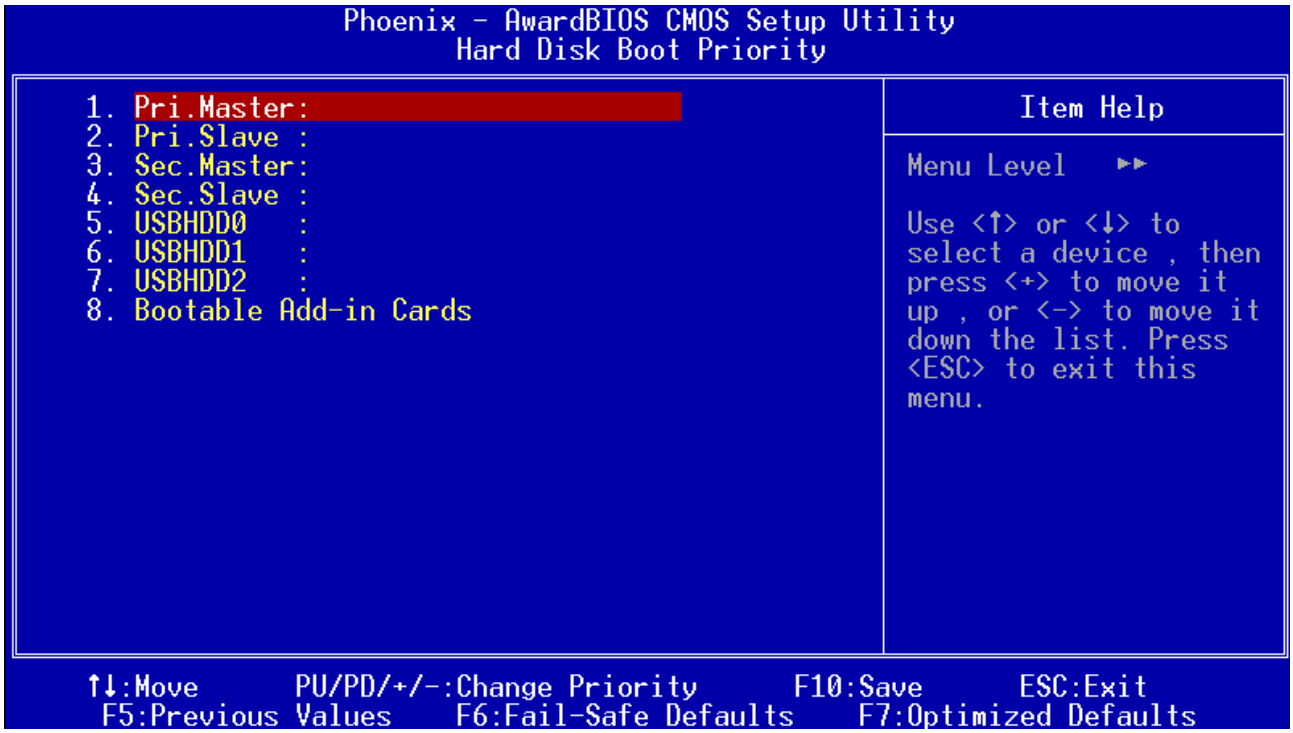


Item	Option	Description
Delay Prior to Thermal	4 Min 8 Min 16 Min 32 Min	

Thermal Management	Thermal Monitor 1 Thermal Monitior 2	
Execute Disable Bit	Enabled Disabled	

3.5.2.2 Hard Disk Boot Priority

This item allows you to select the Hard Disk device boot up priority.



Item	Description
Pri.Master	Boot up from IDE Primary Master Hard Disk
Pri.Slave	Boot up from IDE Primary Slave Hard Disk
Sec.Master	Boot up from IDE Secondary Master Hard Disk
Sec.Slave	Boot up from IDE Secondary Slave Hard Disk
USBHDD0	Boot up from First USB Hard Disk
USBHDD1	Boot up from Second USB Hard Disk
USBHDD2	Boot up from Thrid USB Hard Disk
Bootable Add-in Cards	Boot up from other Add-In Card Hard Disk Device.

3.5.2.3 Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Item	Description
Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

3.5.2.4 CPU L1 & L2 Cache

This item allows you to speed up memory access. However, it depends on CPU design.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.5 CPU L3 Cache

This is the extra cache that sits on the motherboard between the processor and main memory, since the processor already contains L1 and L2 cache and starting to ship with L3 cache built-in as well to speed up memory operations further. However, it depends on CPU design.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.6 CPU L2 Cache ECC Checking

This feature enables or disables the L2 cache's ECC checking function (if available). Enabling this feature is recommended because it will detect and correct single-bit errors in data stored in the L2 cache. It will also detect double-bit errors but not correct them. Still, ECC checking stabilizes the system, especially at overclocked speeds when errors are most likely to creep in.

There are those who advocate disabling ECC checking because it reduces performance. The performance difference is negligible, if at all. However, the stability and reliability achieved via ECC checking is real and substantial. It may even enable you to overclock higher than is possible with ECC checking disabled. So, enable it for added stability and reliability.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.7 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Item	Description
Enabled	Enable quick POST
Disabled	Normal POST

3.5.2.8 First/Second/Third/Other Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

Item	Description
Floppy	Floppy Device
LS120	LS120 Device
Hard Disk	Hard Disk Device
CDROM	CDROM Device
ZIP100	ZIP-100 Device
USB-FDD	USB Floppy Device
USB-ZIP	USB ZIP Device
USB-CDROM	USB CDROM Device
USB-HDD	USB Hard Disk Device
Legacy LAN	Network Device
Disabled	Disabled any boot device

3.5.2.9 Boot Other Device

This item allows you to enable the system to boot from other device.

Item	Description

Enabled	Enable booting from other device
Disabled	Disable booting from other device

3.5.2.10 Book Up Floppy Seek

Seeks disk drives during boot up. Disabling seeds boot up.

Item	Description
Enabled	Enable Floppy Seek
Disabled	Disable Floppy Seek

3.5.2.11 Boot Up NumLock Status

Select power on state for NumLock.

Item	Description
On	Enable NumLock
Off	Disable NumLock

3.5.2.12 Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

Item	Description
Enabled	Enable typematic rate/delay setting
Disabled	Disable typematic rate/delay setting

3.5.2.13 Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a key stroke when you hold the key down.

The choice: 6, 8, 10, 12, 15, 20, 24, 30.

3.5.2.14 Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke.

The choice: 250, 500, 750, 1000.

3.5.2.15 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

Item	Description
System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

3.5.2.16 MPS Version Control For OS

This feature is only applicable to multiprocessor board as it specifies the version of the Multi-Processor Specification (MPS) that the board will use.

The choice: 1.4, 1.1.

3.5.2.17 OS Select for DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.

Item	Description

Non-OS2	Disable OS for over 64 MB DRAM
OS2	Enable OS for over 64 MB DRAM

3.5.2.18 Video BIOS Shadow

To allow copying Video BIOS into shadow RAM to improve video performance.

Item	Description
Enable	Copy Video BIOS into shadow RAM
Disable	Do not copy Video BIOS into shadow RAM

3.5.2.19 Full Screen LOGO Show

If the BIOS had the full screen logo in it, this item could allow enable/ disable the full screen logo show on display.

Item	Description
Enable	Enable full screen logo show
Disable	Disable full screen logo show

3.5.2.20 Small Logo (EPA) Show

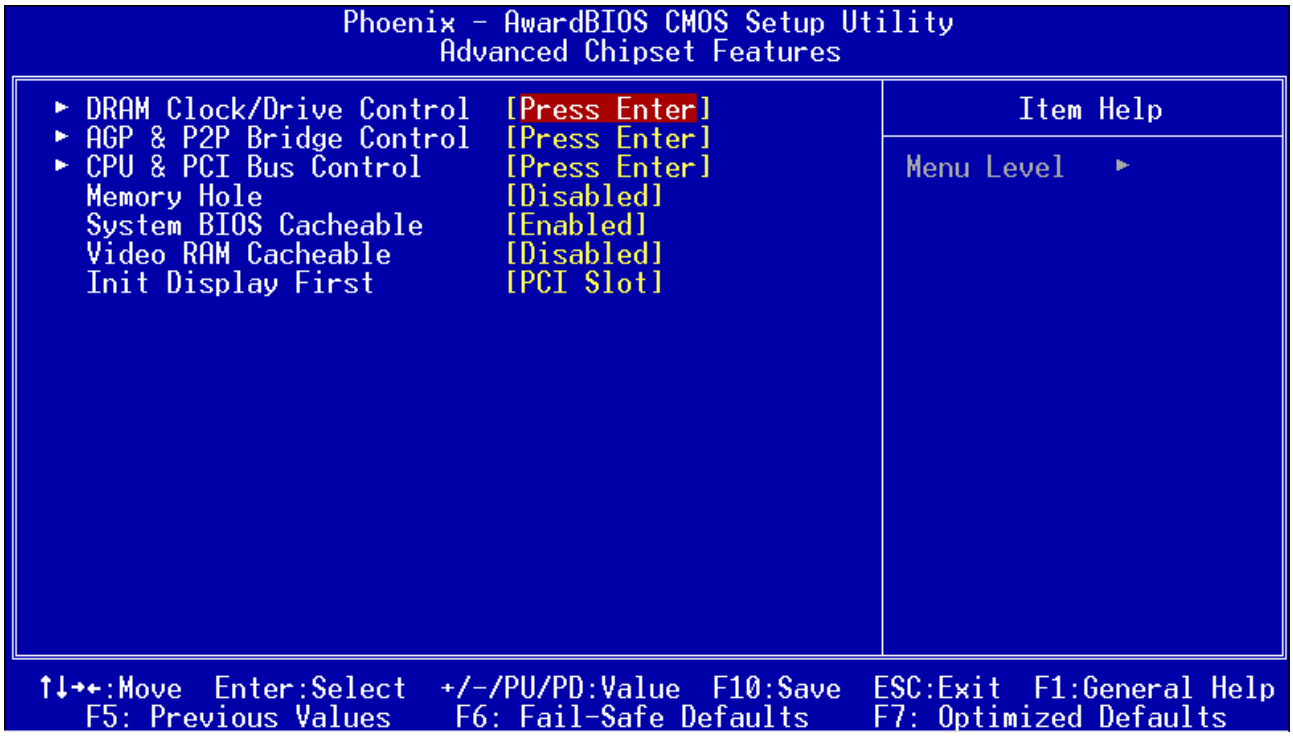
This item allows you enabled/disabled the small EPA logo show on screen at the POST step.

Item	Description
Enabled	EPA Logo show is enabled
Disabled	EPA Logo show is disabled

3.5.3 Advanced Chipset Features

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.



3.5.3.1 DRAM Clock/Drive Control

This section can set the DRAM clock/driver timing.

Item	Options	Description
DRAM Clock	By SPD 200 MHz 266 MHz	Set the memory bus frequency to operate at various values for the proper memory clock setting
DRAM Timing	Manual Auto By SPD	Set the memory timings for the said timings or DRAM Cycle Lengths of 2 or 2.5.
SDRAM CAS Latency (DDR/DDR2)	1.5 / 2 2 / 3 2.5 / 4 3 / 5	This controls the time dealy passing before the SDRAM starts to carry out a read command after receiving it.
Bank Interleave	Diabled 2 Bank 4 Bank 8 Bank	Enables to set the interleave mode of the SDRM interface which allows banks of SDRAM to alternate their refresh and access cycles.
Precharge to Active(Trp)	2T 3T 4T 5T	This item sets the length of time taking to precharge a row in the memory module before a row being active and appears only when **DRAM timing** is set at **Manual**. Longer values are safer but probably not acting the best performance.
Active to Precharge(Tras)	05T, 06T, 07T, 08T 09T, 10T, 11T, 12T 13T, 14T, 15T, 16T 17T, 18T, 19T, 20T	This item sets the length of time that a row staying active fore precharging and appears only when **DRAM timing** is set at **Manual**. Longer values are safer but probably not acting the best performance.
Active to CMD(Trcd)	2T 3T 4T 5T	This timing controls the length of the delay between when a memory bank is activated to when a read/write command is sent to that bank.
REF to ACT/REF to REF(Trfc)	08T ~ 71T	Set the REF to ACT/REF to REF timing. This field appears when **DRAM Timing** is set at **Manual**.
ACT(0) to ACT(1) (TRRD)	2T 3T 4T 5T	Set the minimum time interval between successive ACTIVE commands to the different banks. This field appears when **DRAM Timing** is set at **Manual**.
Read to Precharge (Trtp)	2T 3T	Use this option to select Read to Precharge (Trtp) to set the timing by dram SPD.
Write to Read CMD (Twtr)	2T / 3T 1T / 2T	Use this option to select Write to Read CMD (Twtr) to set the timing by dram SPD.
Write Recovery Time (Twr)	2T 3T 4T 5T	Use this option to select Write Recovery Time (Twr) to set the timing by dram SPD.
DRAM Command Rate	2T Command 1T Command	Allows to set the DRAM Command Rate.
RDSAIT mode	Manual Auto	
RDSAIT selection	3	Key in a HEX number (Min = 0000, Max = 003F)

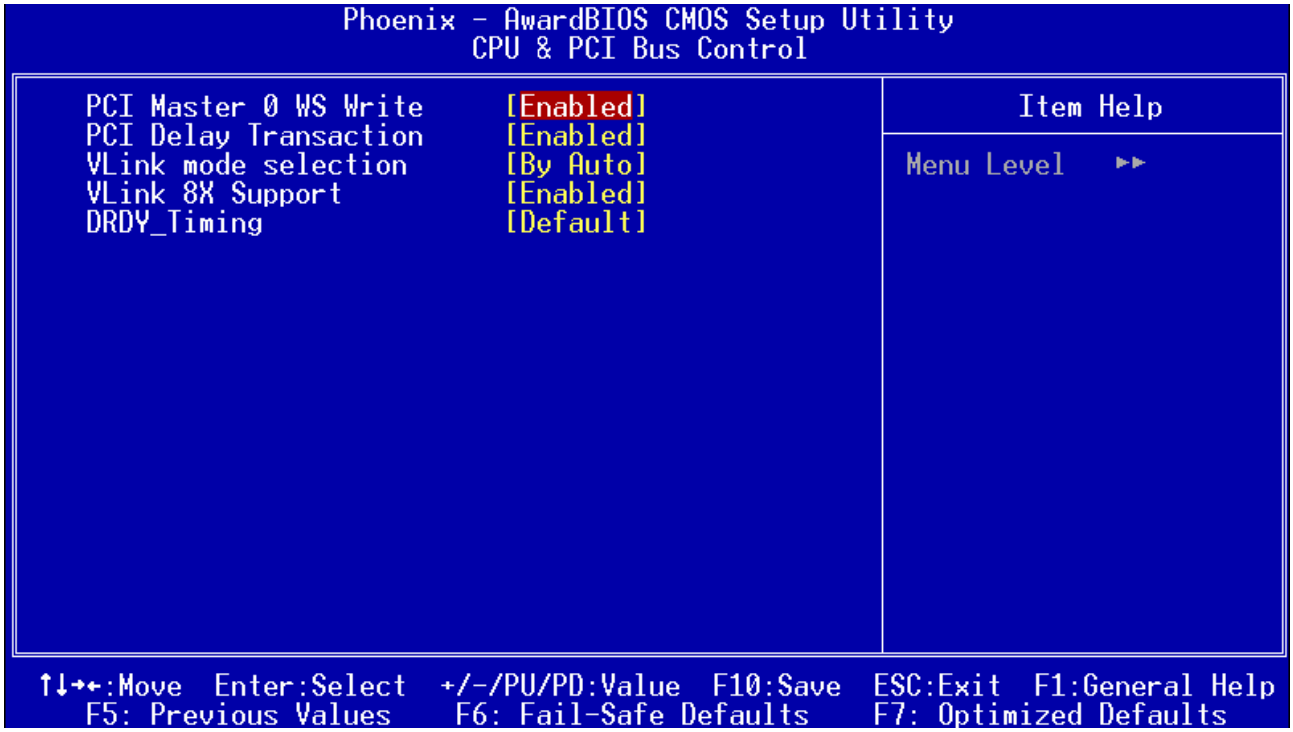
3.5.3.2 AGP & P2P Bridge Control

This item stores the onboard AGP and P2P function information. The reference table is as below.

Item	Options	Description
AGP Aperture Size	32M, 64M, 128M, 256M, 512M, 1G	Select the size of Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation.
AGP 3.0 Mode	8X, 4X	This item allows you to select the AGP 3.0 mode to 8X or 4X.
AGP Driving Control	Auto Manual	This item allows you to select the AGP Driving Control to auto / disable Mode.
AGP Driving Value	00 ~ FF	This item allows you to set the AGP Driving value
AGP Fast Write	Enabled Disabled	This feature controls the AGP bus's Fast Write capability. It accelerates memory write transactions from the chipset to the AGP device.
AGP Master 1 WS Write	Enabled Disabled	Enabled this item to increase AGP writing
AGP Master 1 WS Read	Enabled Disabled	Enabled this item to increase AGP reading
AGP 3.0 Calibration Cycle	Enabled Disabled	This option allows you to disable the AGP 3.0 calibration cycle. This cycle ensures that the on-die termination impedance signal swing and slew rate of the AGP signals are calibrated on a periodic basis to ensure signal integrity. It is recommended to keep this setting enabled.
VGA Share Memory Size	16M, 32M, 64M	Select the size of onboard video controller's frame buffer. The buffer size shares from system memory unit.
Direct Frame Buffer	Enabled Disabled	This item allows you to select the Direct Frame Buffer to enabled / disabled.
Select Display Device	CRT, LCD, TV, HDTV, CRT+LCD, CRT+TV CRT+HDTV	This item allows you to select display device.
Panel Type	640x480 1x18B 800x600 1x18B 1024x768 1x18B 1280x768 1x18B 1280x1024 2x18B 1400x1050 2x18B 1600x1200 2x18B 1280x800 1x18B 800x480 1x18B 1024x768 2x18B 1024x768 1x24B 1024x768 2x24B 1280x768 1x24B 1280x1024 2x24B 1400x1050 2x24B 1600x1200 2x24B	This item allows you to select the panel type.
Outport Port	DI0, DI1	This item allows you to select the outport port.
Dithering	Enabled, Disabled	This item allows you to enable dithering.

TV_Layout	Default COMP. + S-Video S-Video + S-Video COMP. + R/G/B COMP. + Y/Cb/Cr COMP. + SDTV-R, G, B COMP. + SDTV-Y, Pb, Pr COMPOSITE S - Video R, G, B Y, Cb, Cr SDTV – R, G, B SDTV – Y, Pb, Pr S – Video + R, G, B S – Video + Y, Cb, Cr	This item allows you to select TV Layout Disply
TV_type	NTSC PAL / PAL B / PAL G /PAL PALM PLAN PALNc PAL I PAL D NTSC Japan	This item allows you to select your TV type
TV_Connector	CVBS S – Video 0 R / G / B Cr / Y /Cb SDTV – R / G /B SDTV / Pr / Y Pb S – Video 1	This item allows you to select what kind of TV connectors you use.
HDTV_type	SDTV 480P HDTV 720P HDTV 1080I HDTV 1080P	This item allows you to select the input resolution of HDTV
HDTV_Connector	R / G / B Pr / Y / Pb	This item allows you to select the input connector of HDTV

3.5.3.3 CPU & PCI Bus Control



Item	Options	Description
PCI Master 0 WS Write	Enabled Disabled	To write PCI bus while zero wait state is executed.
PCI Delay Transaction	Enabled Disabled	This feature is used to meet the latency of PCI cycles to and from the ISA bus. The ISA bus is much, much slower than the PCI bus. Thus, PCI cycles to and from the ISA bus take a longer time to complete and this slows the PCI bus down. However, enabling **PCI Delayed Transaction** enables the chipset's embedded 32-bit posted write buffer to support delayed transaction cycles. This means that transactions to and from the ISA bus are buffered and the PCI bus can be freed to perform other transactions while the ISA transaction is underway. This option should be **enabled** for better performance and to meet PCI 2.1 specifications. “Disabled” is set only if the PCI cards cannot work properly or if an ISA card that is not PCI 2.1 compliant is used.
VLink Mode Selection	By Auto Mode 0 Mode 1	The North Bridge interface to the South Bridge through a high speed (up to 1GB/Sec)8x, 66MHz Data Transfer interconnect bus caller “V-Link”. This item allows you to select the V-Link mode.
VLink 8X Support	Enabled Disabled	The feature is to toggle the V-Link bus mode between the original V-Link and the newer and faster 8X V-Link.
DDRY_Timing	Slowest Default Optimize	This item allows you to set the DDRY timing.

3.5.3.4 Memory Hole

This feature allows you to create a memory hole.

Item	Description
Disabled 15M-16M	When this item is enabled, ISA ROM will be mapped to 15-16M area and also support legacy ISA devices. While this item is disabled and legacy ISA devices are not utilized, the graphic performance will be enhanced

3.5.3.5 System BIOS Cacheable

This feature is only valid when the system BIOS is shadowed. It enables or disables the caching of the system BIOS ROM at **F0000h-FFFFFh** via the L2 cache. This greatly speeds up accesses to the system BIOS. However, this does **not** translate into better system performance because the OS does not need to access the system BIOS much.

Item	Description
Enabled	Cacheable
Disabled	Non-Cacheable

3.5.3.6 Video RAM Cacheable

It enables or disables the caching of the video RAM at **A0000h-AFFFFh**. This greatly speeds up the video performance.

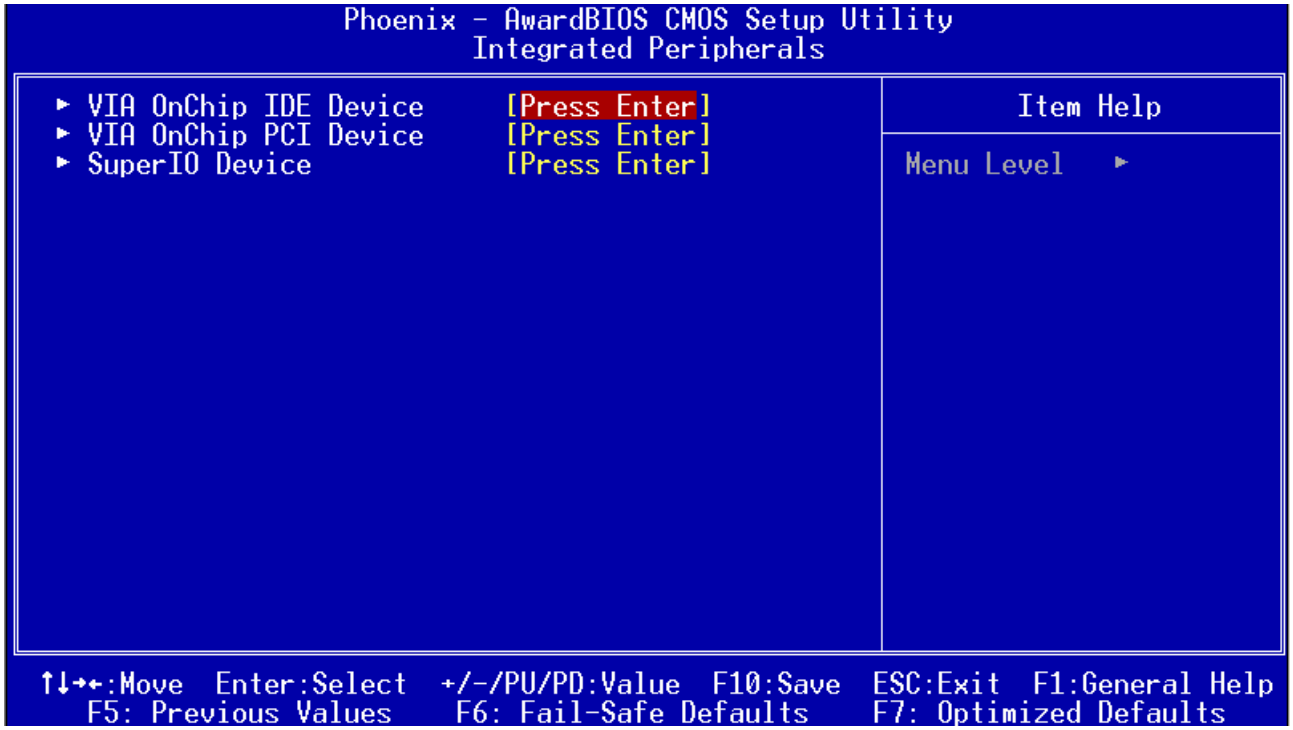
Item	Description
Enabled	Cacheable
Disabled	Non-Cacheable

3.5.3.7 PCI Slot, AGP

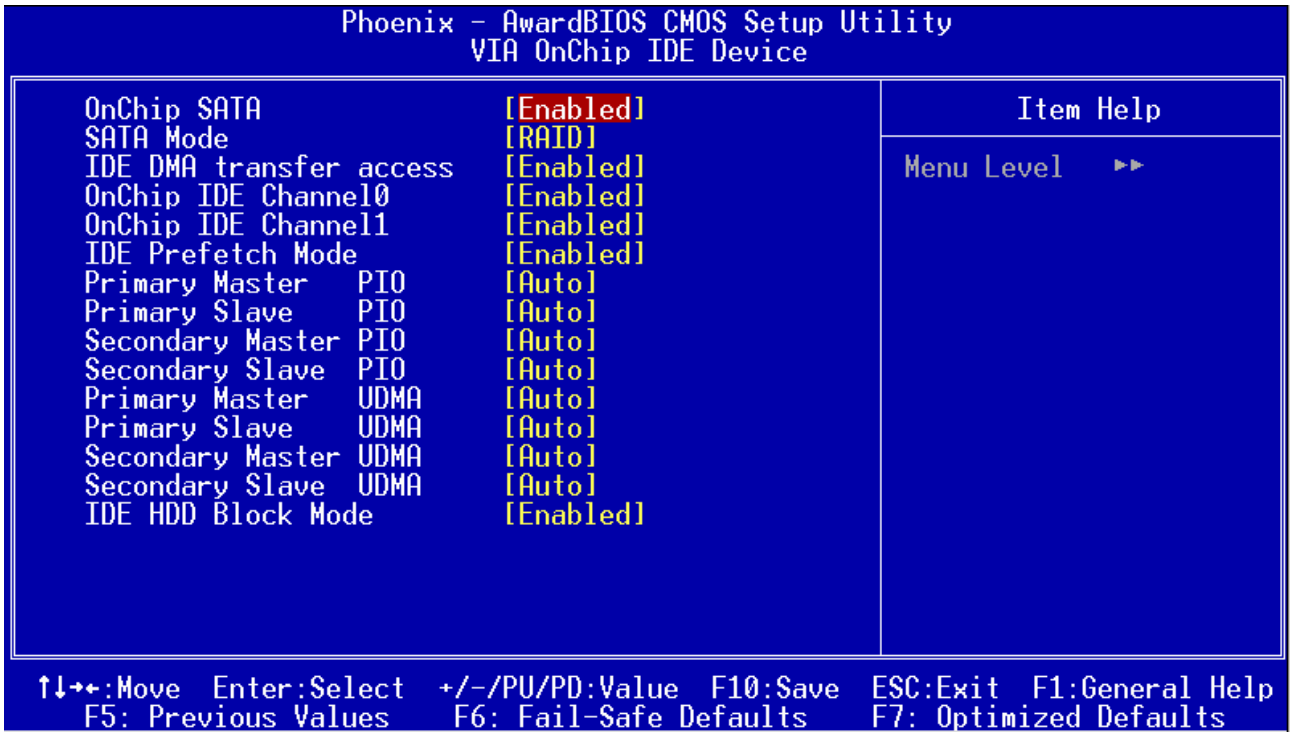
This item allows you to decide to active whether PCI Slot or Onboard/AGP first.
The choices: PCI Slot, Onboard, AGP, PCIE Slot.

3.5.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

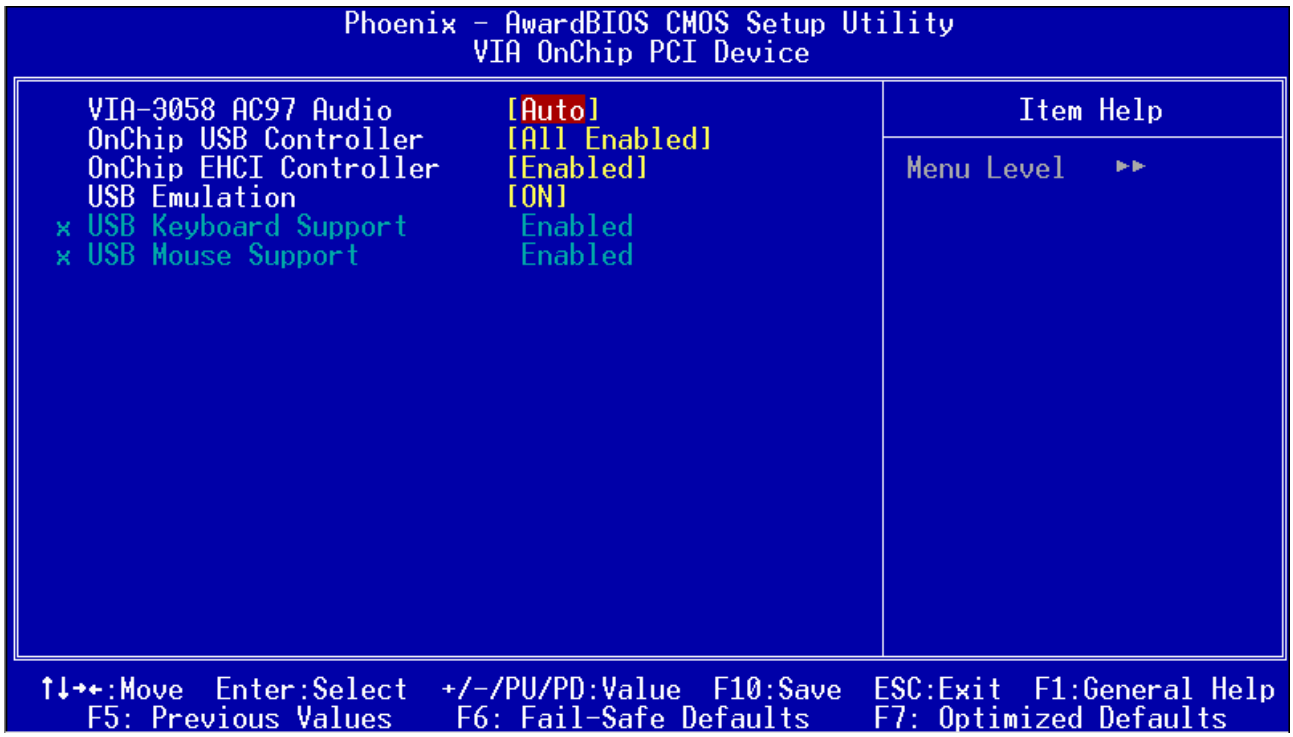


3.5.4.1 VIA OnChip IDE Device



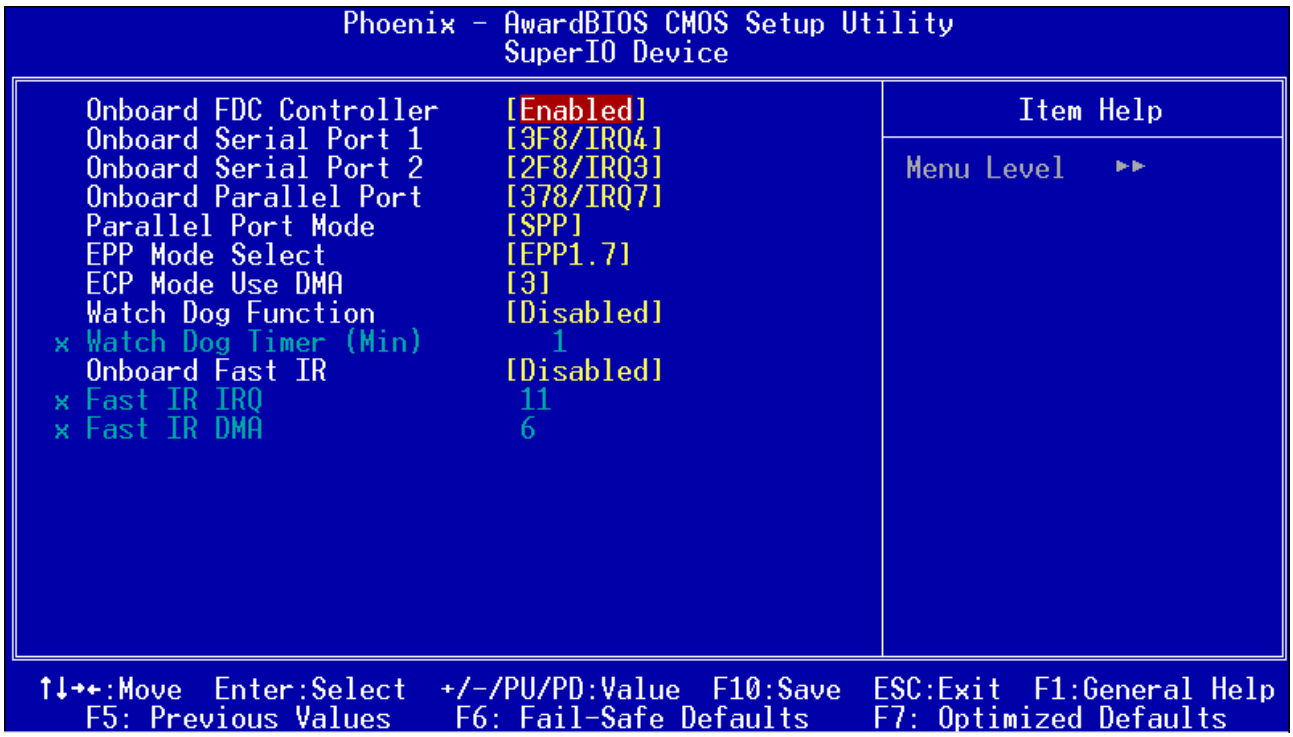
Item	Options	Description
SATA Controller	Enabled Disabled	The chipset contains a SATA IDE interface with support for two IDE channels. Select Enabled to activate the primary IDE interface (Channel0). Select Disabled to deactivate this interface.
SATA Mode	IDE RAID	Setup the onboard SATA Mode.
IDE DMA transfer access	Enabled Disabled	This feature allows you to enable or disable DMA support for all IDE devices.
OnChip IDE Channel10/1	Enabled Disabled	The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary / secondary IDE interface (Channel 10/1). Select Disabled to deactivate this interface.
IDE Prefetch Mode	Enabled Disabled	For faster drive accesses. If you install a primary and/or secondary add-in IDE interface, set this field to Disabled if the interface does not support prefetching.
IDE Primary Master PIO IDE Primary Slave PIO IDE Secondary Master PIO IDE Secondary Slave PIO	Auto Mode 0 Mode 1 Mode 2 Mode 3 Mode 4	The IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.
IDE Primary Master UDMA IDE Primary Slave UDMA IDE Secondary Master UDMA IDE Secondary Slave UDMA	Auto Disabled	Ultra DMA implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If the hard drive and the system software both support Ultra DMA, select Auto to enable BIOS support.
IDE HDD Block Mode	Enabled Disabled	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If the IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.

3.5.4.2 VIA OnChip PCI Device



Item	Options	Description
VIA-3058 AC97 Audio Controller	Auto Disabled	This item allows you to decide to enable / disable the VIA chipset family to support AC97 Audio.
OnChip USB Controller	All Disabled All Enabled 1 & 2 USB Port 2 & 3 USB Port 1 & 3 USB Port 1 USB Port 2 USB Port 3 USB Port	It enable easy connection between PCs and other applications equipped with USB interfaces such as printers, scanners, modems, and other PC peripherals.
OnChip EHCI Controller	Enabled Disabled	It enables the EHCI (USB 2.0) controller.
USB Emulation	OFF KB / MS ON	It allows you to select USB emulation. OFF: It does not support any USB device on DOS. KB/MS: It supports USB legacy keyhoard and mouse except for USB storage. ON: It supports USB legacy keyboard, mouse and storage.

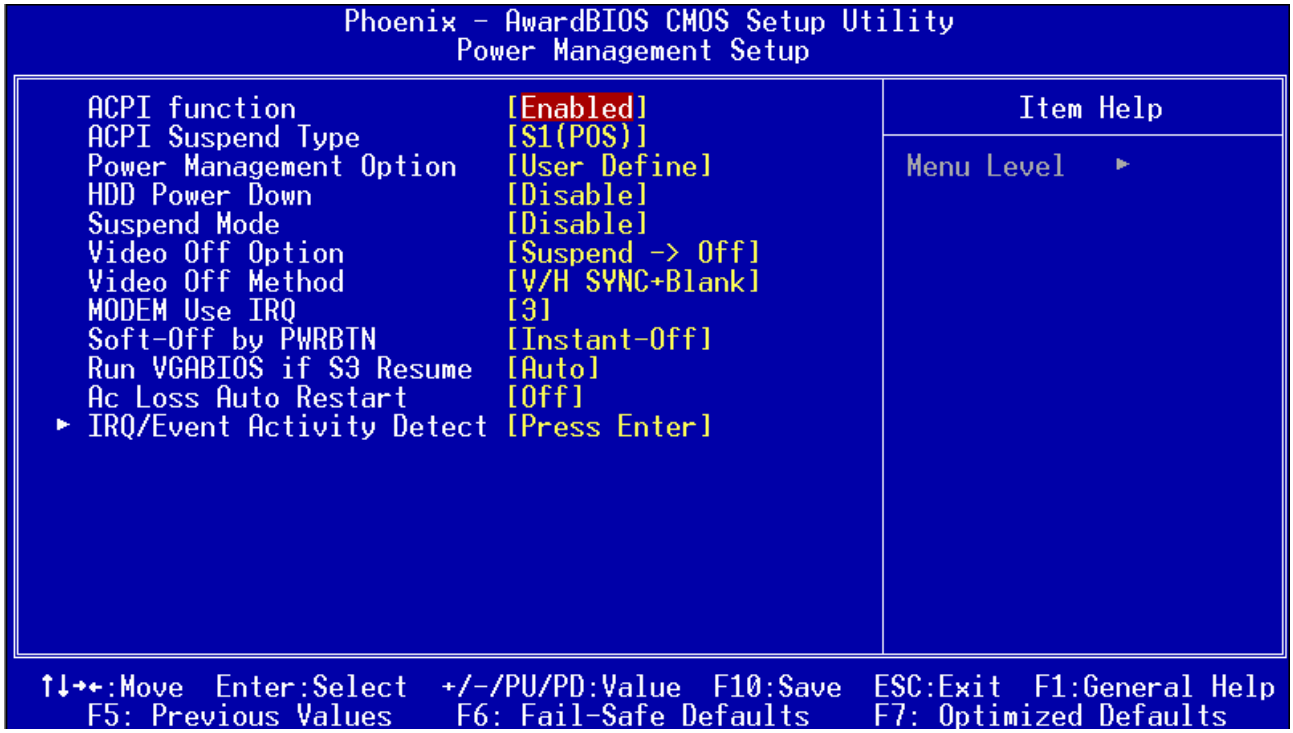
3.5.4.3 Super IO Device



Item	Options	Description
Onboard FDC Controller	Disabled / Enabled	This item is to set whether you wish to use onboard floppy disk controller (FDC).
Onboard Serial Port 1 Onboard Serial Port 2	Disabled, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4 , 2E8/IRQ3, AUTO	Select an address and corresponding interrupt for the first and second serial ports.
Onboard Parallel Port	Disabled, 378 / IRQ7, 278 / IRQ5, 3BC / IRQ7, AUTO, FDD MODE	Configure the LPT Port
Parallel Port Mode	SPP, EPP, ECP, ECP + EPP	This item is to set the parallel port mode.
EPP Mode Select	EPP 1.9 EPP 1.7	This item is to set the version of EPP that parallel port should use.
ECP Mode Use DMA	1, 3	This item is to select DMA1 or DMA3 for ECP mode
Watch Dog Function:	Disabled Enabled	This item is to set the Watch Dog function Enabled/Disabled.
Watch Dog Timer <Min>:	1	This item is to set the timer of Watch Dog function.
Onboard Fast IR:	Enabled Disabled	This item is to set the Onboard Fast IR function Enabled/ Disabled.
Fast IR IRQ:	11, 5 3, 4	Select a corresponding interrupt for Fast IR.
Fast IR DMA:	6, 5	Select a DMA channel for Fast IR.

3.5.5 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.



3.5.5.1 ACPI Function

This item allows you to enable/disable the ACPI function.

The choices: Enabled, Disabled.

3.5.5.2 ACPI Suspend Type

This item allows you to select ACPI suspend type.

The choices: S1 (POS), S3 (STR)

3.5.5.3 Power Management Option

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

Item	Description
Min. Power Saving	Minimum power management, HDD Power Down = 15 Min,
Max. Power Saving	Maximum power management, HDD Power Down =1 Min,
User Defined	Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr. except for HDD Power Down which ranges from 1 min. to 15 min. and disable.

3.5.5.4 HDD Power Down

There are three selections for Power Management Option; both of them have fixed mode settings.

The choices: Disabled, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 Min.

3.5.5.5 Suspend Mode

This setting defines the number of minutes before the system enters "suspend mode", the deepest level of system inactivity shutdown. The exact definition depends on the system, but in general this mode means that all system devices are shutdown (except for any that the BIOS is specifically told to keep running) and the processor is shut down to a trickle mode..

The choices: Disabled, 1, 2, 4, 6, 8, 10, 20, 30, 40 Min, 1 Hour.

3.5.5.6 Video Off Option

This determines the manner in which the monitor is always on or turned off during suspend mode.

The choices: Always On, Suspend -> Off.

3.5.5.7 Video Off Method

This item allows you to select the video off method.

The choices: Blank Screen, V/H SYNC+Blank, DPMS Support

3.5.5.8 MODEM Use IRQ

This determines the IRQ in which the MODEM can use.

The choices: NA, 3, 4, 5, 7, 9, 10, 11.

3.5.5.9 Soft-Off by PWRBTN

Pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has "hung".(Only could working on ATX Power supply)

The choices: Delay 4 Sec, Instant-Off.

3.5.5.10 Run VGABIOS if S3 Resume

This item is to set whether to run VGABIOS if S3 resume.

The choices: Auto, Yes, No

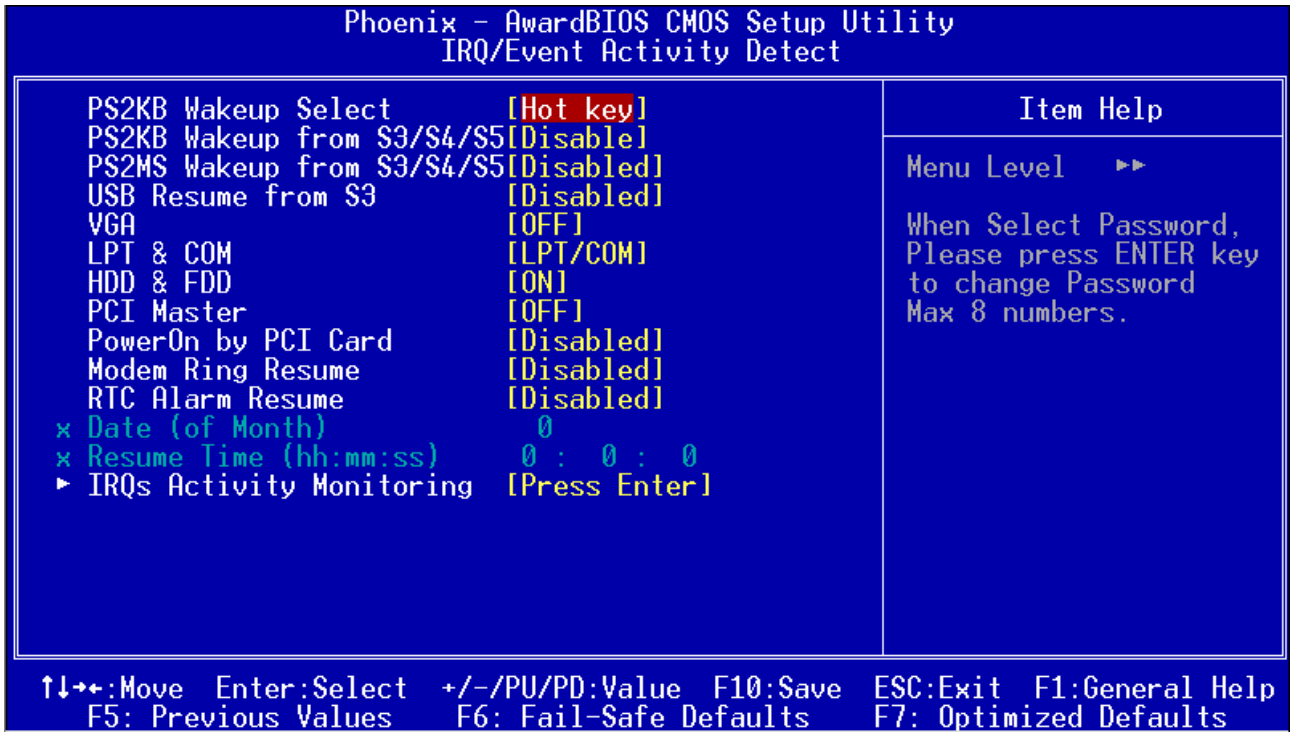
3.5.5.11 Ac Loss Auto Restart:

This item is to set whether to run Ac Loss Auto Restart.

The choices: Off, On, Former-Sts.

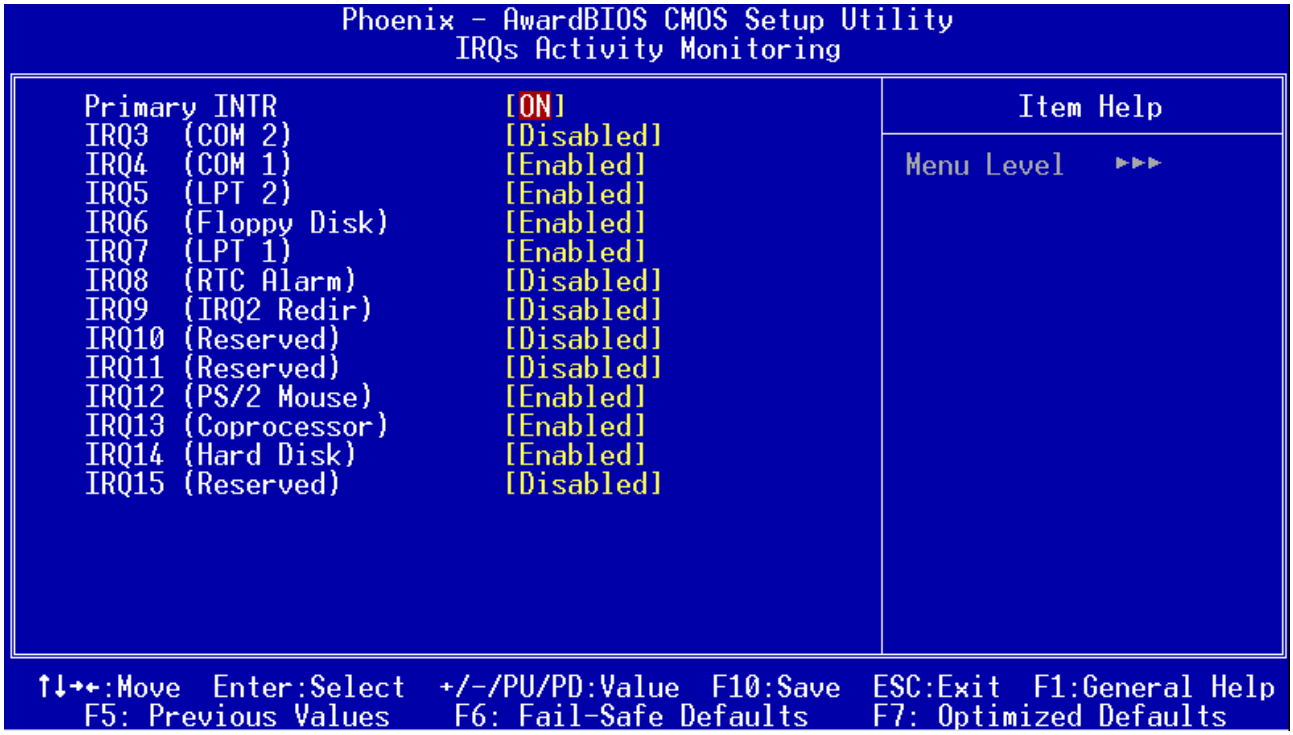
3.5.5.12 IRQ / Event Activity Detect

The IRQ / Event Activity Detect allows you to configure you system for the wake-up function.



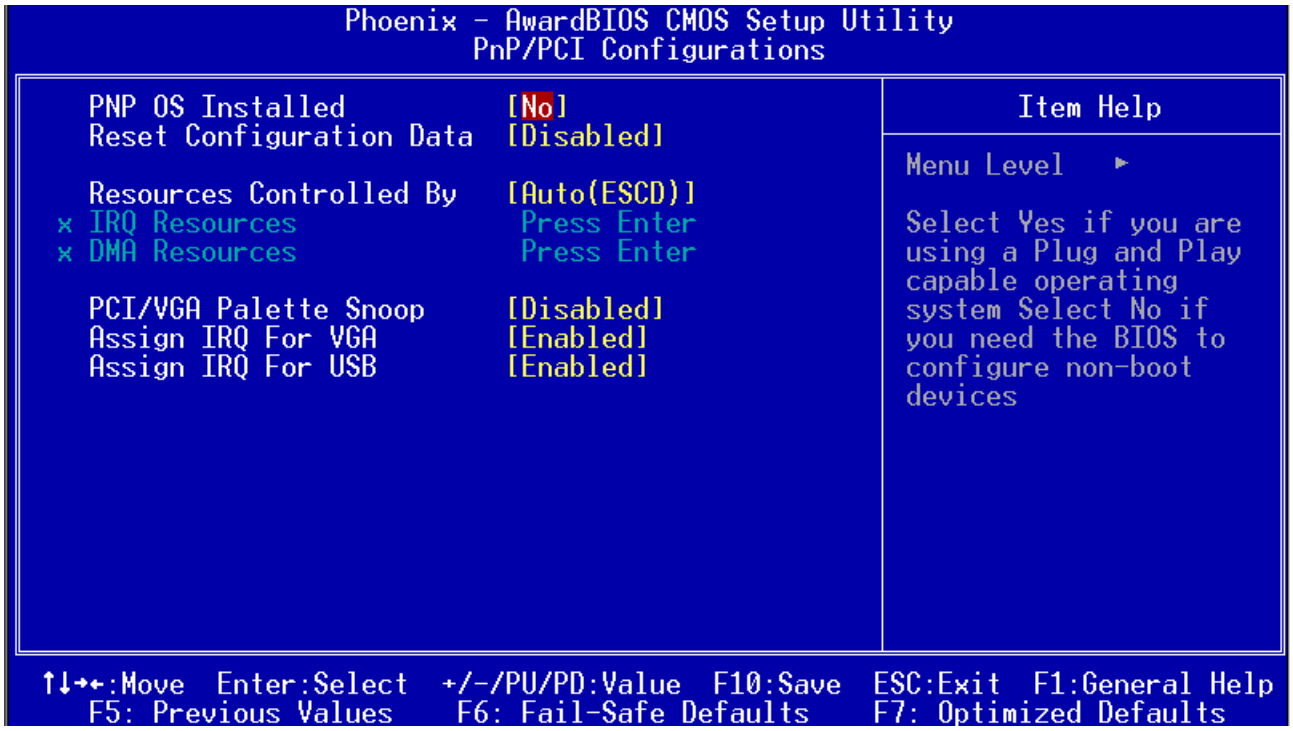
Item	Option	Description
PS2KB Wakeup Select	Hot Key Password	Allows you to select the method of PS2KB wakeup
PS2KB Wakeup from S3/S4 / S5	Disable Ctrl + F1~F12 Power Wake Any Key	Allows you to set the key of PS2 keyboard wakeup from S3 state
PS2MS Wakeup from S3 / S4 / S5	Disabled Enabled	Allows you to set the key of PS2 mouse wakeup from S3 state
USB Resume from S3	Disabled Enabled	Allows the activity of the USB device to wake up the system from S3 (Suspend to RAM) state.
VGA, LPT & COM, HDD & FDD, PCI Master	Disabled / Enabled ON / OFF NONE , LPT, COM, LPT/COM	These fields specify whether the system will be awakened from power saving modes when activity or input signal of the specified hardware peripheral or component is detected.
PowerOn by PCI Card	Disabled Enabled	Allows you to set power on by PCI card
Modem Ring Reume	Disabled Enabled	Allows you to resume modem ring

RTC Alarm Resume	Disabled Enabled	Allows you to enable or disable RTC alarm
Date (of Month)	0	Not applicable with RTC Alarm Resume disabled
Resume Time (hh:mm:ss)	0	Not applicable with RTC Alarm Resume disabled
IRQs Activity Monitoring		
Primary INTR IRQ3 ~ IRQ15	Off, On Enabled, Disabled	Primary INTR: Allows you to restore the system to an active state if IRQ activity is detected from any of the enabled channels IRQ3 ~ IRQ5: Enables or disables the monitoring of the specified IRQ line. These fields are only available if "Primary INTR" is on.



3.5.6 PnP / PCI Configuration

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.



3.5.6.1 PNP OS Installed

The choices: Yes, No.

3.5.6.2 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

The choices: Enabled, Disabled.

3.5.6.3 Resources Controlled By

The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. If you set this field to “manual” choose specific resources by going into each of the sub menu that follows this field (a sub menu is preceded by a “➢”).

The choices: Auto(ESCD), Manual.

3.5.6.4 IRQ Resources

When resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.

This item allows you to determine the IRQ assigned to the PCI bus or reserved.

The Choices: PCI, Reserved.

3.5.6.5 DMA Resources

Direct Memory Access (DMA) is where a device is allowed to take over the main computer bus from the CPU and transfer bytes directly to main memory or to some other device. This item allows you to assign each DMA channel a type, depending on the type of device using the DMA channel.

The Choices: PCI, Reserved.

3.5.6.6 PCI / VGA Palette Snoop

Leave this field at Disabled.

The choices: Enabled, Disabled.

3.5.6.7 Assign IRQ For VGA

While the system has one VGA controller and more than one VGA devices are connected, then "Enabled" is set. If the system VGA controller is not used, then "Disabled" is set.

The choices: Enabled, Disabled.

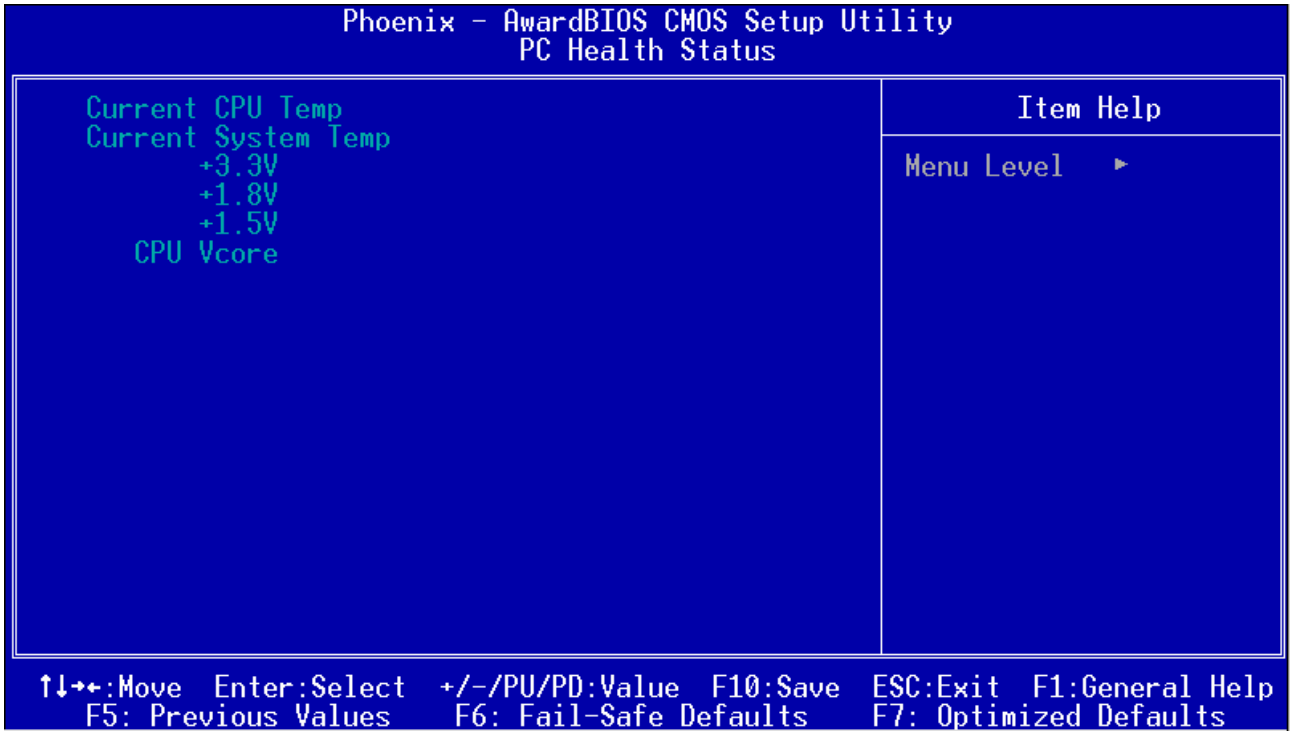
3.5.6.8 Assign IRQ For USB

While the system has one USB controller and more than one USB devices are connected, then "Enabled" is set. If the system USB controller is not used, then "Disabled" is set.

The choices: Enabled, Disabled.

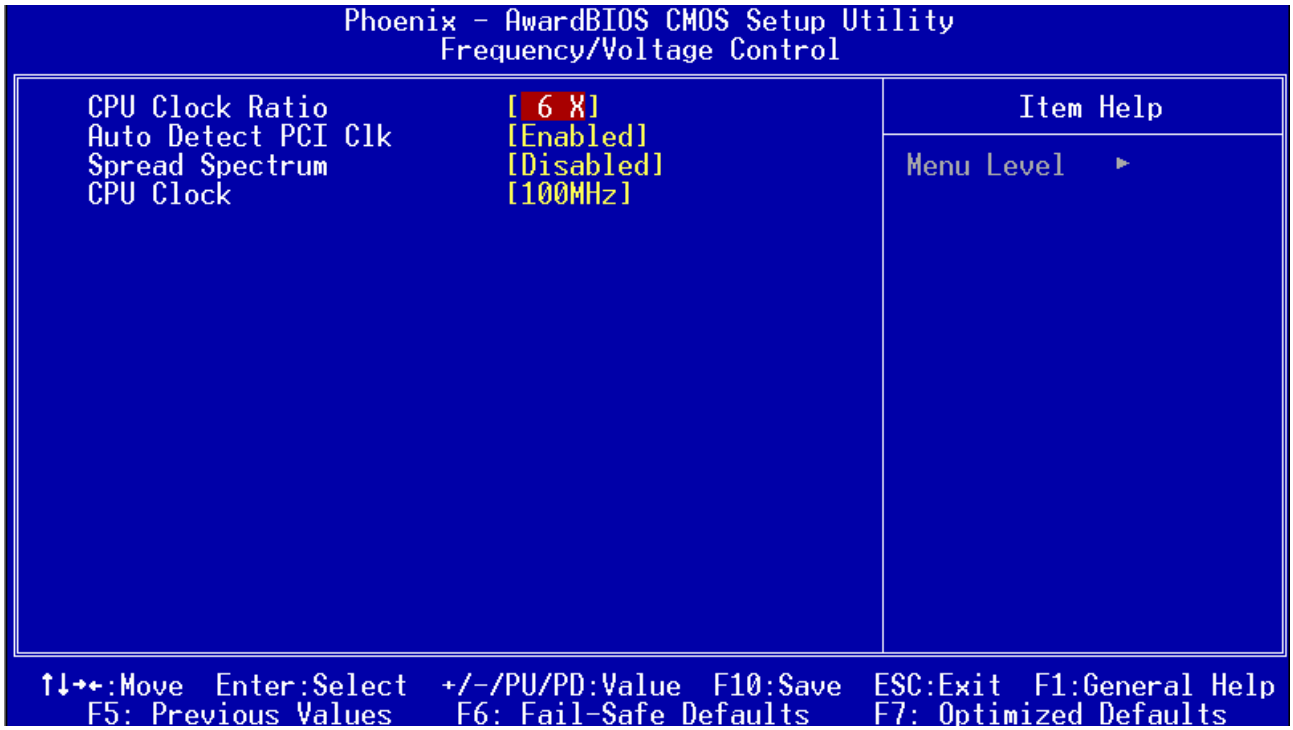
3.5.7 PC Health Status

This section shows the status of your CPU.



3.5.8 Frequency / Voltage Control

This menu specifies your setting for frequency/voltage control.



3.5.8.1 CPU Clock Ratio:

This item allows you to select the CPU clock ratio.

The choices: 4~12X

3.5.8.2 Auto Detect PCI Clk

This item allows you to enable or disable detecting PCI clock automatically.

The choices: Enabled, Disabled.

3.5.8.3 Spread Spectrum

This item is to adjust extreme values of the pulse for EMI test.

The choices: Enabled, Disabled.

3.5.8.4 CPU Clock

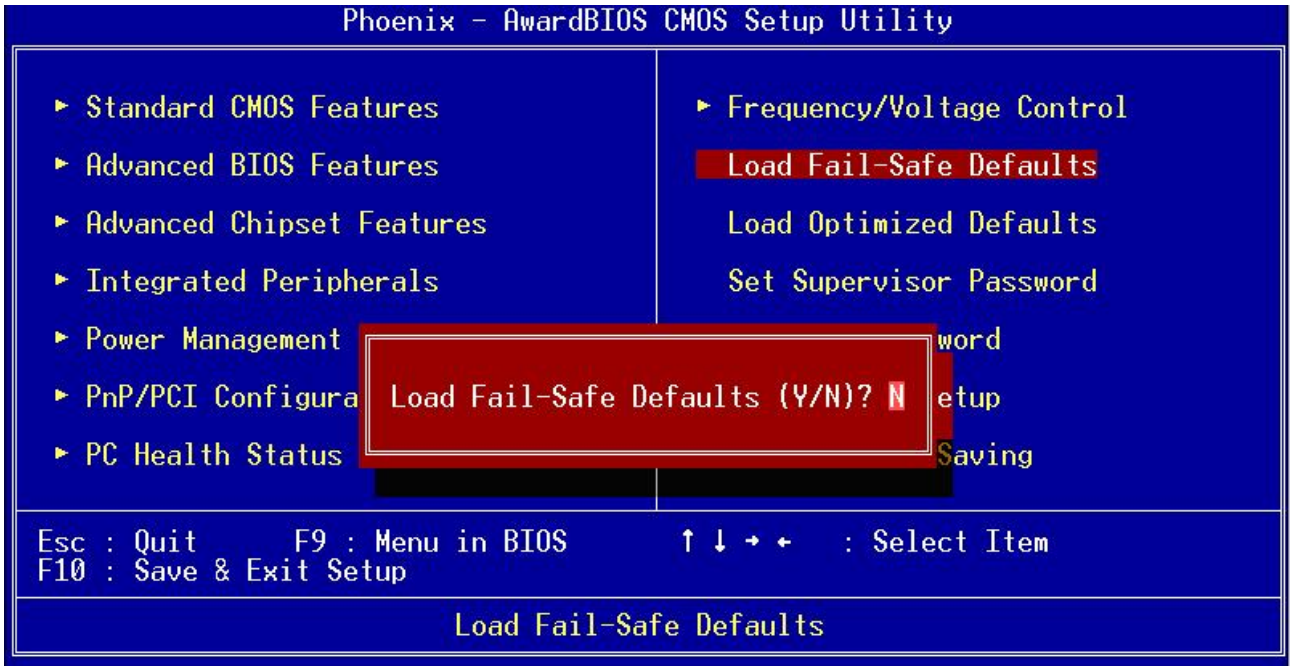
This item allows you to select the CPU clock.

The choices: 100~132Mhz

3.5.9 Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

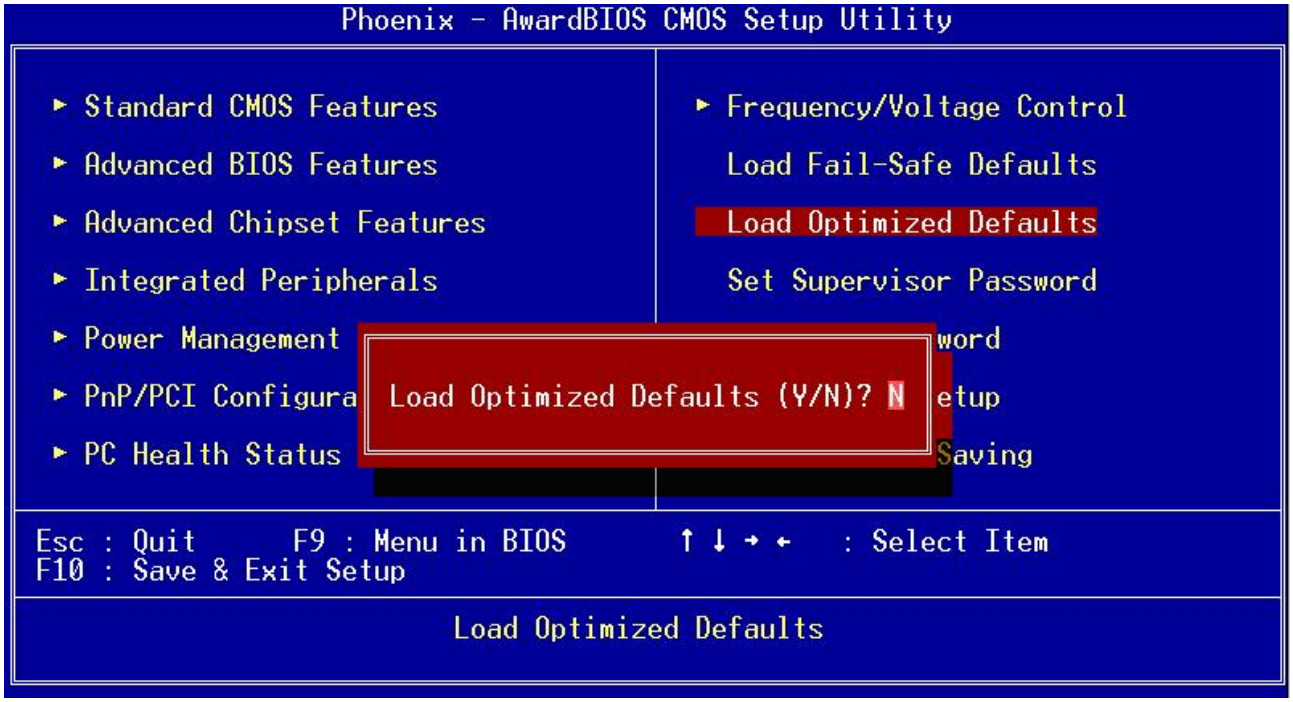
Press <Y> to load the BIOS default values for the most stable, minimal-performance system operations.



3.5.10 Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

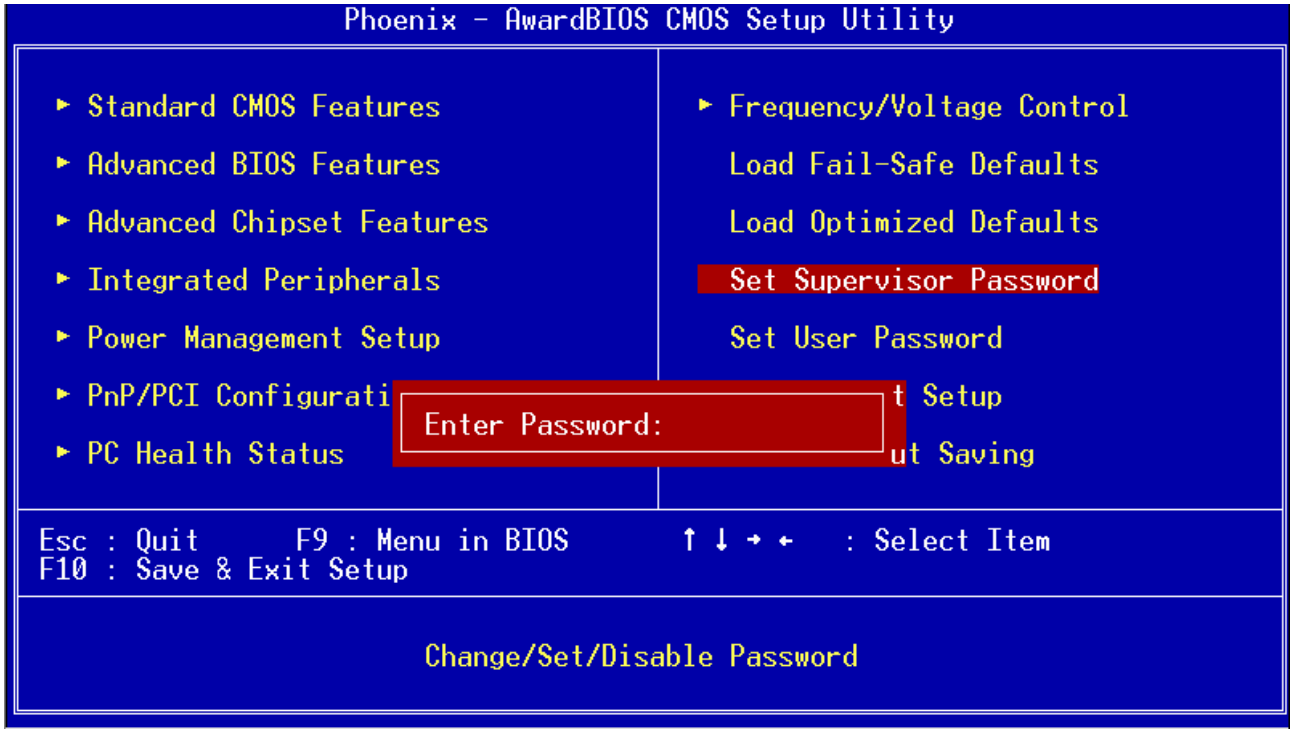
Press <Y> to load the default values setting for optimal performance system operations.



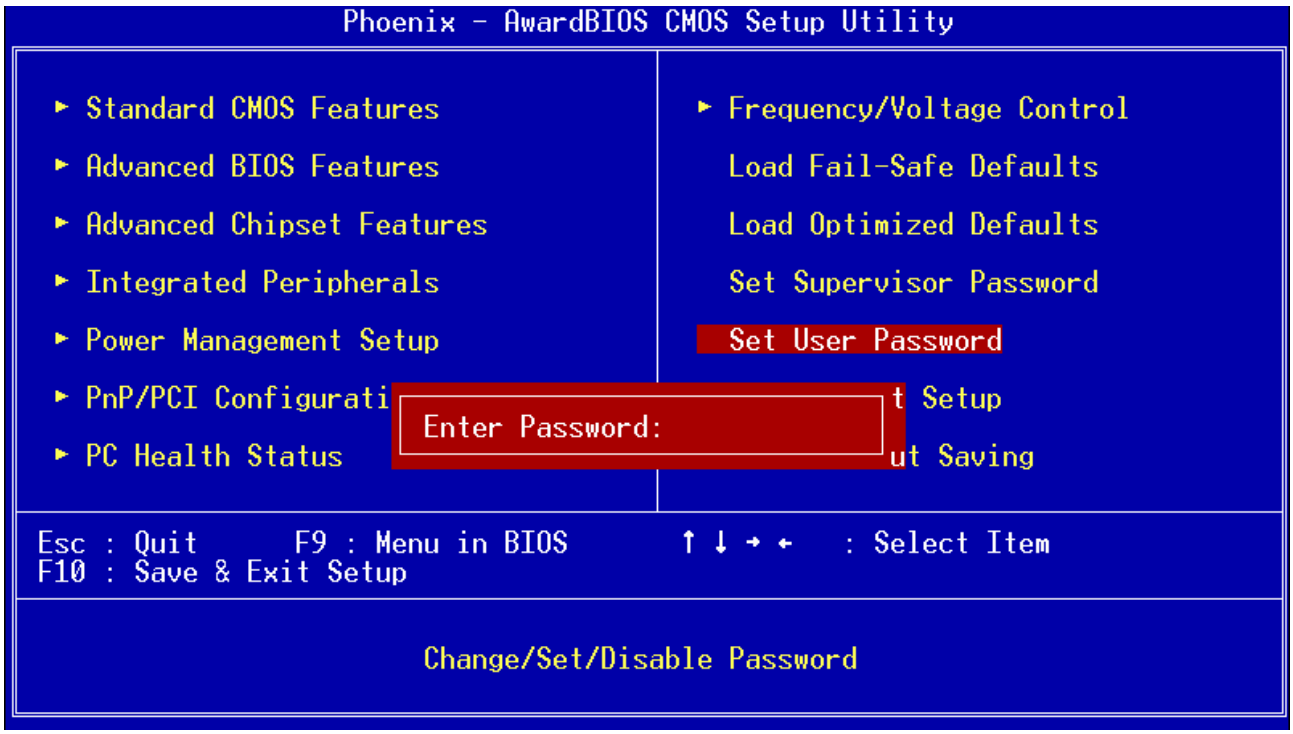
3.5.11 Set Supervisor / User Password

You can set either supervisor or user password, or both of them.

Supervisor Password: able to enter/change the options of setup menus.



User Password: able to enter but no right to change the options of setup menus.



Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also

press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

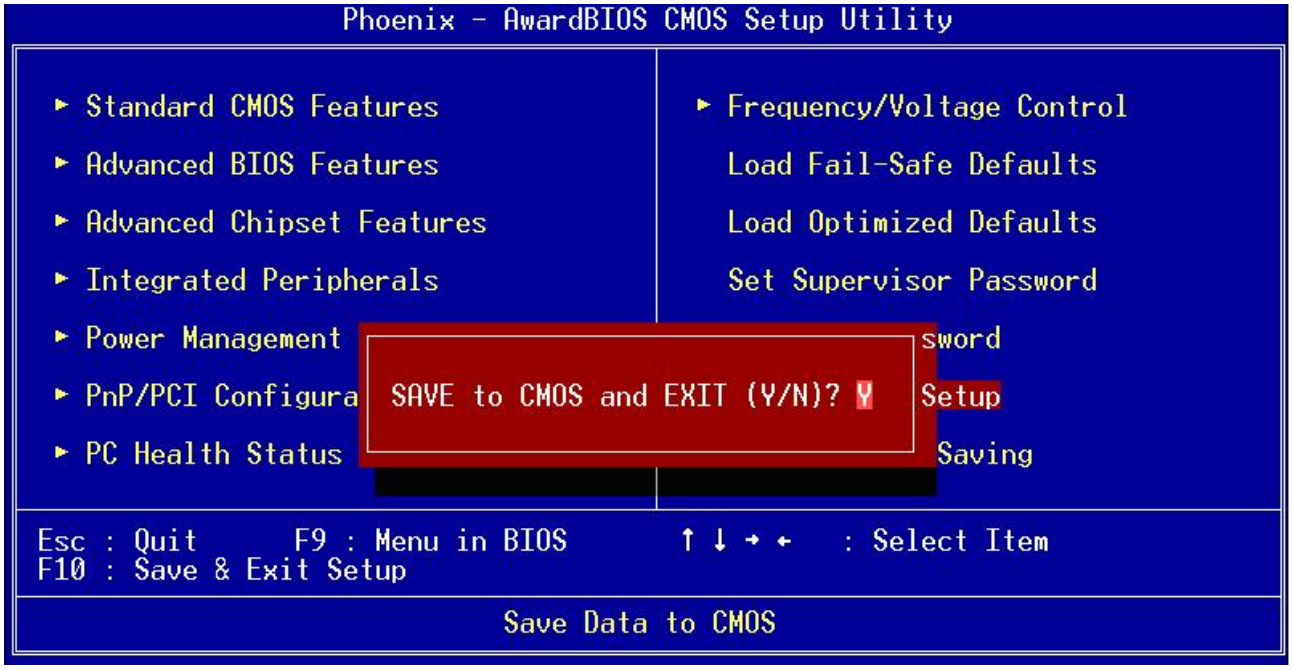
When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration. Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer. You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If set to “Setup”, prompting only occurs when trying to enter Setup

3.5.12 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

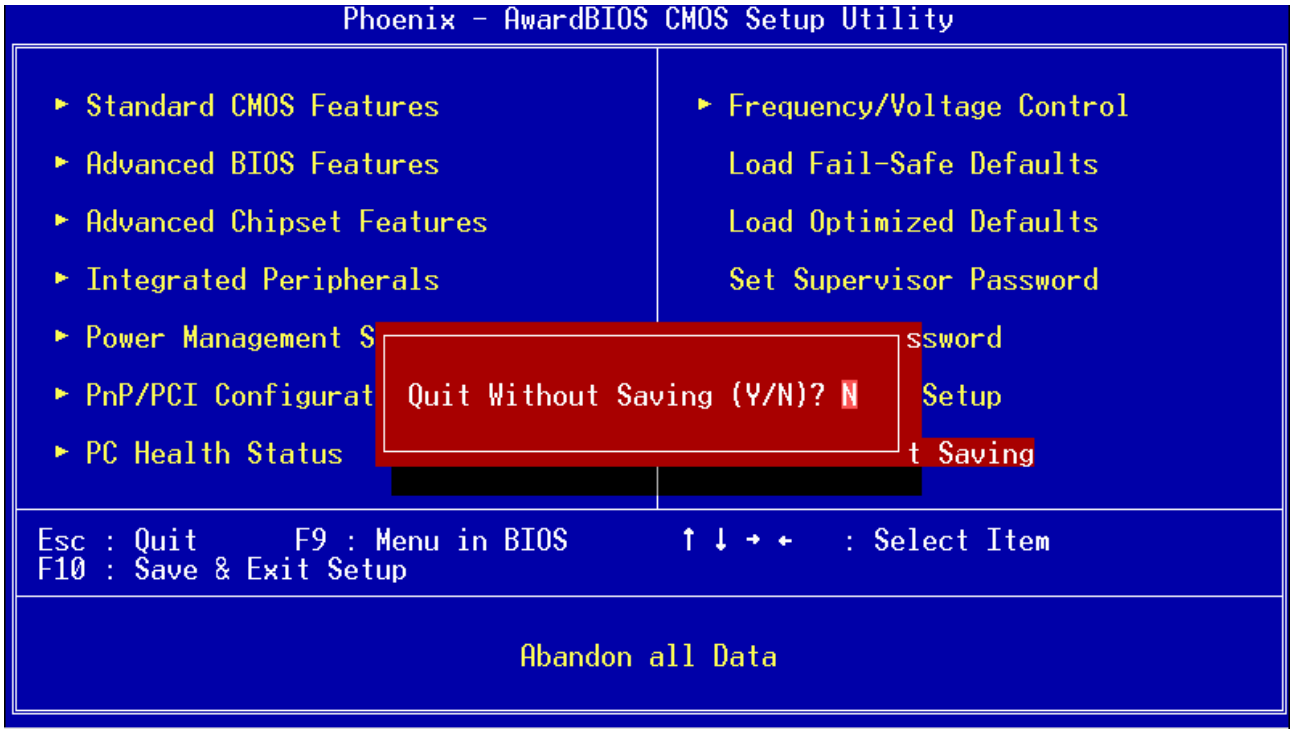
Enter <Y> to store the selection made in the menus in CMOS, a special section in memory that stays on after turning the system off. The BIOS configures the system according to the Setup selection stored in CMOS when boot the computer next time.

The system is restarted after saving the values.



3.5.13 Exit Without Save

Abandon all CMOS value changes and exit setup, and the system is restarted after exiting.



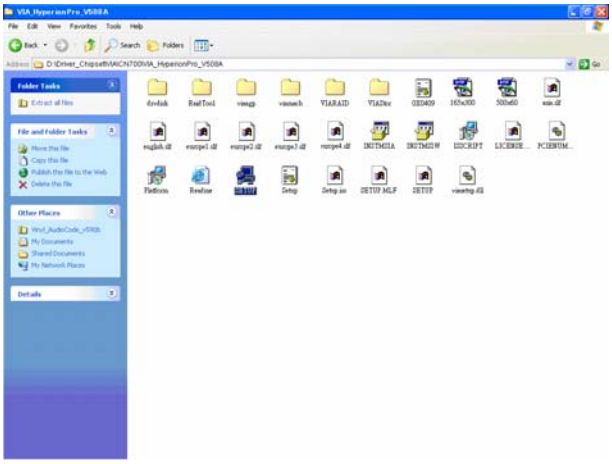
4 Drivers Installation

Note: Installation procedures and screen shots in this section are for your reference and may not be exactly the same as shown on your screen.

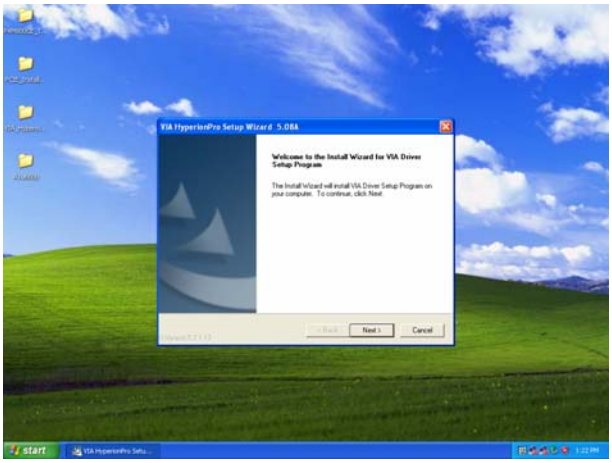
4.1 Install Chipset Driver (For VIA CN700)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Chipset\VIA\CN700.**

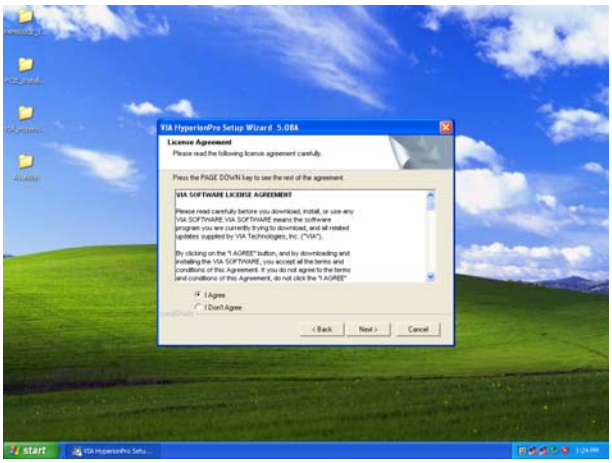
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



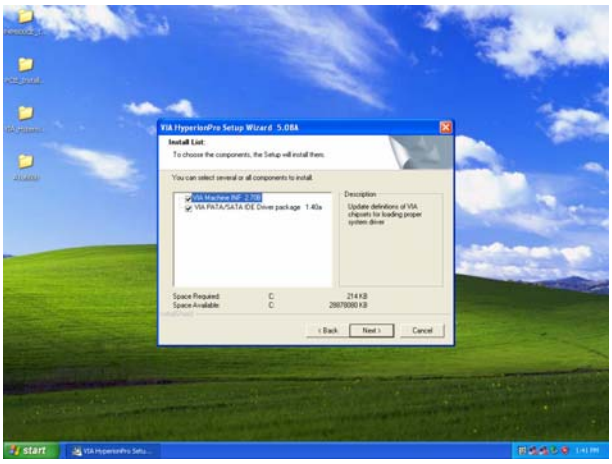
Step 1. Locate「\Driver_Audio\VIA\CN700\VIA_HyperionPro_V508A\setup.exe」.



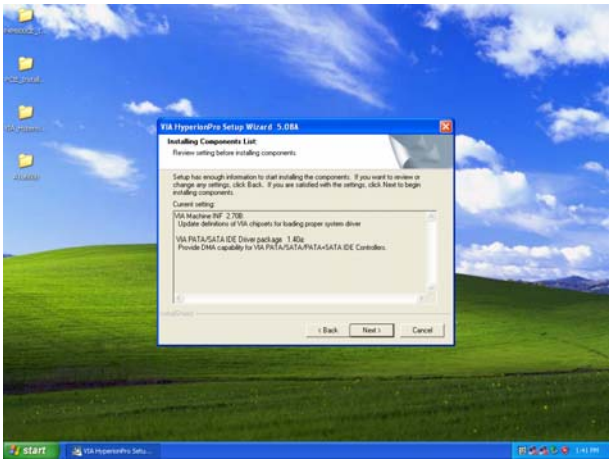
Step 2. Click **Next**.



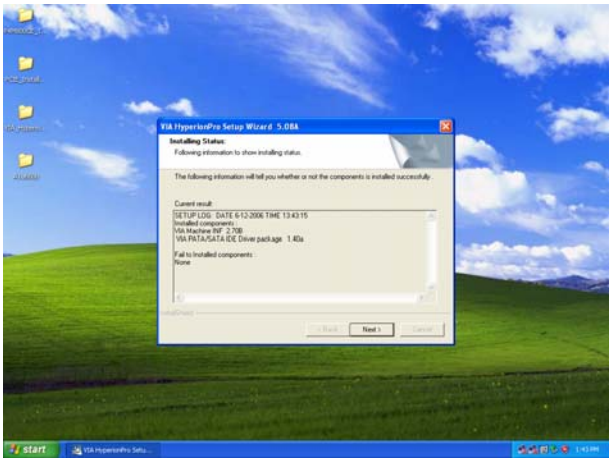
Step 3. Select **I Agree** and click **Next** to the following step.



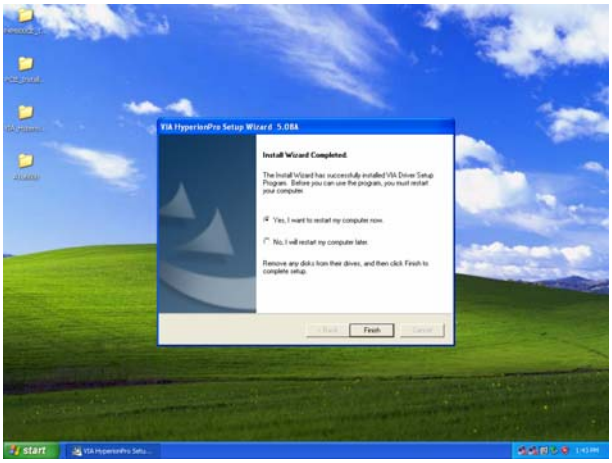
Step 4. Select both items and click **Next** to run the setup.



Step 5. Click **Next**.



Step 6. Click **Next**.

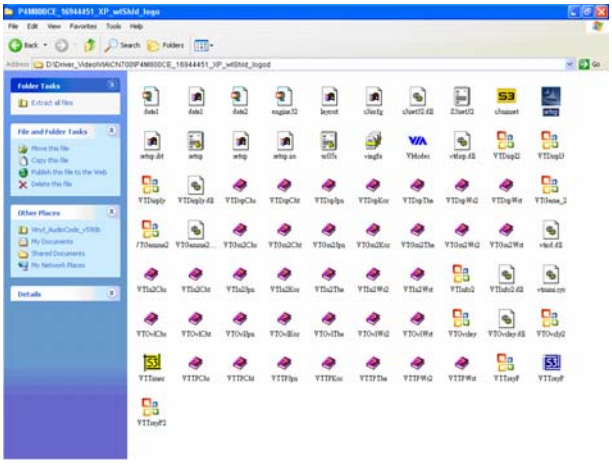


Step 7. Click Finish to restart the PC.

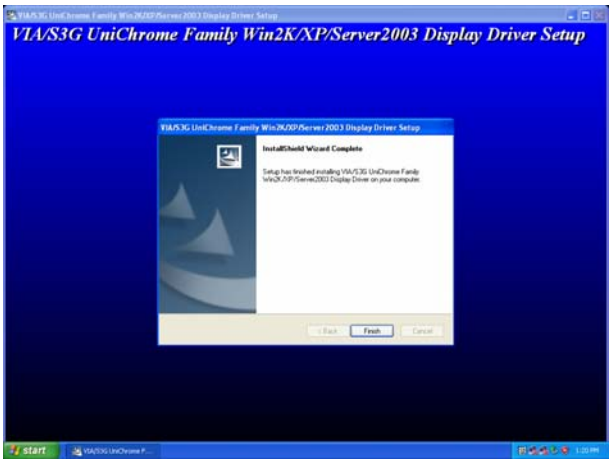
4.2 Install Display Driver (For VIA CN700)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Display\VIA\CN700**.

Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



Step1. Locate 「\Driver_Chipset\VIA \CN700\P4M800CE_16944451_XP _wIShld_logod\Setup.exe」.

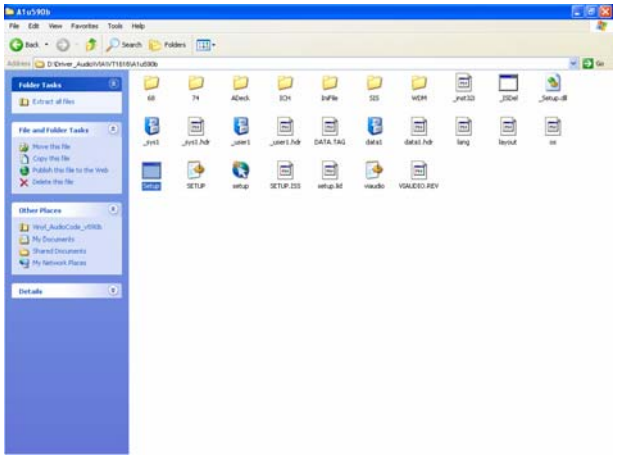


Step 2. Setup will run the installation automatically, then click **Finish** to complete.

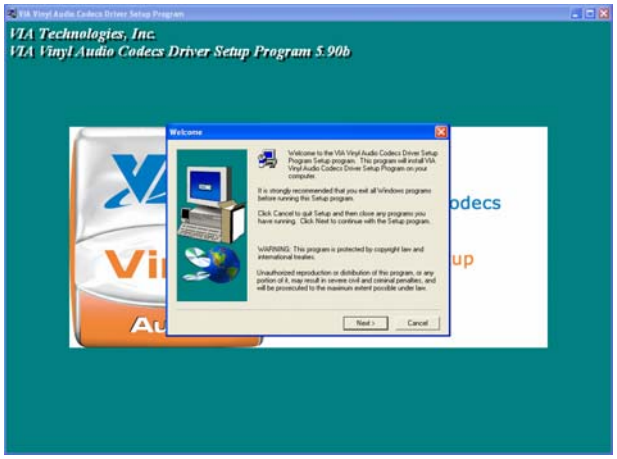
4.3 Install Audio Driver (For VIA VT1616)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Audio\VIA\VT1616.**

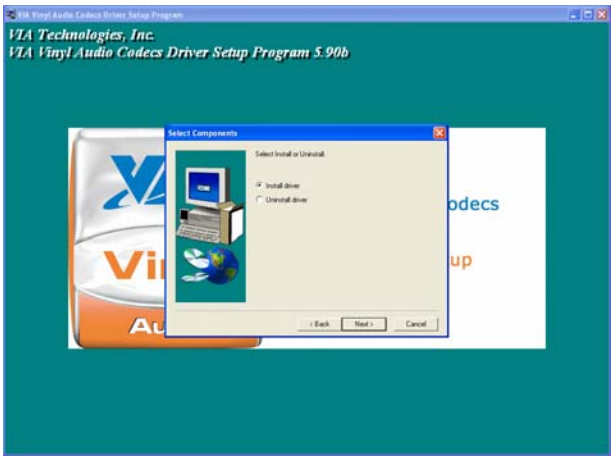
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



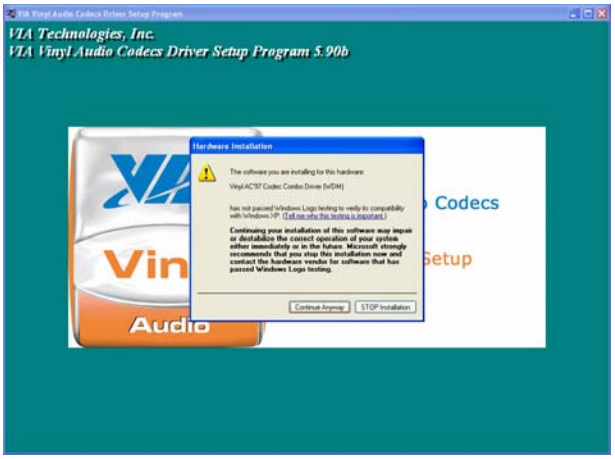
Step 1. Locate「\Driver_Audio\VIA\VT1616\A1u590b\setup.exe」.



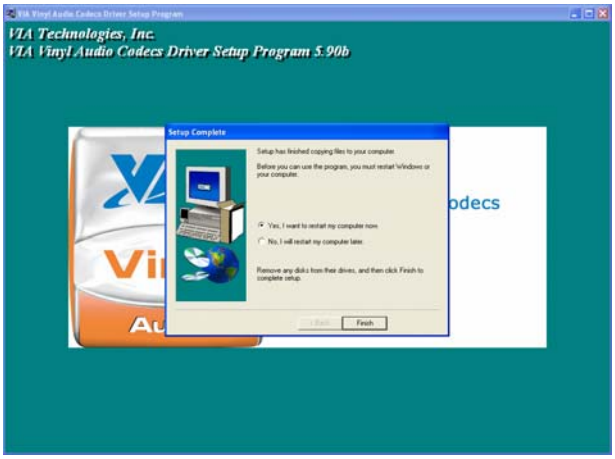
Step 2. Click **Next**.



Step 3. Select **Install Driver** and click **Next** to the following step.



Step 4. Click **Continue Anyway** to run the setup.

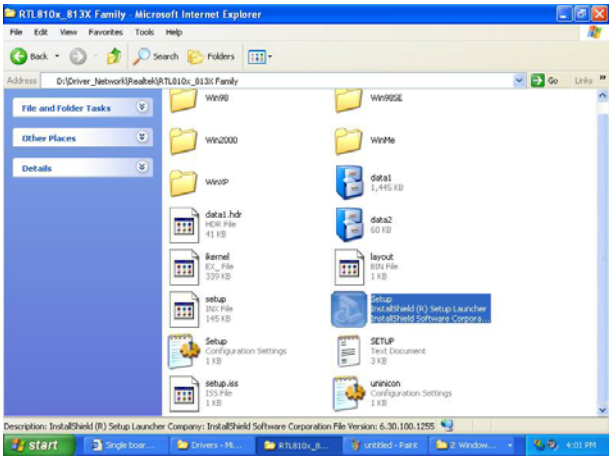


Step 5. Click **Finish** to complete the setup and restart the PC.

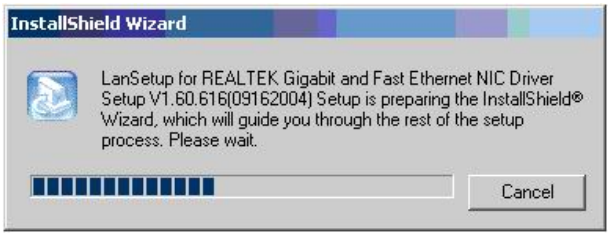
4.4 Install Ethernet Driver (For Realtek RTL810x, RTL813x Family)

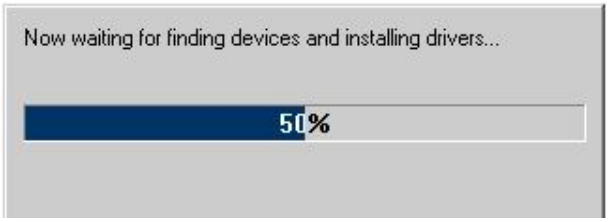
Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to \Driver_Network\Realtek\ RTL810x_813X Family.

Note: The installation procedures and screen shots in this section are based on Windows XP operation system.

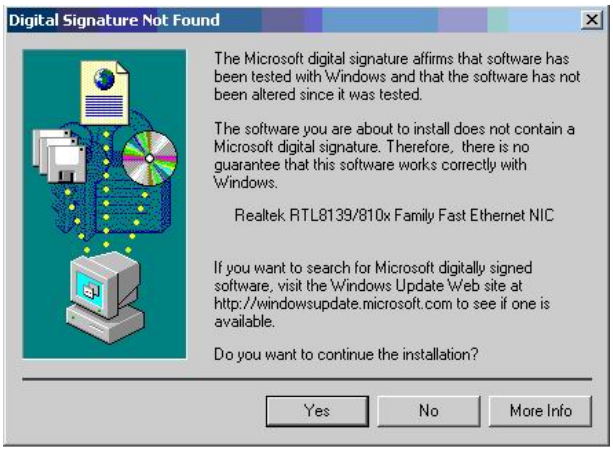


Step 1. Locate \Driver_Network\Realtek\ RTL810x_813X Family\Setup.exe.

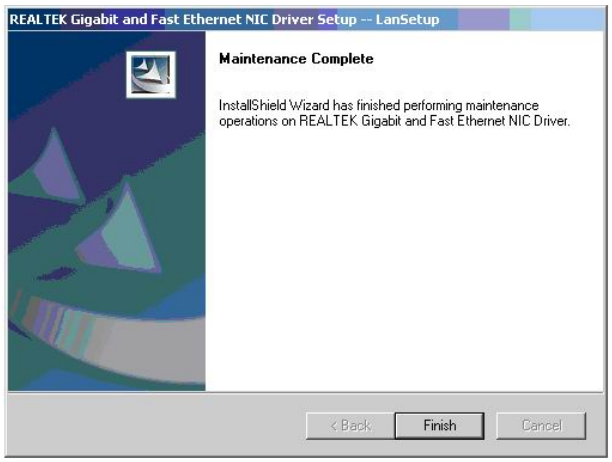




Step 2. Setup executing.

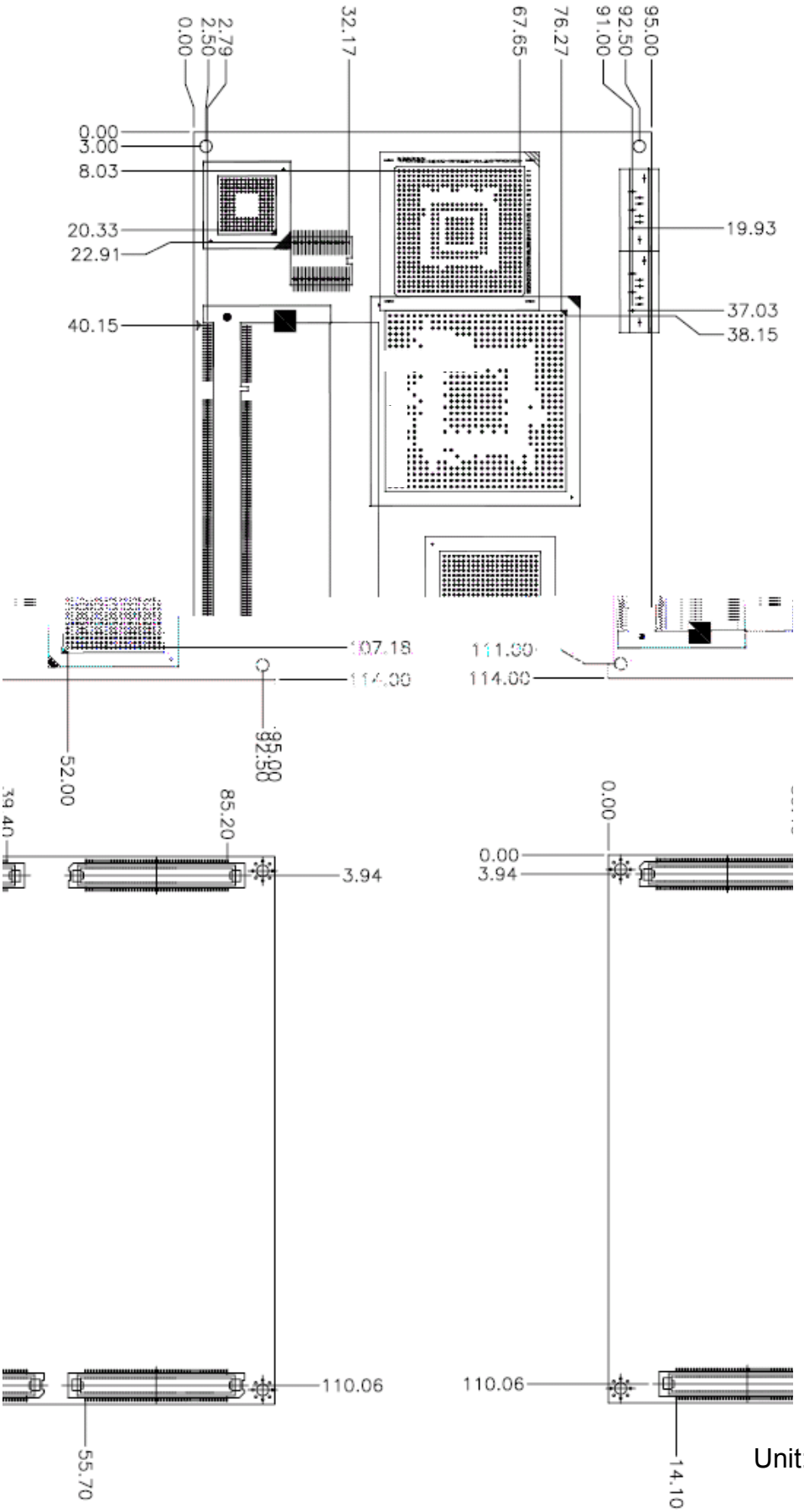


Step 3. Click **Yes** to continue the installation.



Step 4. Click **Finish** to complete the setup.

5 Measurement Drawing


0.00
2.79
2.50
32.17
67.65
76.27
91.00
92.50
95.00
0.00
3.00
8.03
20.33
22.91
40.15
19.93
37.03
38.15
107.18
111.00
114.00
52.00
85.20
3.94
0.00
110.06
55.70
14.10

Unit: mm

Appendix A: BIOS Revisions

BIOS Rev.

New Features

Bugs/Problems Solved

Known Problems

Appendix B: AWARD BIOS POST Messages

Overview

During the Power On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.
If a message is displayed, it will be accompanied by:
PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

Post Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and the EISA BIOS.

1. CMOS BATTERY HAS FAILED

CMOS battery is no longer functional. It should be replaced.

2. CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

3. DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

4. DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

5. DISPLAY SWITCH IS SET INCORRECTLY

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

6. DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

7. EISA Configuration Checksum Error
PLEASE RUN EISA CONFIGURATION UTILITY

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the card is installed firmly in the slot.

8. EISA Configuration Is Not Complete
PLEASE RUN EISA CONFIGURATION UTILITY

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

9. ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

10. ERROR INITIALIZING HARD DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

11. FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

12. Invalid EISA Configuration

PLEASE RUN EISA CONFIGURATION UTILITY

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

13. KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

14. Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

15. Memory parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

16. MEMORY SIZE HAS CHANGED SINCE LAST BOOT

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

17. Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

18. OFFENDING ADDRESS NOT FOUND

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

19. OFFENDING SEGMENT:

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

20. PRESS A KEY TO REBOOT

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

21. PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

22. RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

23. Should Be Empty But EISA Board Found
PLEASE RUN EISA CONFIGURATION UTILITY

A valid board ID was found in a slot that was configured as having no board ID.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

24. Should Have EISA Board But Not Found
PLEASE RUN EISA CONFIGURATION UTILITY

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

25. Slot Not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

26. SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT ...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

27. Wrong Board In Slot
PLEASE RUN EISA CONFIGURATION UTILITY

The board ID does not match the ID stored in the EISA non-volatile memory.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

28. FLOPPY DISK(S) fail (80) → Unable to reset floppy subsystem.
29. FLOPPY DISK(S) fail (40) → Floppy Type dismatch.
30. Hard Disk(s) fail (80) → HDD reset failed.
31. Hard Disk(s) fail (40) → HDD controller diagnostics failed.
32. Hard Disk(s) fail (20) → HDD initialization error.
33. Hard Disk(s) fail (10) → Unable to recalibrate fixed disk.
34. Hard Disk(s) fail (08) → Sector Verify failed.
35. Keyboard is locked out - Unlock the key.

BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

36. Keyboard error or no keyboard present.

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

37. Manufacturing POST loop.

System will repeat POST procedure infinitely while the P15 of keyboard controller is pull low. This is also used for M/B burn in test.

38. BIOS ROM checksum error - System halted.

The checksum of ROM address F0000H-FFFFFH is bad.

39. Memory test fail.

BIOS reports the memory test fail if the onboard memory is tested error.

40. POST Codes

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.

POST (hex)	Description
15h	Reserved
16h	Initial Early_Init_Onboard_Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0.
24h	Reserved
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed. 5. Invoke video BIOS.
2Ah	Reserved
2Bh	Reserved
2Ch	Reserved

POST (hex)	Description
2Dh	1. Initialize multi-language 1. Put information on screen display, including Award title, CPU type, CPU speed ….
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	Reserved
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program writes allocation for AMD K5 CPU.
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved
4Eh	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
4Fh	Reserved
50h	Initialize USB

POST (hex)	Description
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to “AUTO”.
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved

POST (hex)	Description
73h	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive. -ALT+F2 is pressed
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..
76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported. -If errors occur, report errors & wait for keys -If no errors occur or F1 key is pressed to continue: ◆Clear EPA or customization logo.
80h	Reserved
81h	Reserved
82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code

POST (hex)	Description
94h	1. Enable L2 cache 1. Program boot up speed 2. Chipset final initialization. 3. Power management final initialization 4. Clear screen & display summary table 5. Program K6 write allocation 6. Program P6 class write combining
95h	1. Program daylight saving 1. Update keyboard LED & typematic rate
96h	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)