ESM-945GSX

Intel® 945GSE Intel® Atom™ processor N270 ETX Module

User's Manual

1st Ed – 17 August 2009

Part No. E2047274900R

FCC Statement

THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

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1. Collect all the information about the problem encountered. (For example, CPU type and speed, Avalue's products model name, hardware & BIOS revision number, other hardware and software used, etc.) Note anything abnormal and list any on-screen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information available.
3. If your product is diagnosed as defective, obtain an RMA (return material authorization) number from your dealer. This allows us to process your good return more quickly.
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5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Contents

1. Getting Started

1.1 Safety Precautions

Warning!

Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!

Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

1.2 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 x ESM-945GSX Intel® 945GSE Atom N270 ETX Module
- 1 x Quick Installation Guide
- 1 x DVD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Audio drivers and utilities

If any of the above items is damaged or missing, contact your retailer.

1.3 Document Amendment History

Revision	Date	Comment
1st	August. 2009	Initial Release

1.4 Manual Objectives

This manual describes in detail the Avalue Technology ESM-945GSX Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with ESM-945GSX series or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings (see the description of the Jumper Settings for details).

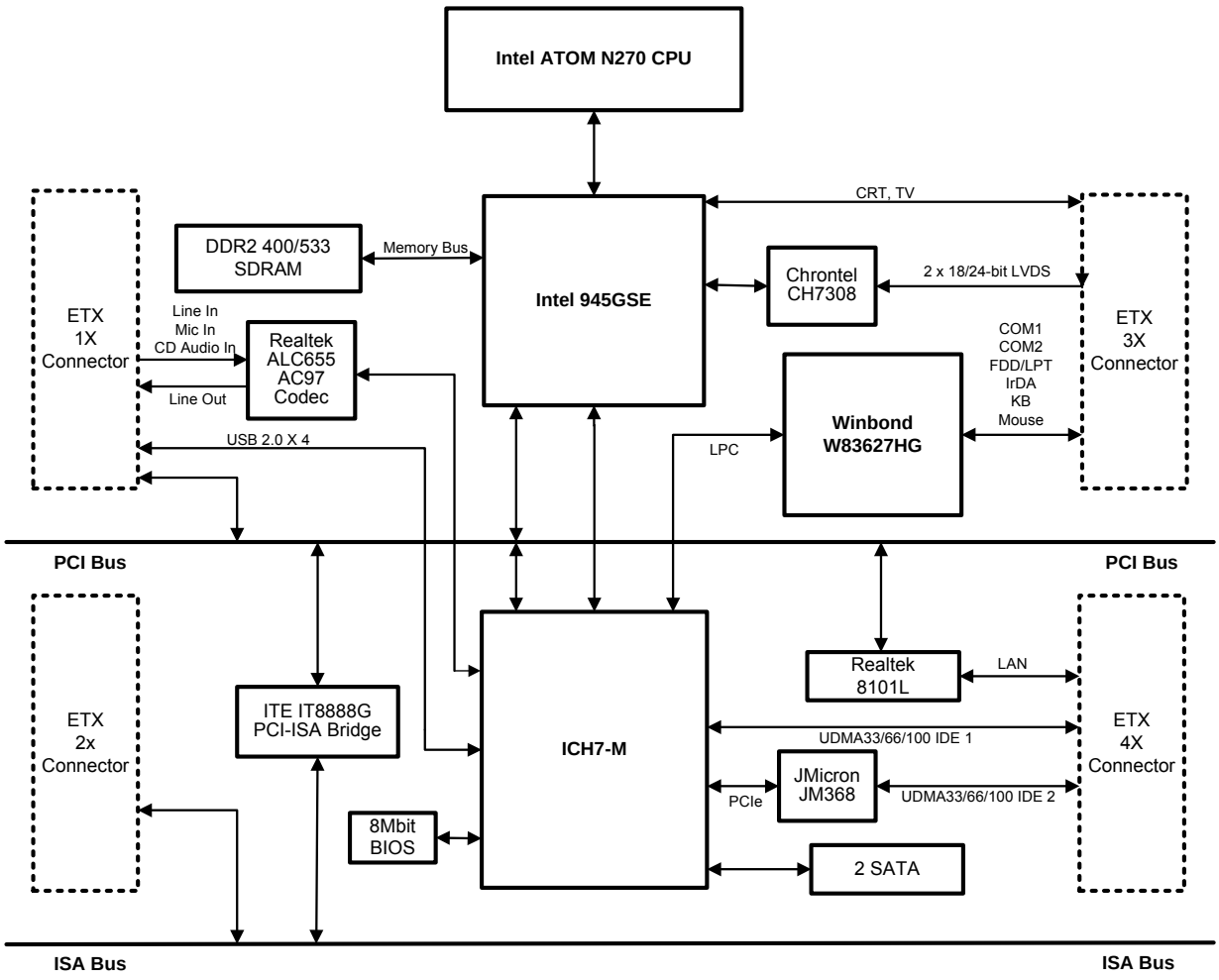
If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

1.5 System Specifications

System	
CPU	Onboard Intel® Atom™ processor N270 1.6 GHz CPU
BIOS	Award 8 Mbit Flash BIOS
System Chipset	Intel® 945GSE / ICH7-M
System Memory	One 200-pin SODIMM socket supports up to 2 GB DDR2 SDRAM, supports 400/533 MHz
Watchdog Timer	Reset: 1~65535 sec./min and 1 sec. or 1 min./step
Expansion	4 PCI, 1 ISA Bus
I/O	
MIO	2 x EIDE, 2 x SATA, 1 x FDD/LPT, 2 x TTL Serial, 1 x K/B & Mouse
USB	4 x USB 2.0 ports
IrDA	115k bps, IrDA 1.0 compliant
Display	
Chipset	Intel® 945GSE Integrated
Display Memory	Intel® DVMT 3.0 Supports up to 224 MB shared video memory
Resolution	CRT mode: 2048 x 1536 @ 75 Hz LCD/ Simultaneous mode: 1600 x 1200 @ 60 Hz
Multiple Display	CRT + LVDS, CRT + TV, LVDS + TV
LVDS Interface	Dual-channel 18/ 24-bit LVDS
TV-out	Intel® 945GSE Integrated TV-out interface supports HDTV
Audio	
Chipset	Intel® ICH7-M
AC97 Codec	Realtek ALC655
Audio Interface	Line in, Line out & Mic in
Ethernet	
LAN	Realtek RTL8101L
Ethernet Interface	10/ 100 Base-Tx Fast Ethernet compatible
Mechanical & Environmental	
Power Requirement	+5V, +5Vsb (for ATX only)
Power Type	AT/ ATX
Operation Temperature	0~60°C (32~140°F)
Operating Humidity	0%~90% relative humidity, non-condensing
Size (L x W)	4.5" x 3.7" (114 mm x 95 mm)
Weight	0.44 lbs (0.2 Kg)

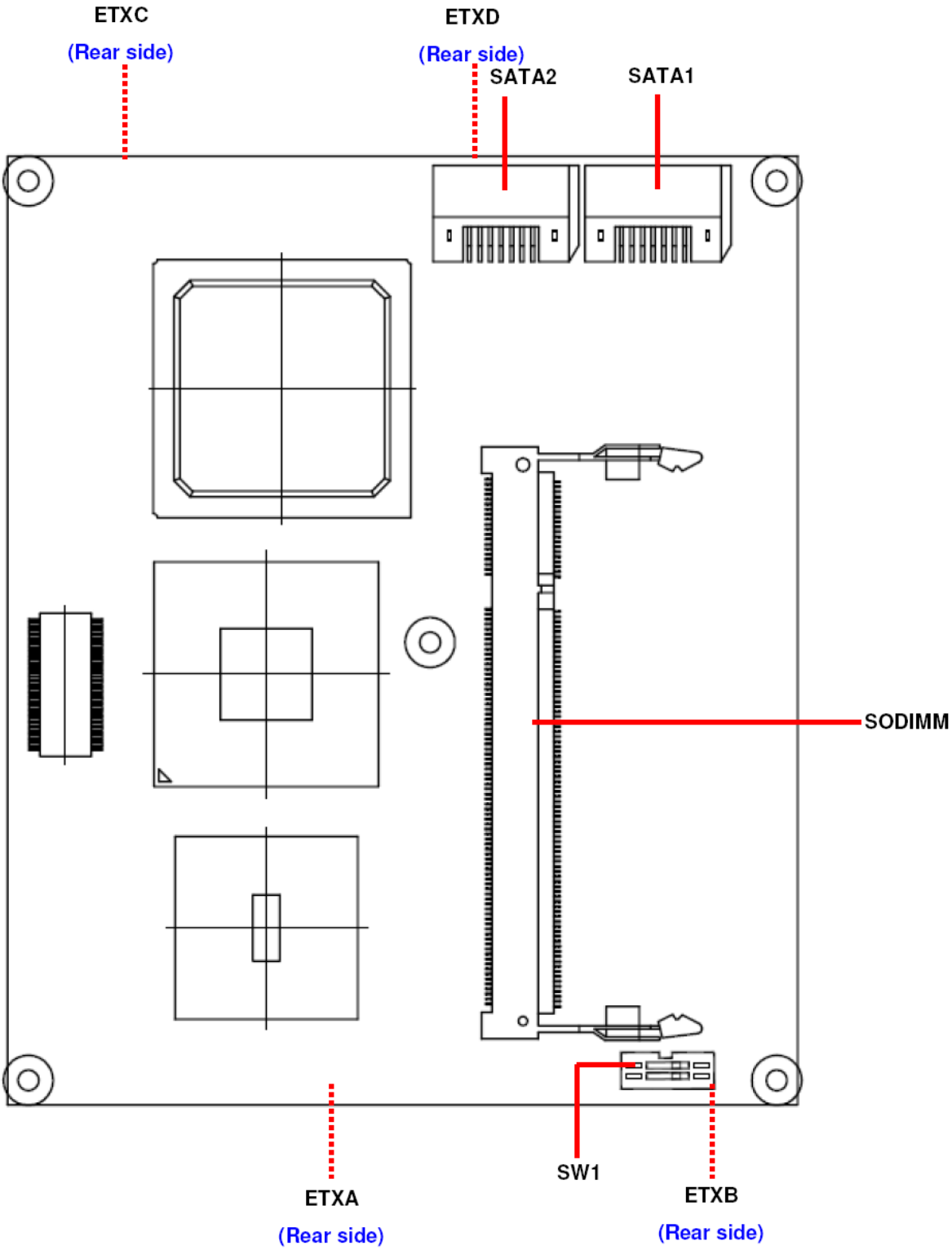
1.6 Architecture Overview – Block Diagram

The following block diagram shows the architecture and main components of ESM-945GSX.



2. Hardware Configuration

2.1 Product Overview



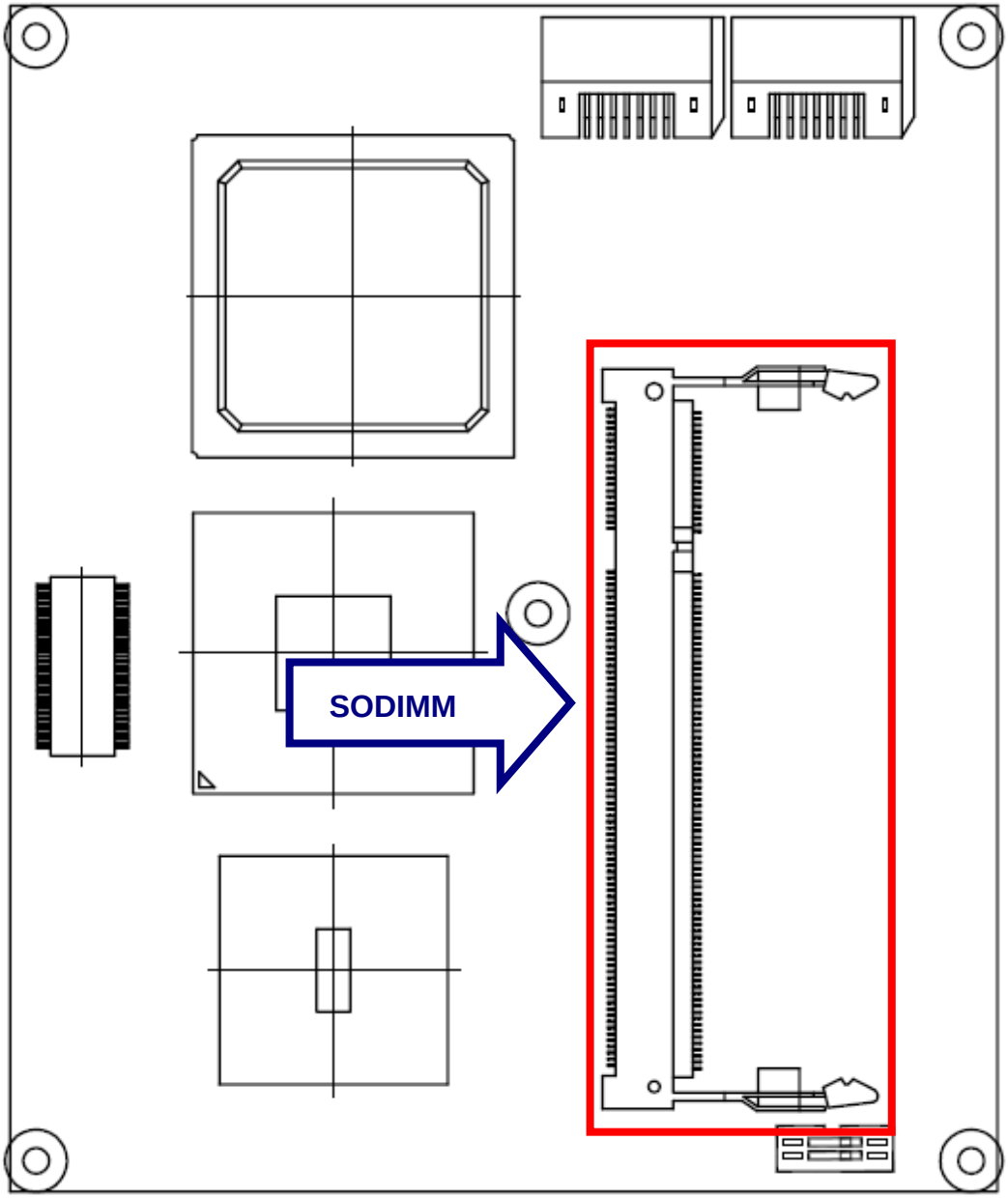
2.2 Installation Procedure

This chapter explains you the instructions of how to setup your system.

1. Turn off the power supply.
2. Insert the SODIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the ATXPWR.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the “LOAD BIOS DEFAULTS” feature. The ***Integrated Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilized, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

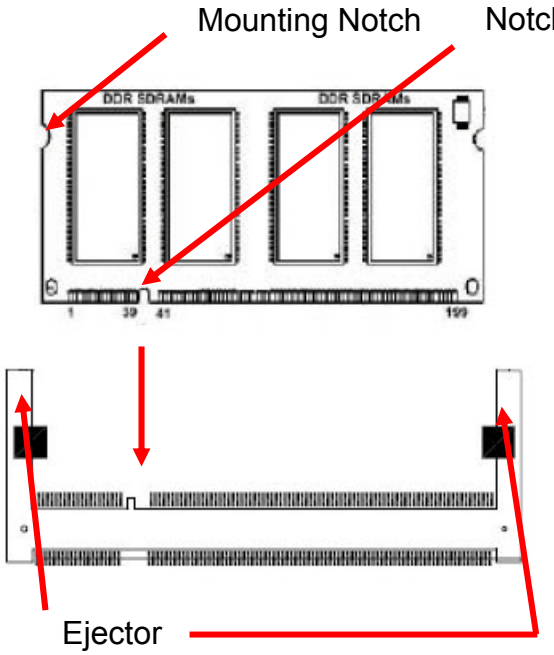
2.2.1 Main Memory

ESM-945GSX provides one 200-pin SODIMM sockets to support DDR2 SDRAM. The total maximum memory size is 2GB.



Make sure to unplug the power supply before adding or removing SODIMMs or other system components. Failure to do so may cause severe damage to both the board and the components.

- Locate the SODIMM socket on the board.
- Hold two edges of the SODIMM module carefully. Keep away of touching its connectors.
- Align the notch key on the module with the rib on the slot.
- Firmly press the modules into the socket automatically snaps into the mounting notch. Do not force the SODIMM module in with extra force as the SODIMM module only fit in one direction.



200-pin DDR2 SODIMM

- To remove the SODIMM modules, push the two ejector tabs on the slot outward simultaneously, and then pull out the SODIMM module.

Note:

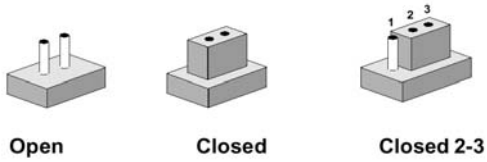
(1) Please do not change any DDR2 SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.

(2) Static electricity can damage the electronic components of the computer or optional boards. Before starting these procedures, ensure that you are discharged of static electricity by touching a grounded metal object briefly.

2.3 Jumper and Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip. To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:

A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

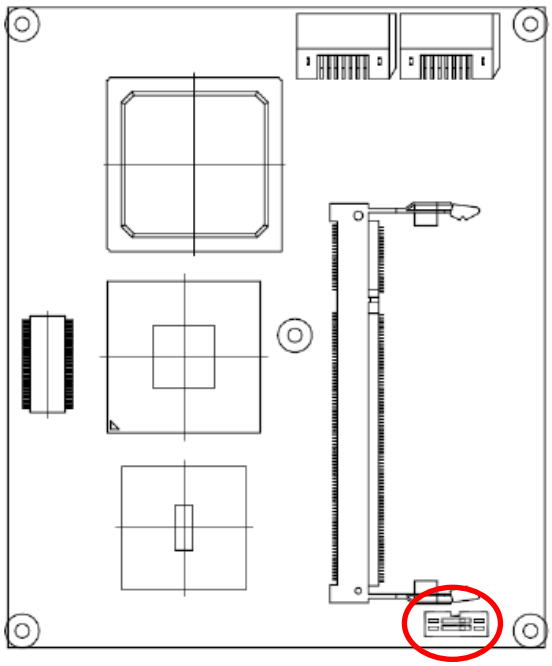
The following tables list the function of each of the board's jumpers and connectors.

Connectors

Label	Function	Note
SATA1	Serial ATA connector 1	
SATA2	Serial ATA connector 2	
SODIMM	200-pin DDR2 SODIMM socket	
SW1	AT/ATX Power Input type/ power on mode select	
ETXA	ETX connector 1	HIROSE FX8-100P-SV
ETXB	ETX connector 2	HIROSE FX8-100P-SV
ETXC	ETX connector 3	HIROSE FX8-100P-SV
ETXD	ETX connector 4	HIROSE FX8-100P-SV

2.4 Setting Jumpers & Connectors

2.4.1 AT/ATX Power Input type/ power on mode select (SW1)



1 2 on

*Default

AT/ATX Power Input type

AT type

OFF	1		⇨	ON
	2			

ATX type*

OFF	1	⇦		ON
	2			

AT/ATX power on mode

AT power on mode

OFF	1			ON
	2		⇨	

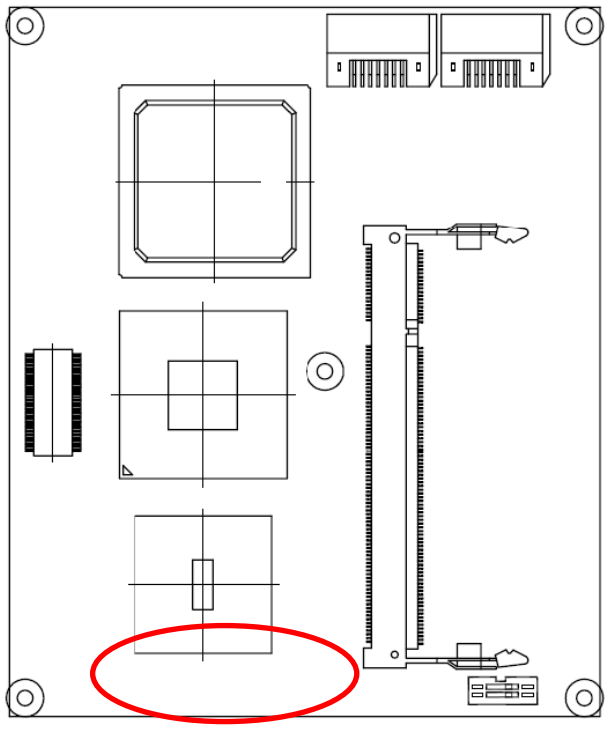
ATX power on mode*

OFF	1			ON
	2	⇦		

2.4.1.1 Signal Description –AT/ATX Power Input type/ power on mode select

Input power type/ Power-ON Mode	Description
AT type/ AT Mode 	Use AT type power input, and set the board in AT mode.
AT type/ ATX Mode 	Use AT type power input, and set the board in ATX mode.
ATX type/ AT Mode 	Use ATX type power input, and set the board in AT mode.
ATX type/ ATX Mode 	Use ATX type power input, and set the board in ATX mode.

2.4.2 ETX Connector X1 (ETXA)



(Rear side)

Signal	PIN	PIN	Signal
GND	A1	A2	GND
PCICLK3	A3	A4	PCICLK4
GND	A5	A6	GND
PCICLK1	A7	A8	PCICLK2
REQ#3	A9	A10	GNT#3
GNT#2	A11	A12	+3V
REQ#2	A13	A14	GNT#1
REQ#1	A15	A16	+3V
GNT#0	A17	A18	NC
+5V	A19	A20	+5V
SERIRQ	A21	A22	REQ#0
AD0	A23	A24	+3V
AD1	A25	A26	AD2
AD4	A27	A28	AD3
AD6	A29	A30	AD5
CBE#0	A31	A32	AD7
AD8	A33	A34	AD9
GND	A35	A36	GND
AD10	A37	A38	AUXAL
AD11	A39	A40	MIC
AD12	A41	A42	AUXAR
AD13	A43	A44	ASVCC
AD14	A45	A46	SNDL
AD15	A47	A48	ASGND
CBE#1	A49	A50	SNDR
+5V	A51	A52	+5V
PAR	A53	A54	SERR#
PERR#	A55	A56	NC
PME#	A57	A58	USB2-
LOCK#	A59	A60	DEVSEL#

Signal	PIN	PIN	Signal
TRDY#	A61	A62	USB3-
IRDY#	A63	A64	STOP#
FRAME#	A65	A66	USB2+
GND	A67	A68	GND
AD16	A69	A70	CBE#2
AD17	A71	A72	USB3+
AD19	A73	A74	AD18
AD20	A75	A76	USB0-
AD22	A77	A78	AD21
AD23	A79	A80	USB1-
AD24	A81	A82	CBE#3
+5V	A83	A84	+5V
AD25	A85	A86	AD26
AD28	A87	A88	USB0+
AD27	A89	A90	AD29
AD30	A91	A92	USB1+
PCIRST#	A93	A94	AD31
INTR#C	A95	A96	INTR#D
INTR#A	A97	A98	INTR#B
GND	A99	A100	GND

2.4.3 Signal Description – ETX Connector X1 (ETXA)

2.4.3.1 PCI Signals

Signal	Signal Description
PCICLK [1:4]	*PCI clock outputs* for up to 4 external PCI slots or devices. The baseboard designer should route these clocks for 1300pS total delay from the ETX connector pin to the clock pin of the PCI device. See the ETX Design Guide for typical route length calculations.
REQ [0:3]#	*Bus Request signals* for up to 4 external bus mastering PCI devices. When asserted, a PCI device is requesting PCI bus ownership from the arbiter.
GNT [0:3]#	*Grant signals* to PCI Masters. When asserted by the arbiter, the PCI master has been granted ownership of the PCI bus.
AD [0:31]	*PCI Address and Data Bus Lines*. These lines carry the address and data information for PCI transactions.
CBE [0:3]#	*PCI Bus Command and Byte Enables.* Bus command and byte enables are multiplexed in these lines for address and data phases, respectively.
PAR	*Parity bit* for the PCI bus. Generated as even parity across AD [31:0] and CBE [3:0]#.
SERR#	*System Error.* Asserted for hardware error conditions such as parity errors detected in DRAM.
PERR#	*Parity Error.* For PCI operation per exception granted by PCI 2.1 Specification.
LOCK#	*Lock Resource Signal.* This pin indicates that either the PCI master or the bridge intends to run exclusive transfers.
DEVSEL#	*Device Select*. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.
TRDY#	*Target Ready*. This pin indicates that the target is ready to complete the current data phase of a transaction.
IRDY#	*Initiator Ready.* This signal indicates that the initiator is ready to complete the current data phase of a transaction.
STOP#	*Stop.* This signal indicates that the target is requesting that the master stop the current transaction.
FRAME#	*Cycle Frame* of PCI Buses. This indicates the beginning and duration of a PCI access. The access will be either an output driven by the Northbridge on behalf of the CPU, or an input during PCI master access.
PCIRST#	*PCI Bus Reset*. This is an output signal to reset the entire PCI Bus. This signal is asserted during system reset.
INTRA#, INTRB#, INTRC#, INTRD#	*PCI interrupts.* These interrupts are sharable and are typically wired in rotation to PCI slots or devices.
IDSEL	This pin is not present on the ESM-945ETX/945ETX module connector, but it is present on each PCI slot connector or device. IDSEL is an input to the device that is used to set the device's configuration address for PCI configuration cycles. The IDSEL pin of each device is typically connected to one of the AD lines in order to set a unique configuration address. In ETX systems, the four external bus slots or devices are assumed to use AD[19:22] for IDSEL connections.
PME#	Power management event..

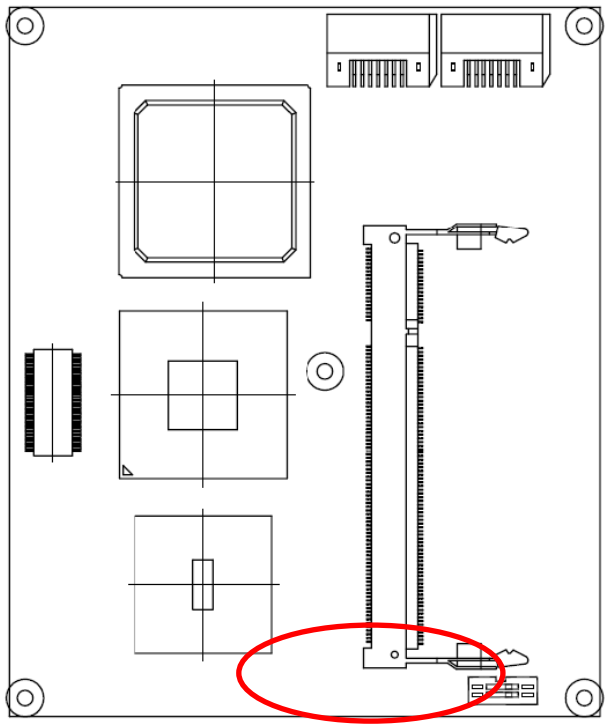
2.4.3.2 Audio Signals

Signal	Signal Description
SNDL/ SNDR	*Line-level stereo output left/ right.* These outputs have a nominal level of 1 volt RMS into a 10K impedance load. These outputs cannot drive low-impedance speakers directly.
AUXAL/ AUXAR	*Auxiliary A input left/ right.* Normally intended for connection to an internal or external CDROM analog output or a similar line-level audio source. Minimum input impedance is 5KOhm. Nominal input level is 1 volt RMS.
MIC	*Microphone input*. Minimum input impedance is 5KOhm, max. Input voltage is 0.15 Vp-p.
ASGND	*Analog ground for sound controller.* Use this signal ground for an external amplifier in order to achieve lowest audio noise levels.
ASVCC	*Analog supply voltage for sound controller.* This is an output which is used for production test only. Do not make external connections to this pin.

2.4.3.3 USB Signals

Signal	Signal Description
USB [0:3]	*Universal Serial Bus* Port [0:3] positive signal. These are the serial data pairs for USB Port N-and Port N#.
USB [0:3]-	*Universal Serial Bus* Port [0:3] negative signal. These are the serial data pairs for USB Port N-and Port N#.

2.4.4 ETX Connector X2 (ETXB)



(Rear side)

Signal	PIN	PIN	Signal
GND	B1	B2	GND
SD14	B3	B4	SD15
SD13	B5	B6	MASTER#
SD12	B7	B8	DREQ7
SD11	B9	B10	DACK#7
SD10	B11	B12	DREQ6
SD9	B13	B14	DACK#6
SD8	B15	B16	DREQ5
MEMW#	B17	B18	DACK#5
MEMR#	B19	B20	DREQ0
LA17	B21	B22	DACK#0
LA18	B23	B24	IRQ14
LA19	B25	B26	IRQ15
LA20	B27	B28	IRQ12
LA21	B29	B30	IRQ11
LA22	B31	B32	IRQ10
LA23	B33	B34	IO16#
GND	B35	B36	GND
SBHE#	B37	B38	M16#
SA0	B39	B40	OSC
SA1	B41	B42	BALE
SA2	B43	B44	TC
SA3	B45	B46	DACK#2
SA4	B47	B48	IRQ3
SA5	B49	B50	IRQ4
+5V	B51	B52	+5V
SA7	B53	B54	IRQ5
SA8	B55	B56	IRQ6
SA9	B57	B58	IRQ7
SA10	B59	B60	SYSCLK

Signal	PIN	PIN	Signal
SA10	B61	B62	REFCH#
SA11	B63	B64	DREQ1
SA12	B65	B66	DACK#1
GND	B67	B68	GND
SA13	B69	B70	DREQ3
SA14	B71	B72	DACK#3
SA15	B73	B74	IOR#
SA16	B75	B76	IOW#
SA18	B77	B78	SA17
SA19	B79	B80	SMEMR#
IOCHRDY	B81	B82	AEN
+5V	B83	B84	+5V
SD0	B85	B86	SMEMW#
SD2	B87	B88	SD1
SD3	B89	B90	NOWS#
DREQ2	B91	B92	SD4
SD5	B93	B94	IRQ9
SD6	B95	B96	SD7
IOCHK#	B97	B98	RSTDRV
GND	B99	B100	GND

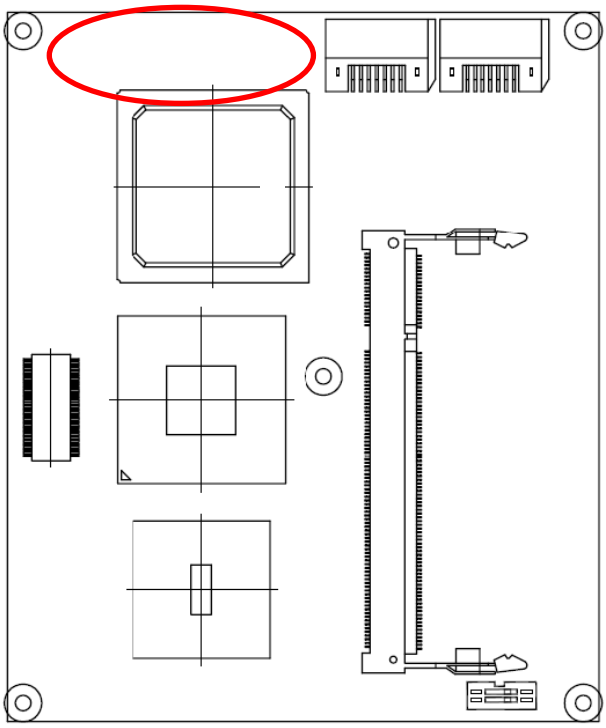
2.4.5 Signal Description – ETX Connector X2 (ETXB)

2.4.5.1 ISA Signals

Signal	Signal Description
SD[0:15]	These signals provide data bus bits 0 to 15 for any peripheral devices. All 8-bit devices use SD[0:7] for data transfers. 16-bit devices use SD[0:15]. To support 8-bit devices, the data on SD[8:15] is gated to SD[0:7] during 8-bit transfers to these devices. 16-bit CPU cycles will be automatically converted into two 8-bit cycles for 8-bit peripherals.
SA[0:19]	Address bits 0 through 15 are used to address I/O devices. Address bits 0 through 19 are used to address memory within the system. These 20 address lines, in addition to LA[17:23] allow access of up to 16MB of memory. SA[0:19] are gated on the ISA-bus when BALE is high and latched on to the falling edge of BALE.
SBHE#	*Bus High Enable* indicates a data transfer on the upper byte of the data bus SD[8:15]. 16-bit I/O devices use SBHE# to enable data bus buffers on SD[8:15].
BALE	BALE is an active-high pulse generated at the beginning of any bus cycle initiated by a CPU module. It indicates when the SA[0:19], LA17.23, AEN, and SBHE# signals are valid.
AEN	AEN is an active-high output that indicates a DMA transfer cycle. Only resources with a active DACK# signal should respond to the command lines when AEN is high.
MEMR#	MEMR# instructs memory devices to drive data onto the data bus. MEMR# is active for all memory read cycles.
SMEMR#	SMEMR# instructs memory devices to drive data onto the data bus. SMEMR# is active for memory read cycles to addresses below 1MB.
MEMW#	MEMW# instructs memory devices to store the data present on the data bus. MEMW# is active for all memory write cycles.
SMEMW#	SMEMW# instructs memory devices to store the data present on the data bus. SMEMW# is active for all memory write cycles to address below 1MB.
IOR#	I/O read instructs an I/O device to drive its data onto the data bus. It may be driven by the CPU or by the DMA controller. IOR# is inactive (high) during refresh cycles.
IOW#	I/O write instructs an I/O device to store the data present on the data bus. It may be driven by the CPU or by the DMA controller. IOW# is inactive (high) during refresh cycles.
IOCHK#	IOCHK# is an active-low input signal that indicates that an error has occurred on the module bus. If I/O checking is enabled on the CPU module, an IOCHK# assertion by a peripheral device sends a NMI to the processor.
IOCHRDY	The I/O Channel Ready is pulled low in order to extend the read or write cycles of any bus access when required. The CPU, DMA controllers or refresh controller can initiate the cycle. Any peripheral that cannot present read data or strobe in write data within this amount of time use IOCHRDY to extend these cycles. This signal should not be held low for more than 2.5 µs for normal operation. Any extension to more than 2.5 µs does not guarantee proper DRAM memory content due to the fact that memory refresh is disabled while IOCHRDY is low.
M16#	The M16# signal determines when a 16-bit to 8-bit conversion is needed for memory bus cycles. A conversion is done any time the CPU module requests a 16-bit memory cycle while the M16# line is high. If M16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If M16# is low, an access to peripherals is done 16 bits wide.
IO16#	The IO16# signal determines when a 16-bit to 8-bit conversion is needed for I/O bus cycles. A conversion is done any time the CPU module requests a 16-bit I/O cycle while the IO16# line is high. If IO16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If IO16# is low, an access to peripherals is done at 16 bit width.

Signal	Signal Description
REFSH#	REFSH# is pulled low whenever a refresh cycle is initiated. A refresh cycle is activated every 15.6 us in order to prevent loss of DRAM data.
NOWS#	The Zero wait state signal tells the CPU to complete the current bus cycle without inserting the default wait states. By default the CPU inserts 4 wait states for 8-bit transfers and 1 wait state for 16-bit transfers.
MASTER#	This signal is used with a DRQ line to gain control of the system bus. A processor or a DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DACK#. Upon receiving the DACK#, a bus master may pull MASTER# low, which will allow it to control the system address, data and control lines. After MASTER# is low, the bus master must wait one system clock period before driving the address and data lines, and two clock periods before issuing a read or write command. If this signal is held low for more than 15 us, system memory may be lost as memory refresh is disabled during this process.
SYSCLK	SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with a duty cycle of 40-60 percent. The frequency supplied by different CPU modules may vary. This signal is supplied at all times except when the CPU module is in sleep mode.
OSC	OSC is supplied by the CPU module. It has a nominal frequency of 14.31818 MHz and a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.
RESETDRV	This active-high output is system reset generated from CPU modules. It is responsible for resetting external devices.
DREQ [0, 1, 2, 3, 5, 6, 7]	The asynchronous DMA request inputs are used by external devices to indicate when they need service from the CPU modules DAM controllers. DREQ0..3 are used for transfers between 8-bit I/O adapters and system memory. DREQ5..7 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pull-up resistors on the CPU modules.
DACK [0, 1, 2, 3, 5, 6, 7]#	DMA acknowledge 0..3 and 5.7 are used to acknowledge DMA requests. They are active-low.
TC	The active-high output TC indicates that one of the DMA channels has transferred all data.
IRQ [3:7, 9,15]	These are the asynchronous interrupt request lines. IRQ0, 1, 2 and 8 are not available as external interrupts because they are used internally on the CPU module. All IRQ signals are active-high. The interrupt requests are prioritized. IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest). IRQ3 through IRQ7 have the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt service routine).

2.4.6 ETX Connector X3 (ETXC)



(Rear side)

Signal	PIN	PIN	Signal
GND	C1	C2	GND
R	C3	C4	B
HSY	C5	C6	G
VSY	C7	C8	DDCK
DETECT#	C9	C10	DDDA
LCD16/B4	C11	C12	LCD18/SHFCLK
LCD17/B5	C13	C14	LCD19/EN
GND	C15	C16	GND
LCD13/B1	C17	C18	LCD15/B3
LCD12/B0	C19	C20	LCD14/B2
GND	C21	C22	GND
LCD8/G2	C23	C24	LCD11/G5
LCD9/G3	C25	C26	LCD10/G4
GND	C27	C28	GND
LCD4/R4	C29	C30	LCD7/G1
LCD5/R5	C31	C32	LCD6/G0
GND	C33	C34	GND
LCD1/R1	C35	C36	LCD3/R3
LCD0/R0	C37	C38	LCD2/R2
+5V	C39	C40	+5V
JILI_DAT	C41	C42	LTGIO0/VSYNC
JILI_CLK	C43	C44	BLON#
BIASON/HSYNC	C45	C46	DIGON
COMP	C47	C48	Y
SYNC	C49	C50	C
LPT/FLPY#	C51	C52	NC
+5V	C53	C54	GND
STB#/I.C	C55	C56	AFD#/DENSEL
NC	C57	C58	PD7/NC
IRRX	C59	C60	ERR#/HDSEL#

Signal	PIN	PIN	Signal
IRTX	C61	C62	PD6/NC
RXD2	C63	C64	INIT#/DIR#
GND	C65	C66	GND
RTS#2	C67	C68	PD5/NC
DTR#2	C69	C70	SLIN#/STEP#
DCD#2	C71	C72	PD4/DSKCHG#
DRS#2	C73	C74	PD3/RDATA#
CTS#2	C75	C76	PD2/WP#
TXD#2	C77	C78	PD1/TRK0#
RI#2	C79	C80	PD0/INDEX#
+5V	C81	C82	+5V
RXD1	C83	C84	ACK#/DRV
RTS#1	C85	C86	BUSY#/MOT
DTR#1	C87	C88	PE/WDATA#
DCD#1	C89	C90	SLCT#/WGATE#
DRS#1	C91	C92	MSCLK
CTS#1	C93	C94	MSDAT
TXD#1	C95	C96	KBCLK
RI#1	C97	C98	KBDAT
GND	C99	C100	GND

2.4.7 Signal Description – ETX Connector X3 (ETXC)

2.4.7.1 LVDS Flat Panel Interface Signals

Signal	1 Pixel / Clock LVDS Mode	2 Pixel / Clock LVDS Mode
LCDDO0	Txout0#	Odd Txout0#
LCDDO1	Txout0	Odd Txout0
LCDDO2	Txout1#	Odd Txout1#
LCDDO3	Txout1	Odd Txout1
LCDDO4	Txout2#	Odd Txout2#
LCDDO5	Txout2	Odd Txout2
LCDDO6	Txclk#	Odd Txclk#
LCDDO7	Txclk	Odd Txclk
LCDDO8	Txout3#	Odd Txout3#
LCDDO9	Txout3	Odd Txout3
LCDDO10	-	Even Txout0#
LCDDO11	-	Even Txout0
LCDDO12	-	Even Txout1#
LCDDO13	-	Even Txout1
LCDDO14	-	Even Txout2#
LCDDO15	-	Even Txout2
LCDDO16	-	Even Txclk#
LCDDO17	-	Even Txclk
LCDDO18	-	Even Txout3#
LCDDO19	-	Even Txout3
BIASON	Controls panel contrast voltage.	
DIGON	Controls panel digital power.	
ENBKL#	Controls backlight power enable.	
I^2C_DAT, I^2C_CLK	I^2C interface for panel parameter EEPROM. This EERPOM is mounted on the LVDS receiver. The data in the EEPROM allows the EXT module to automatically set the proper timing parameters for a specific LCD panel.	

2.4.7.2 IrDA (SIR) Signals

Signal	Signal Description
IRTX, IRRX	Infrared transmit and receive pins.

2.4.7.3 Parallel Port Signals

Signal	Signal Description
STB#	This active-low signal is used to strobe the printer data into the printer.
AFD#	This active-low output tells the printer to automatically feed the next single line after each preceding line has been printed.
PD[0:7]	This bi-directional parallel data bus is used to transfer information between the CPU and the peripherals.
ERR#	This active-low signal indicates an error situation has occurred at the printer.
INIT#	This active-low signal is used to initiate the printer when low.
SLIN#	This active-low signal selects the printer.
ACK#	This active-low output from the printer indicates that it has received the previous data and that it is ready to receive new data.

2.4.7.4 PS/2 Keyboard and Mouse Signals

Signal	Signal Description
KBDAT	Bi-directional keyboard data signal.
KBCLK	Keyboard clock signal.
MSDAT	Bi-directional mouse data signal.
MSCLK	Mouse clock signal.

2.4.7.5 Serial Port Signals

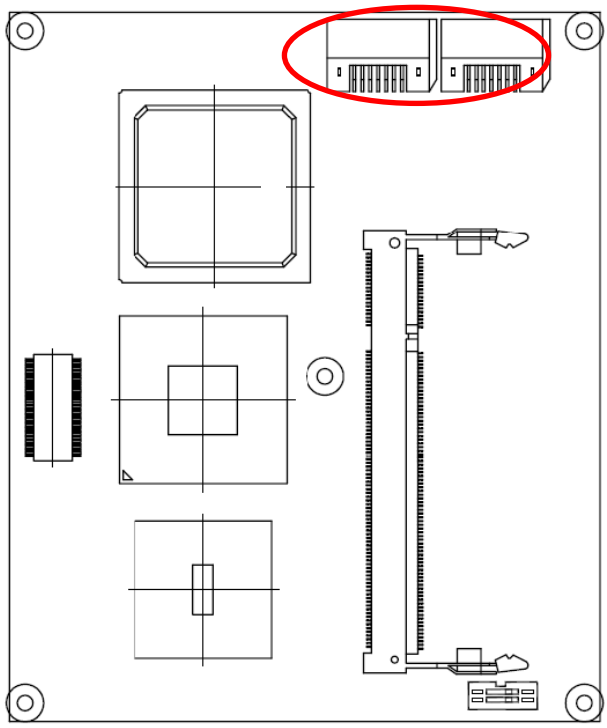
Note that all serial port signals on ESM-945ETX/945ETX connectors are logic level signals. External transceiver devices are necessary for the conversion of the logic level signals to the desired physical interface such as RS232, RS422, or RS485.

Signal	Signal Description
DTR1#, DTR2#	Active-low data terminal ready outputs for the serial port. Handshake output signal notifies the modem that the UART is ready to establish a data communication link.
RI1#, RI2#	Active-low input is for the serial port. Handshake signals notify the UART when a telephone ring signal is detected by the modem.
TXD1, TXD2	Transmitter serial data output from serial port.
RXD1, RXD2	Receiver serial data input.
CTS1#, CTS2#	Active-low input for serial ports. Handshake signals notify the UART when the modem is ready to receive data.
RTS1#, RTS2#	Active-low output for serial port. Handshake signals notify the modem when the UART is ready to transmit data.
DCD1#, DCD2#	Active-low input for serial port. Handshake signals notify the UART when a carrier signal is detected by the modem.
DSR1#, DSR2#	This active-low input is for serial port. Handshake signals are use to notify the UART that the modem is ready to establish the communication link.

2.4.7.6 VGA Signals

Signal	Signal Description
HSY	*Horizontal Sync*: This output supplies the horizontal synchronization pulse to the CRT monitor.
VSY	*Vertical Sync*: This output supplies the vertical synchronization pulse to the CRT monitor.
R, G, B	Red, green and blue analog video output signals for CRT monitors. These lines should be terminated with 75 ohms to ground at the video connector.
DDCK, DDDA	These two pins can be used for a DDC interface between the graphics controller chip and the CRT monitor.

2.4.8 ETX Connector X4 (ETXD)



(Rear side)

Signal	PIN	PIN	Signal
GND	D1	D2	GND
5V_SB	D3	D4	PWGIN
PS_ON	D5	D6	SPEAKER
PWRBTN#	D7	D8	BATT
KBINH	D9	D10	LILED
RSMRST#	D11	D12	ACTLED
POMKBCS#	D13	D14	SPEEDLED
EXT_PRG	D15	D16	I2CLK
+5V	D17	D18	+5V
OVCR#	D19	D20	GPCS#
ESTSMI#	D21	D22	I2DAT
SMBCLK	D23	D24	SMBDAT
SIDE_CS3#	D25	D26	SMBALRT#
SIDE_CS1#	D27	D28	DASP_S
SIDE_A2	D29	D30	PIDE_CS3#
SIDE_A0	D31	D32	PIDE_CS1#
GND	D33	D34	GND
PDIAG_S	D35	D36	PIDE_A2
SIDE_A1	D37	D38	PIDE_A0
SIDE_INTRQ	D39	D40	PIDE_A1
BATLOW#	D41	D42	GPE1#
SIDE_ACK#	D43	D44	PIDE_INTRQ
SIDE_RDY	D45	D46	PIDE_ACK#
SIDE_IOR#	D47	D48	PIDE_RDY
+5V	D49	D50	+5V
SIDE_LOW#	D51	D52	PIDE_IOR#
SIDE_DRQ	D53	D54	PIDE_LOW#
SIDE_D15	D55	D56	PIDE_DRQ
SIDE_D0	D57	D58	PIDE_D15
SIDE_D14	D59	D60	PIDE_D0

Signal	PIN	PIN	Signal
SIDE_D1	D61	D62	PIDE_D14
SIDE_D13	D63	D64	PIDE_D1
GND	D65	D66	GND
SIDE_D2	D67	D68	PIDE_D13
SIDE_D12	D69	D70	PIDE_D2
SIDE_D3	D71	D72	PIDE_D12
SIDE_D11	D73	D74	PIDE_D3
SIDE_D4	D75	D76	PIDE_D11
SIDE_D10	D77	D78	PIDE_D4
SIDE_D5	D79	D80	PIDE_D10
+5V	D81	D82	+5V
SIDE_D9	D83	D84	PIDE_D5
SIDE_D6	D85	D86	PIDE_D9
SIDE_D8	D87	D88	PIDE_D6
GPE2#	D89	D90	PIDE_P#
RTD-	D91	D92	PIDE_D8
RTD+	D93	D94	SIDE_D7
TXD-	D95	D96	PIDE_D7
TXD+	D97	D98	HDRST#
GND	D99	D100	GND

2.4.9 Signal Description – ETX Connector X4 (ETXD)

2.4.9.1 Ethernet Signals

Signal	Signal Description
TXD#, TXD	Ethernet Transmit Differential Pair. These pins transmit the serial bit stream on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.
RXD#, RXD	Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer. The bit stream can be transmitted in either two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.
ACTLED	The Activity LED pin indicates either transmitted or received data activity on the Ethernet port. This pin is asserted low when activity is detected. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.
LILED	The Link Integrity LED pin indicates link integrity. This pin is asserted low when the link is valid. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.
SPEEDLED	The Speed LED pin indicates high speed operation. This LED is not supported by ESM-945ETX. This pin is asserted low when a 100Mbps link is detected, and is not asserted for a 10Mbps link. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.

2.4.9.2 IDE Signals

Signal	Signal Description
PIDE_D[0:15]/ SIDE_D[0:15]	IDE Data Bus.
PIDE_A[0:2]/ SIDE_A[0:2]	IDE Address Bus.
PIDE_CS1#/ SIDE_CS1#	IDE Chip Select 1. This is the Chip Select 1 command output pin that enables the IDE device to watch the Read/Write Command.
PIDE_CS3#/ SIDE_CS3#	IDE Chip Select 3. This is the Chip Select 3 command output pin that enables the IDE device to watch the Read/Write Command.
PIDE_DRQ/ SIDE_DRQ	IDE DMA Request for IDE Master. This signal is asserted by an IDE device. It will be active-high in DMA or Ultra-33 mode and always be inactive-low in PIO mode.
PIDED_AK#/ SIDED_AK#	IDE DACK# for IDE Master. This signal grants the IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.
PIDE_RDY/ SIDE_RDY	IDE Ready. This is the input pin from the IDE Channel. It indicates that the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions.
PIDE_IOR#/ SIDE_IOR#	IDE IOR# Command. This is the IOR# command output pin used to tell the IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.
PIDE_IOW#/ SIDE_IOW#	IDE IOW# Command. This is the IOW# command output pin used to notify the IDE device that the available Write Data is already asserted by the IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.
PIDE_INTRQ/ SIDE_INTRQ	Interrupt request signal from the IDE device.
HDRST#	Low-active hardware reset (RSTDRV inverted).
DASP_S	Time-multiplexed, open collector output that indicates that a drive is active. Also used for Master/Slave negotiation on the Secondary IDE channel.
PDIAG_S	The signal is used for Master/Slave negotiation on the Secondary IDE channel. It is asserted by the Slave to indicate to a master that the slave has passed its internal Diagnostic command. If an IDE device such as a Flash Disk exists onboard the ETX module, this signal must be connected to the PDIAG_S pin of any other device connected to the Secondary IDE channel. On ETX modules that support DMA66 or DMA100, this pin may additionally be used to detect the presence of the 80 conductor IDE cable which is required to support these modes.
CBLID_P#	On ETX modules that support DMA66 or DMA100, this pin may be used to detect the presence of an 80 conductor IDE cable on the primary IDE channel. This allows BIOS or system software to determine whether to enable high-speed transfer modes.

2.4.9.3 Miscellaneous Signals

Signal	Signal Description
SPEAKER	PC speaker output signal. This logic-level signal can be connected to an external transistor in order to drive a piezoelectric or dynamic speaker.
BATT	3V backup cell input. BATT is typically connected to a 3V lithium backup cell for RTC operation and CMOS register non-volatility in the absence of system power.
I^2CLK, I^2DAT	These clock and data lines implement an I^2C-bus which supports external slave devices only. Data rate is approximate 1-10kHz. This interface is intended for support of EEPROMs and other simple I/O-devices.
SMBDATA, SMBCLK	System Management Bus clock and data lines. May be used to support external SMBUS devices such as temperature and battery monitoring chips. The addresses of external SMBUS devices must be chosen so they do not conflict with addresses used internally on the ETX module.
KBINH	Keyboard Inhibit. Asserting this pin disables data input from the keyboard.
OVCR#	*Over-current detect* input. Used to monitor the USB power over-current. Pull with open collector to GND if over-current is detected.

2.4.9.4 Power Control Signals

Signal	Signal Description
5V_SB	Power input for the internal suspends and power control circuitry. Connect to a 5V, 100mA stand-by power source available. May be a no-connect if a standby supply is not available.
PS_ON	Active-low output from ESM-945ETX. Can be connected to the PS_ON input of an ATX power supply in order to switch the main output. In order for this pin to function, 5V_SB must be supplied to the ESM-945ETX.
PWRBTN#	Power Button Input. Connect to GND with momentary-contact switch or open collector driver to implement ATX power button control of PS_ON. In order for this pin to function, 5V_SB must be supplied to the ESM-945ETX.

2.4.9.5 Power Management Signals

Signal	Signal Description
RSMRST#	*Resume Reset input*. This input may be driven low by external circuitry in order to reset the power management logic on the ETX module.
EXTSMI	System management interrupt input. May be driven low by external circuitry to initiate an SMI.
GPE2#	General purpose power management event input 2. May be driven low by external circuitry to signal an external power management event. Within the ETX module, this pin is commonly connected to the chipset's RING# input.

3. BIOS Setup

3.1 Starting Setup

The AwardBIOS™ is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing <Del> immediately after switching the system on, or

By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

Press F1 to Continue, DEL to enter SETUP

3.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Button	Description
↑	Move to previous item
↓	Move to next item
←	Move to the item in the left hand
→	Move to the item in the right hand
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

- **Navigating Through The Menu Bar**

  Use the left and right arrow keys to choose the menu you want to be in.

Note: Some of the navigation keys differ from one screen to another.

- **To Display a Sub Menu**

  Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A "➢" pointer marks all sub menus.

3.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

3.4 In Case of Problems

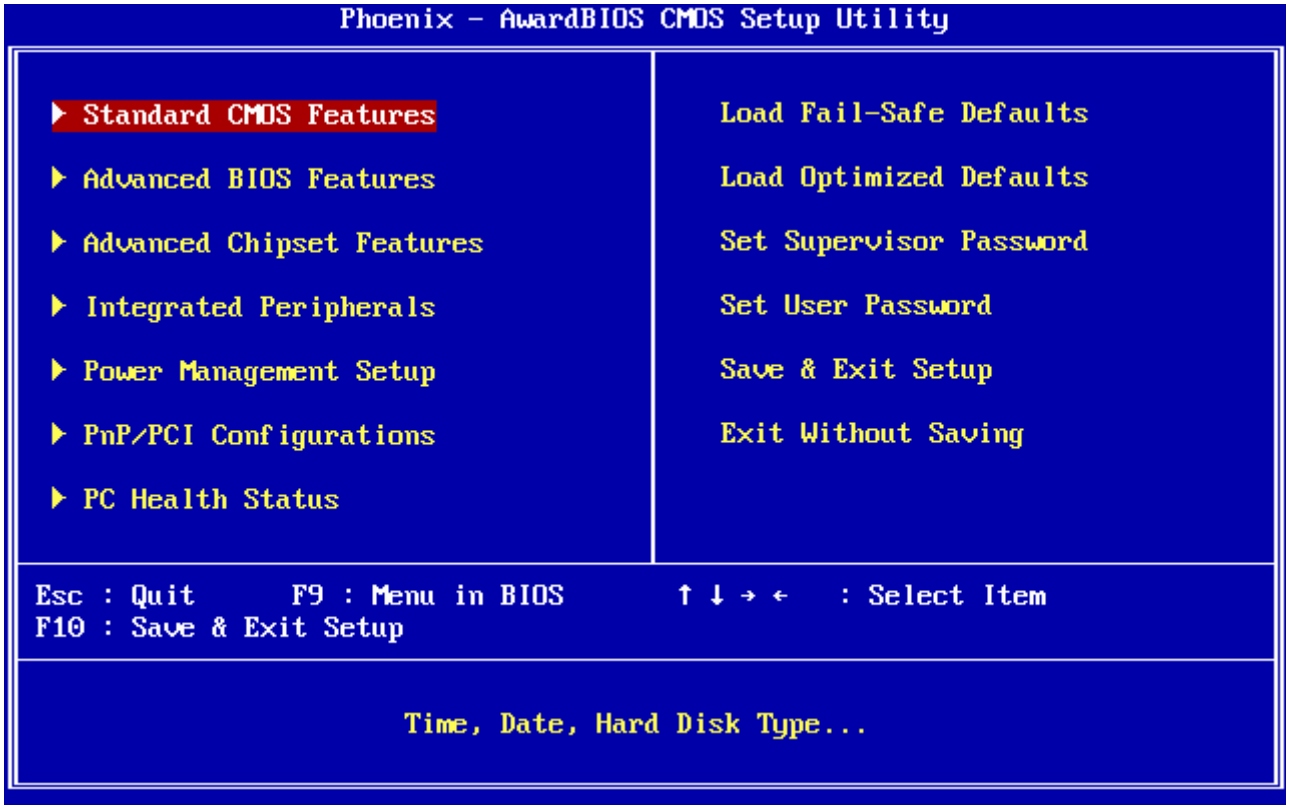
If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

3.5 Main Menu

Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

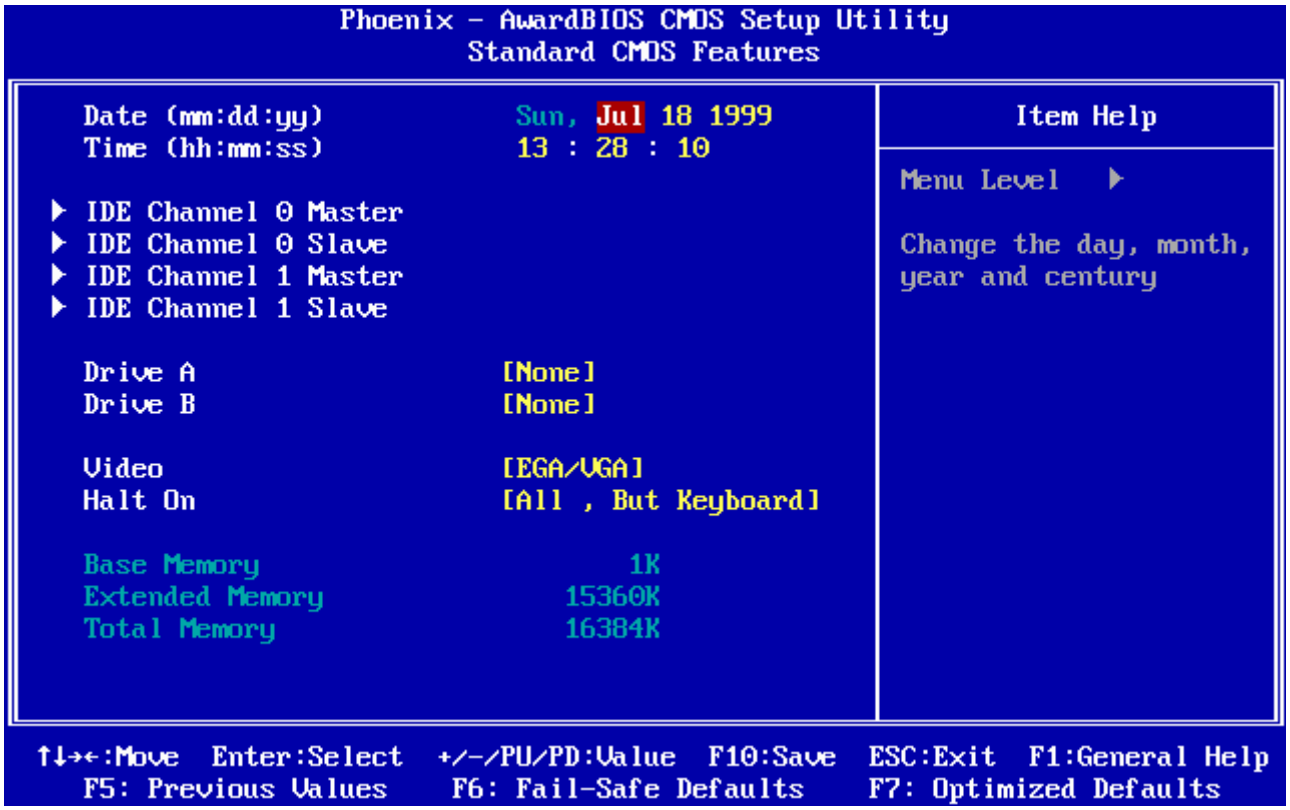
Note that a brief description of each highlighted selection appears at the bottom of the screen.



Note: The BIOS setup screens shown in this chapter are for reference purposes only, and may not exactly match what you see on your screen.
Visit the Avalue website (www.avalue.com.tw) to download the latest product and BIOS information.

3.5.1 Standard CMOS Features

The items in Standard CMOS Setup Menu are divided into few categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.



3.5.1.1 Main Menu Selection

This reference table shows the selections that you may make on the Main Menu.

Item	Options	Description
Time	HH : MM : SS	Set the system time
IDE Channel 0 Master IDE Channel 0 Slave IDE Channel 1 Master IDE Channel 1 Slave	Options are in 3.5.1.2	Press <Enter> to enter the sub menu of detailed options
Drive A Drive B	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you

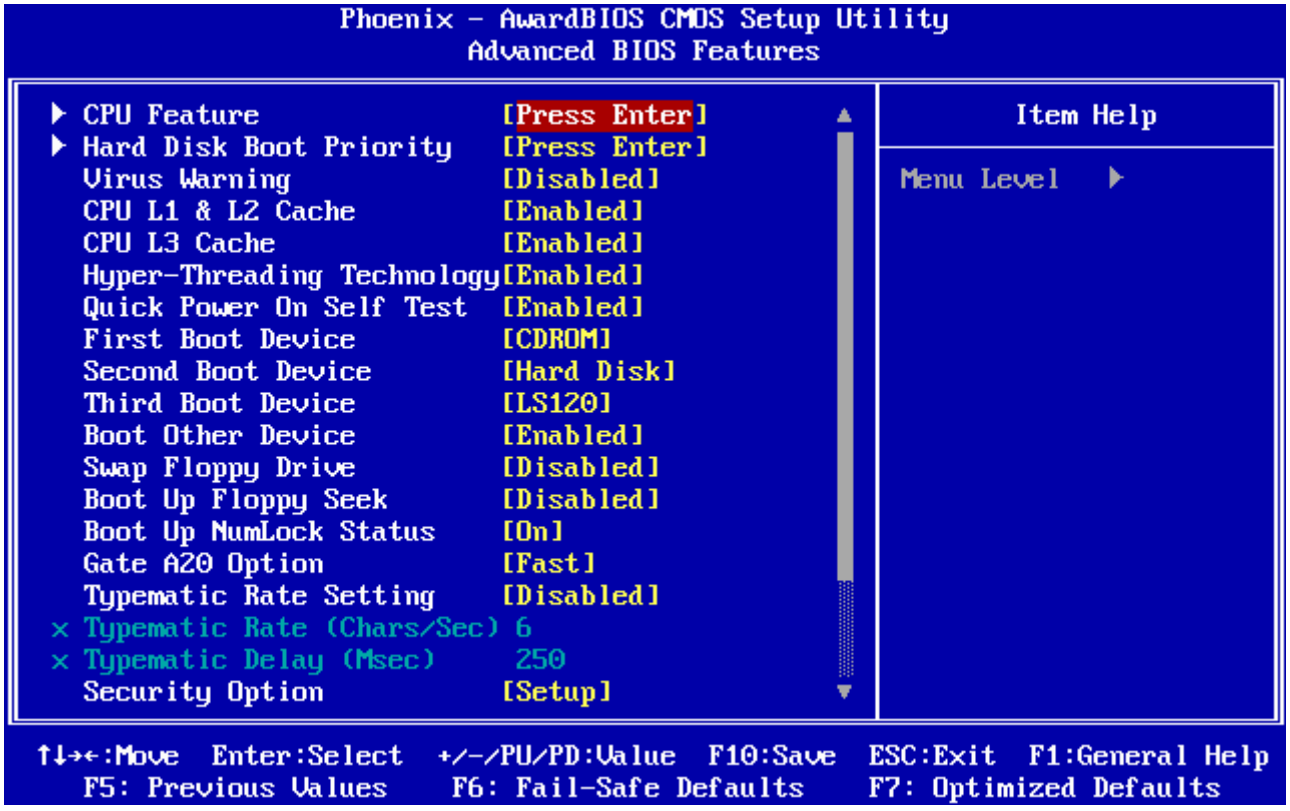
3.5.1.2 IDE Adapter Setup

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive. The below table will shows the IDE primary master sub menu.

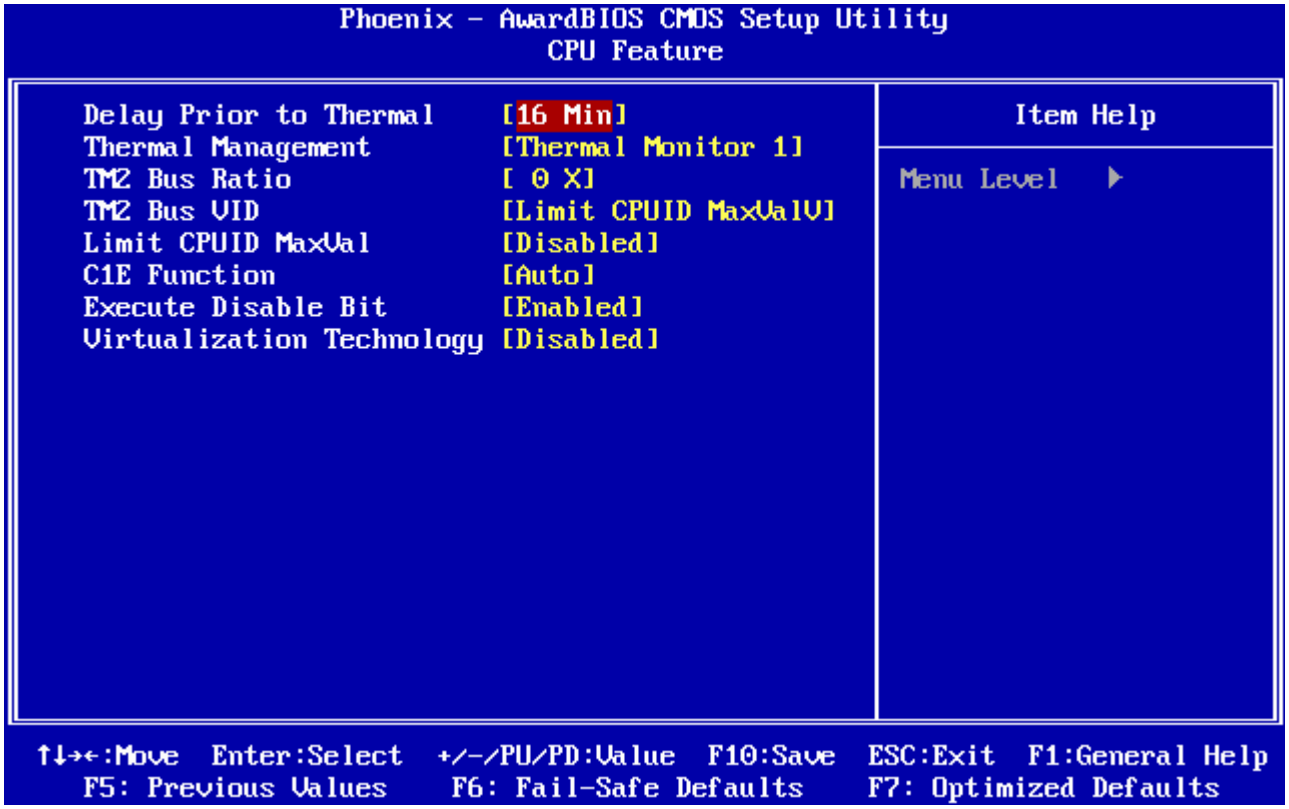
Item	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Channel 0 Master IDE Channel 0 Slave IDE Channel 1 Master IDE Channel 1 Slave	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Access Mode	CHS, LBA Large, Auto	Choose the access mode for this hard disk
The following options are selectable only if the 'IDE Channel …' item is set to 'Manual'		
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** **Warning**: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

3.5.2 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



3.5.2.1 CPU Feature

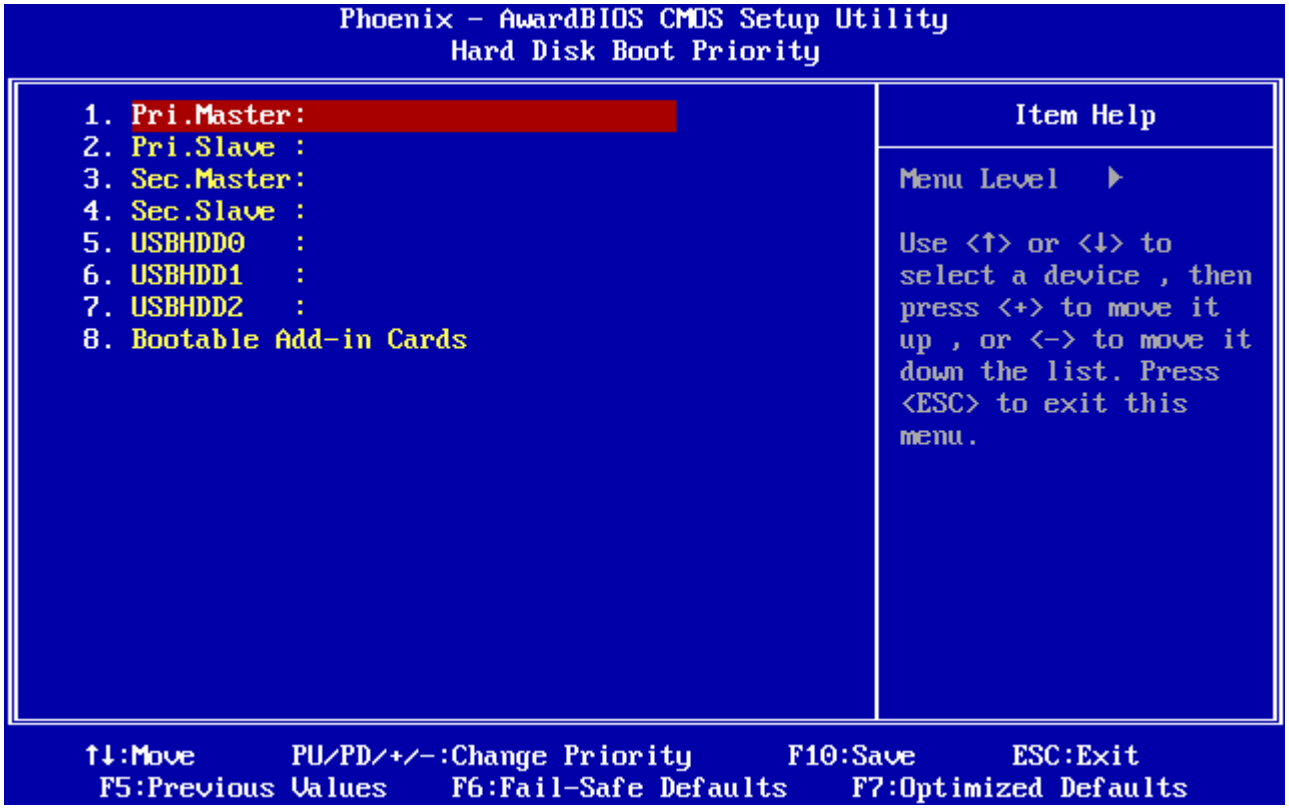


This item allows you to setup the CPU thermal management function.

Item	Options	Description
Delay Prior to Thermal	4, 8, 16, 32 Min	Allow the Thermal Monitor to be activated of certain minutes in automatic mode after the system boots.
Thermal Management	Thermal Monitor 1 Thermal Monitor 2	Allow to choose the thermal management method of the monitor.
TM2 Bus Ratio	0~255	Represents the frequency. Bus ratio of the throttled performance state that will be initiated when the on-die sensor goes from not hot to hot.
TM2 Bus VID	0.700 ~ 1.708	Represents the voltage of the throttled performance state that will be initiated when the on-die sensor goes from not hot to hot.
Limit CPUID MaxVal	Disable Enable	In order to mask the physical CPUID for Proscott core when running WinNT, Award BIOS provides "Limit CPUID MaxVal" feature. Enabling this feature will make the main board BIOS respond "suitable", "virtual" CPUID to OS kernel. So WinNT or the legacy OS can use the masked CPUID to work well with the new CPU design.
C1E Function	Auto, Disabled	The C1E function enables the Core 2 Extreme to throttle back to its standard clock rate under light load
Execute Disable Bit	Enabled, Disabled	It can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system.

Virtualization Technology	Enabled, Disabled	This BIOS feature is used to enable or disable the Intel Virtualization Technology (IVT) extensions that allow multiple operating systems to run simultaneously on the same system.

3.5.2.2 Hard Disk Boot Priority



This item allows you to set the boot priority of the hard drives installed in the system.

Item	Description
Pri./Sec. Master/Slave	Boot up from IDE Primary/Secondary Master/Slave Hard Disk
USBHDD 0/1/2	Boot up from 1st/2nd/3rd USB Hard Disk
Bootable Add-in Cards	Boot up from other Add-In Card Hard Disk Device.

3.5.2.3 Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Item	Description
Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

3.5.2.4 CPU L1 & L2 & L3 Cache

The item allows you to speed up memory access. However, it depends on CPU design.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.5 Hyper-Threading Technology

The item allows you to enable HT Technology. However, it depends on CPU design.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.6 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Item	Description
Enabled	Enable quick POST
Disabled	Normal POST

3.5.2.7 First/Second/Third/Other Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

Item	Description
LS120	LS120 Device
Hard Disk	Hard Disk Device
CDROM	CDROM Device
ZIP100	ZIP-100 Device
USB-FDD	USB Floppy Device
USB-ZIP	USB ZIP Device
USB-CDROM	USB CDROM Device
LAN	Network Device
Disabled	Disabled any boot device

3.5.2.8 Swap Floppy Drive

While system has two floppy drivers installed, this item will be affected. This function is to assign physical drive B to logical drive A

Item	Description
Enabled	Assign physical drive B to logical drive A
Disabled	No change

3.5.2.9 Boot Up Floppy Seek

Seeks disk drives during boot up. Disabling seeds boot up.

Item	Description
Enabled	Enable Floppy Seek
Disabled	Disable Floppy Seek

3.5.2.10 Boot Up NumLock Status

Select power on state for NumLock.

Item	Description
On	Enable NumLock
Off	Disable NumLock

3.5.2.11 Gate A20 Option

Select if chipset or keyboard controller should control Gate A20.

Item	Description
Normal	A pin in the keyboard controller controls Gate A20
Fast	Lets chipset control Gate A20

3.5.2.12 Typematic Rate Setting

This feature enables you to control the keystroke repeat rate when you depress a key continuously. When enabled, you can manually adjust the settings using the two typematic controls (Typematic Rate and Typematic Delay). If disabled, the BIOS will use the default setting.

Item	Description
Enabled	Enable typematic rate/delay setting
Disabled	Disable typematic rate/delay setting

3.5.2.13 Typematic Rate (Chars/Sec)

This is the rate at which the keyboard will repeat the keystroke if you press it continuously. This setting will only work if Typematic Rate Setting is enabled..

Options: 6, 8, 10, 12, 15, 20, 24, 30

3.5.2.14 Typematic Delay (Msec)

This is the delay, in milliseconds, before the keyboard automatically repeats the keystroke that you have pressed continuously. This setting will only work if Typematic Rate Setting is enabled.

Options: 250, 500, 750, 1000

3.5.2.15 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

Item	Description
System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

3.5.2.16 APIC Mode

The BIOS supports versions 1.4 of the Intel multiprocessor specification. When enabled, The MPS Version 1.4 Control for OS can be activated.
The choice: Enabled/Disabled.

3.5.2.17 MPS Version Control For OS

This feature is only applicable to multiprocessor board as it specifies the version of the Multi-Processor Specification (MPS) that the board will use.
The choice: 1.4, 1.1.

3.5.2.18 OS Select for DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.

Item	Description
Non-OS2	Disable OS for over 64 MB DRAM
OS2	Enable OS for over 64 MB DRAM

3.5.2.19 Report No FDD For WIN95

The original Windows95 requires the presence of a floppy. Unless the BIOS tells it to disregard the absence of the drive, it will generate an error message. For other operating systems as Win98 etc this field is without relevance.

Item	Description
No	Don't generate error message
Yes	Generate error message

3.5.2.20 Small Logo (EPA) Show

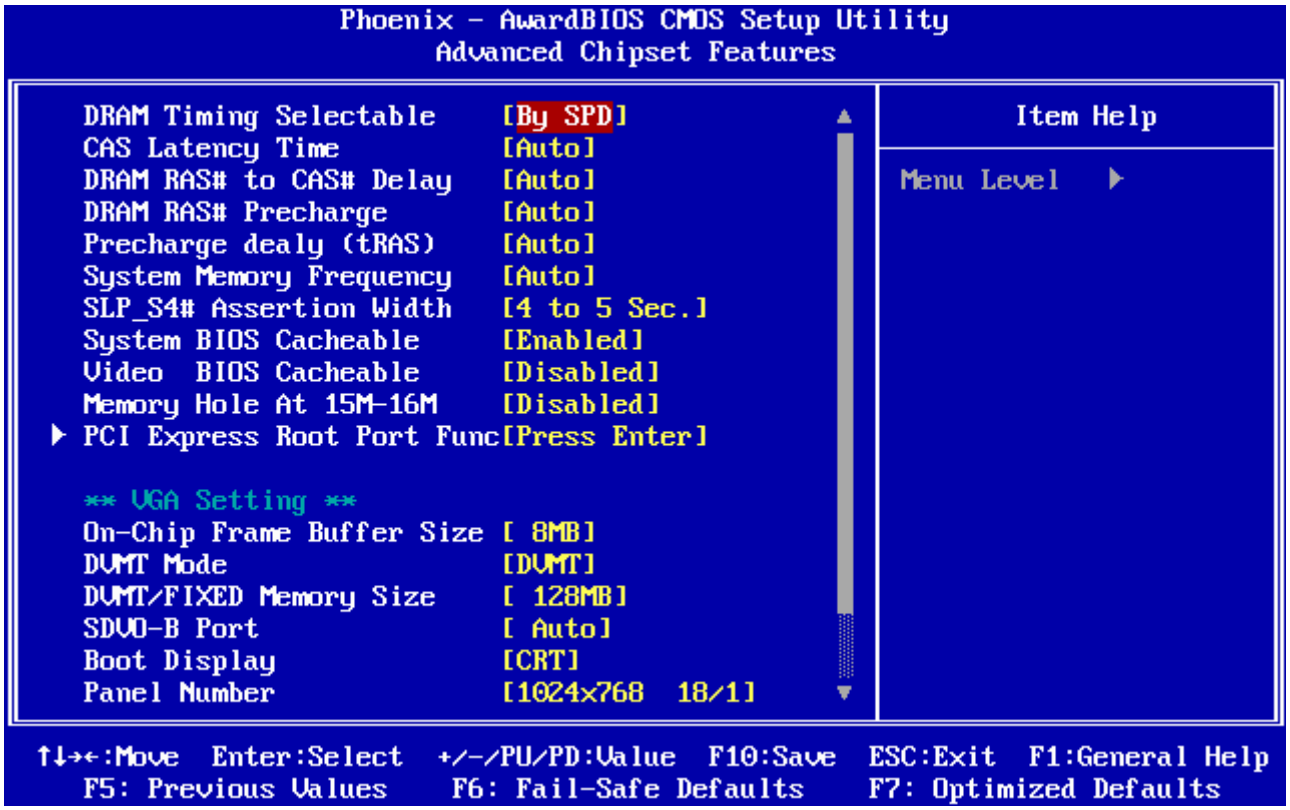
This item allows you enabled/disabled the small EPA logo show on screen at the POST step.

Item	Description
Enabled	EPA Logo show is enabled
Disabled	EPA Logo show is disabled

3.5.3 Advanced Chipset Features

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.



3.5.3.1 DRAM Timing Selectable

This item allows you to select the DRAM timing value by SPD data or Manual by yourself.
The choices: Manual, By SPD.

3.5.3.2 CAS Latency Time

This item controls the time delay (in clock cycles - CLKs) that passes before the SDRAM starts to carry out a read command after receiving it. This also determines the number of CLKs for the completion of the first part of a burst transfer. In other words, the lower the latency, the faster the transaction.
The choices: 5, 4, 3, 6, Auto.

3.5.3.3 DRAM RAS# to CAS# Delay

This option allows you to insert a delay between the RAS (**Row Address Strobe**) and CAS (**Column Address Strobe**) signals. This delay occurs when the SDRAM is written to, read from or refreshed. Naturally, reducing the delay improves the performance of the SDRAM while increasing it reduces performance.
The choices: 2, 3, 4, 5, 6, Auto.

3.5.3.4 DRAM RAS# Precharge

This option sets the number of cycles required for the RAS to accumulate its charge before the SDRAM refreshes. Reducing the precharge time to **2** improves SDRAM performance but if the precharge time of **2** is insufficient for the installed SDRAM, the SDRAM may not be refreshed properly and it may fail to retain data
So, for better SDRAM performance, set the **SDRAM RAS Precharge Time** to **2** but increase it to **3** if you face system stability issues after reducing the precharge time.
The choices: 2, 3, 4, 5, 6, Auto.

3.5.3.5 Precharge Delay (tRAS)

It allows controlling the memory bank's minimum row active time (tRAS). This constitutes the time when a row is activated until the time the same row can be deactivated. If the tRAS period is too long, it can reduce performance by unnecessarily delaying the deactivation of active rows. Reducing the tRAS period allows the active row to be deactivated earlier.
If the tRAS period is too short, there may not be enough time to complete a burst transfer. This reduces performance and data may be lost or corrupted.
The choices: Auto, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15.

3.5.3.6 System Memory Frequency

It allows controlling the system memory frequency. The memory frequency will either be equal to or less than the processor system bus frequency.
The choices: Auto, 400MHz, 533MHz, 667MHz.

3.5.3.7 SLP_S4# Assertion Width

This item allows you to set the SLP_S4# Assertion Width.
The choices: 4 to 5 Sec., 3 to 4 Sec., 2 to 3 Sec., 1 to 2 Sec...

3.5.3.8 System BIOS Cacheable

This feature is only valid when the system BIOS is shadowed. It enables or disables the caching of the system BIOS ROM at **F0000h-FFFFFh** via the L2 cache. This greatly speeds up accesses to the system BIOS. However, this does **not** translate into better system performance because the OS does not need to access the system BIOS much.
The choices: Disabled, Enabled.

3.5.3.9 Video BIOS Cacheable

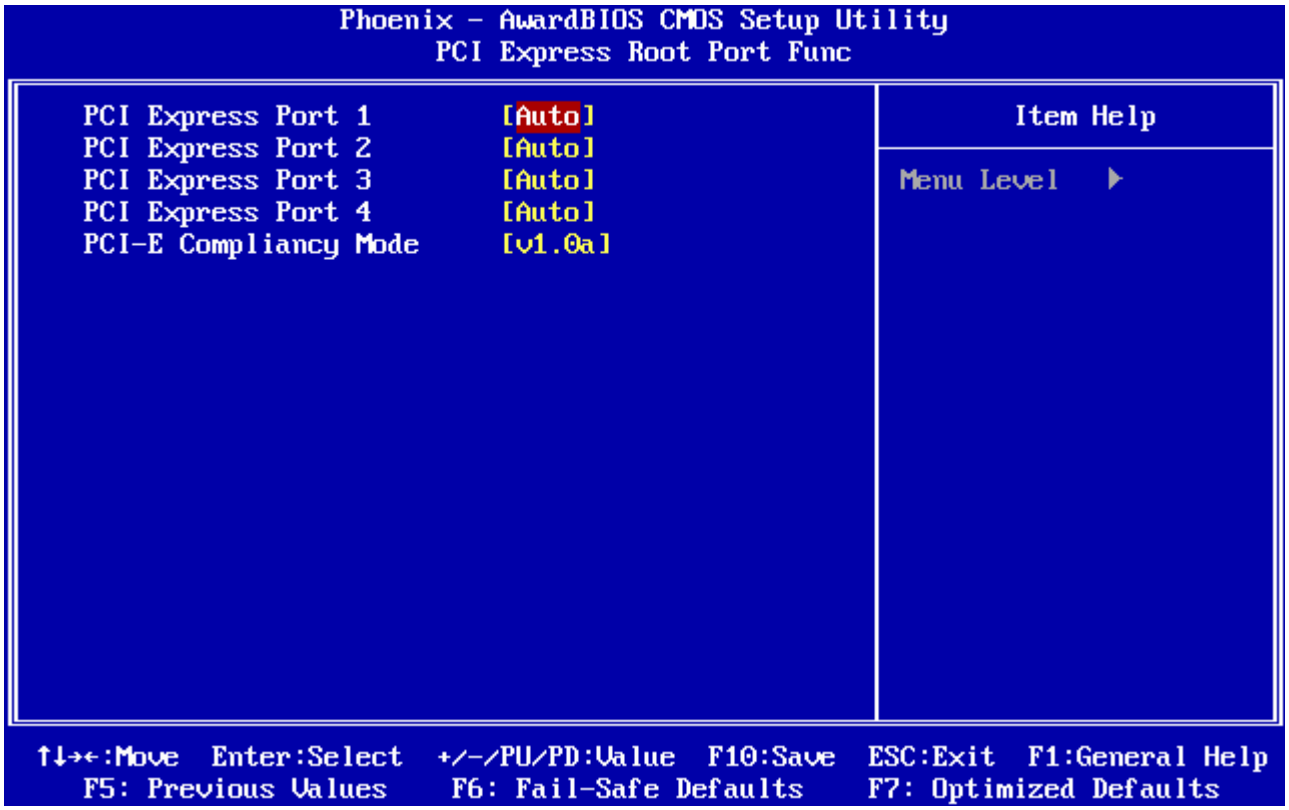
This feature is only valid when the video BIOS is shadowed. It enables or disables the caching of the video BIOS ROM at **C0000h-C7FFFh** via the L2 cache. This greatly speeds up accesses to the video BIOS. However, this does **not** translate into better system performance because the OS bypasses the BIOS using the graphics driver to access the video card's hardware directly.
The Choice: Enabled, Disabled.

3.5.3.10 Memory Hole At 15M-16M

Enabling this feature reserves 15MB to 16MB memory address space to ISA expansion cards that specifically require this setting. This makes the memory from 15MB and up unavailable to the system. Expansion cards can only access memory up to 16MB.
The choice: Enable, Disable.

3.5.3.11 PCI Express Root (PCI Express Port1/2/3/4)

For the PCI Express root ports, the assignment of a function umber to a root port is not fixed. This item allows you to re-assign the function numbers on a port by port basis. You can disable/hide any root port and have still have functions 0 thru N-1 where N is the total number of enabled root ports.



The choices: Auto, Enabled, Disabled.

3.5.3.12 PCI-E Compliancy Mode

This feature is used to select the compliancy mode for PCI-E.

The choices: v.1.0a, v1.0

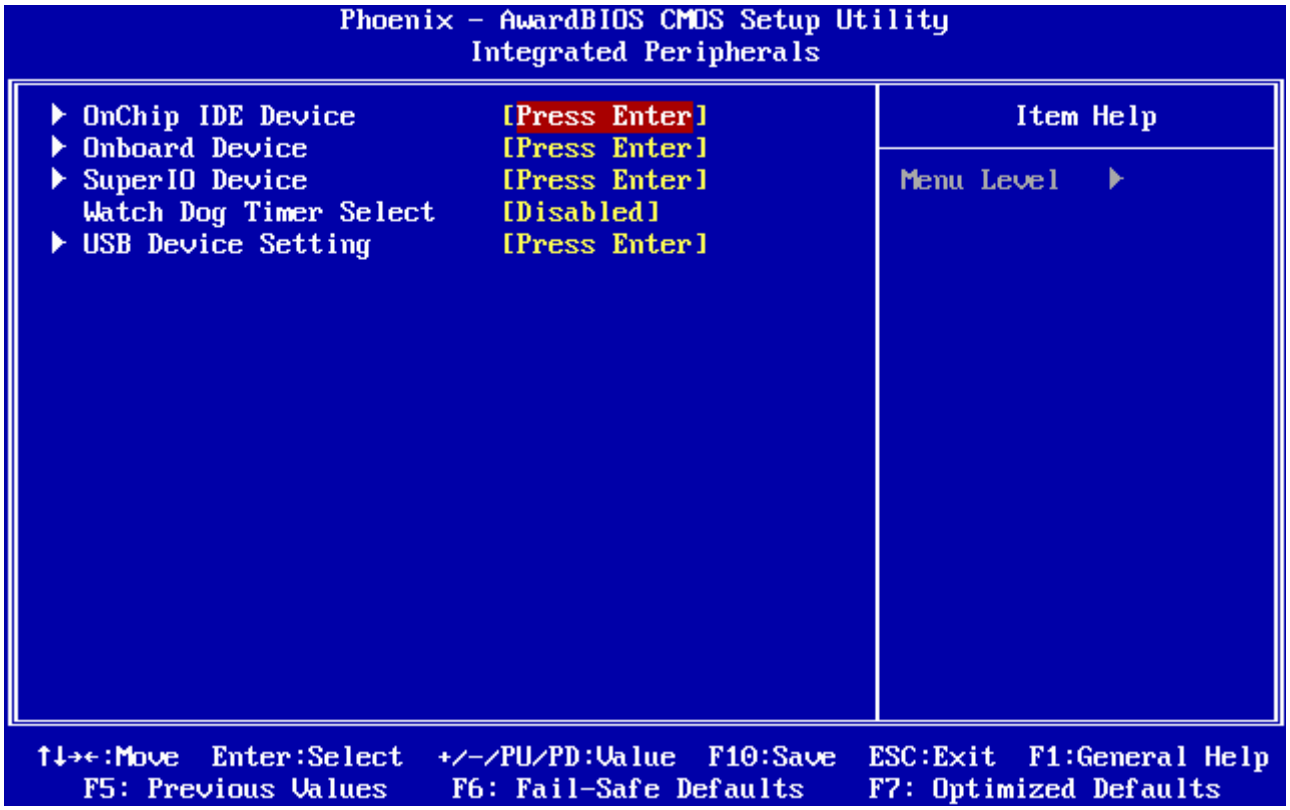
3.5.3.13 VGA Setting

Item	Options	Description
On-Chip Frame Buffer Size	1/ 4/ 8/ 16/ 32 MB	This item is to select the amount of system memory that will be utilized as internal graphics device memory.
DVMT Mode	FIXED DVMT BOTH	This feature allows you to select the Dynamic Video Memory Technology (DVMT) operating mode.
DVMT/FIXED Memory Size	64MB 128MB 224MB	This feature allows you to select the memory size of DVMT/BOTH operating mode.
SDVO-B Port	Auto	This feature allows you to select the SDVO-B Port.
Boot Display	Auto CRT, LCD,	This feature allows you to select the display device when you boot up the system.

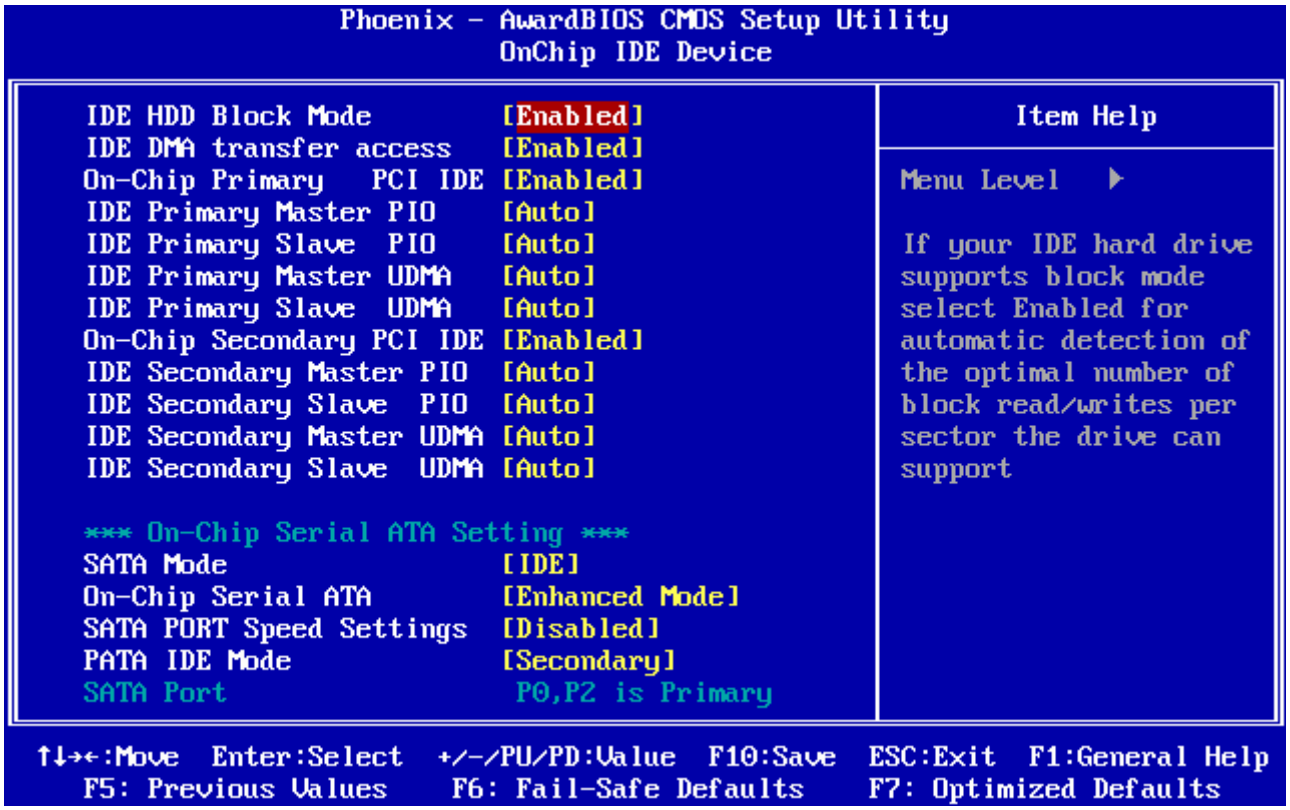
	CRT+LCD, TV, CRT+TV	
Panel Number	1680x1050 2x24B, 1024x768 1x24B, 1280x1024 2x24B, 1440x900 2x24B.	This feature allows you to select Panel Resolution that will be displayed depending on the LCD Panel.
TV Standard	Off, NTSC, PAL, SECAM	This feature allows you to select an analog TV standard system.
Video Connector	Automatic, Composite, Component, Both.	This feature allows you to select the output video connector style.
TV Format	Auto, NTSC_M, NTSC_M_J, NTSC_433, NTSC_N, PAL_B, PAL_G, PAL_D, PAL_H, PAL_I, PAL_M, PAL_N, PAL_60, SECAM_L, SECAM_L1, SECAM_B, SECAM_D, SECAM_G, SECAM_H.	This feature allows you to select the TV format.

3.5.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.



3.5.4.1 OnChip IDE Device



The chipset contains a PCI IDE interface with support for one IDE channel and two SATA

channels. Select Enabled to activate the primary IDE interface. Select Disabled to deactivate this interface.

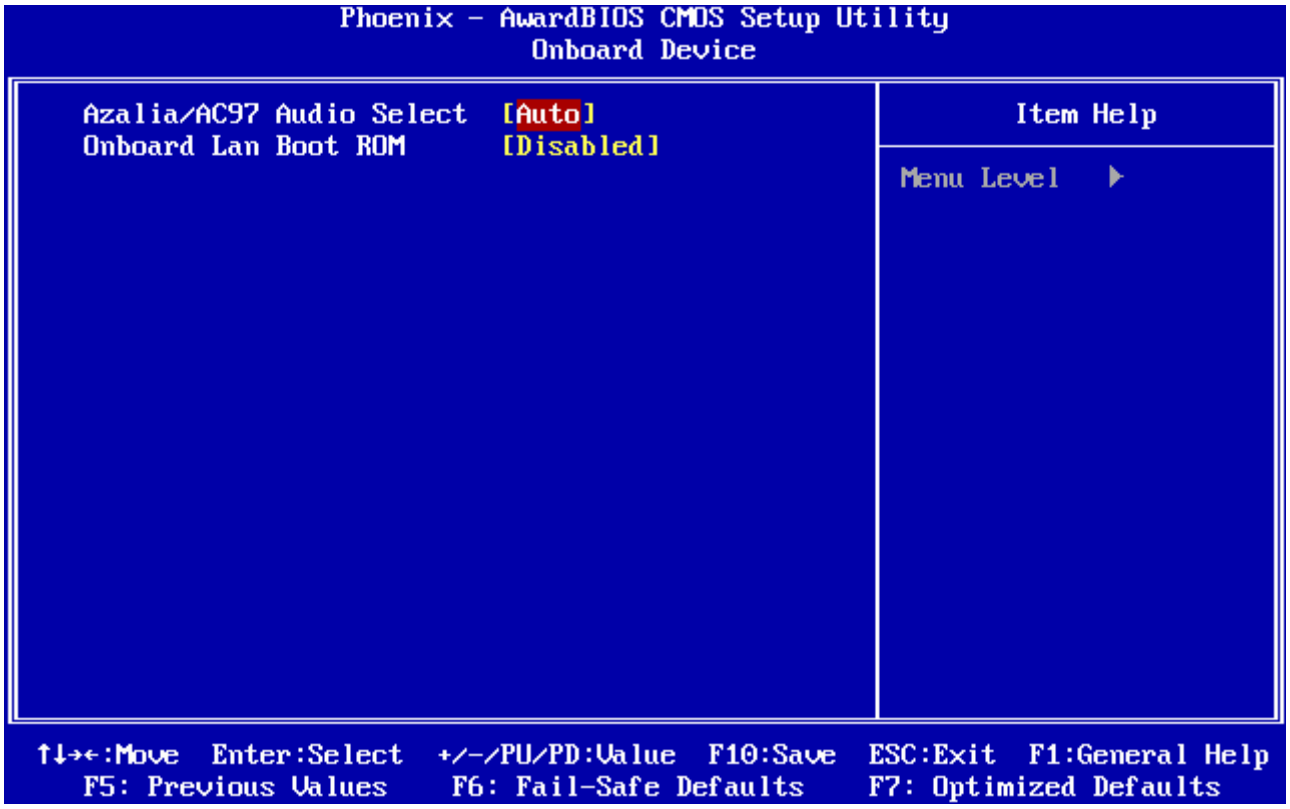
Item	Options	Description
IDE HDD Block Mode	Enabled Disabled	Speeds up HDD access by transferring data from multiple sectors at once instead of using the old single sector transfer mode if the HDD supports block transfers and configure the proper block transfer settings for it. Up to 64KB of data can be transferred per interrupt with IDE HDD Block Mode enabled. (Virtually all HDDs now support block transfers.)
IDE DMA transfer access	Enabled Disabled	It allows you to enable or disable DMA (Direct Memory Access) support for all IDE devices. If you disable this BIOS feature, the BIOS will disable DMA transfers for all IDE drives. They will revert to PIO mode transfers. If you enable this BIOS feature, the BIOS will enable DMA transfers for all IDE drives. The proper DMA mode will be detected at boot-up. If the drive does not support DMA transfers, then it will use PIO mode instead.
On-Chip Primary PCI IDE **On-Chip Secondary PCI IDE**	Enabled Disabled	The integrated peripheral controller contains an IDE interface with support for two IDE channels. It allows you to activate each channel separately.
IDE Primary Master PIO **IDE Primary Slave PIO** **IDE Secondary Master PIO** **IDE Secondary Slave PIO**	Auto Mode 0 Mode 1 Mode 2 Mode 3 Mode 4	The IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.
IDE Primary Master UDMA **IDE Primary Slave UDMA** **IDE Secondary Master UDMA** **IDE Secondary Slave UDMA**	Auto Disabled	Ultra DMA implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If the hard drive and the system software both support Ultra DMA, select Auto to enable BIOS support.

3.5.4.1.1 On-Chip Serial ATA Setting

The field under the SATA setting includes SATA Mode (IDE), On-Chip Serial ATA (Auto), PATA IDE Mode (Secondary) and SATA Port (P0, P2 is Primary).

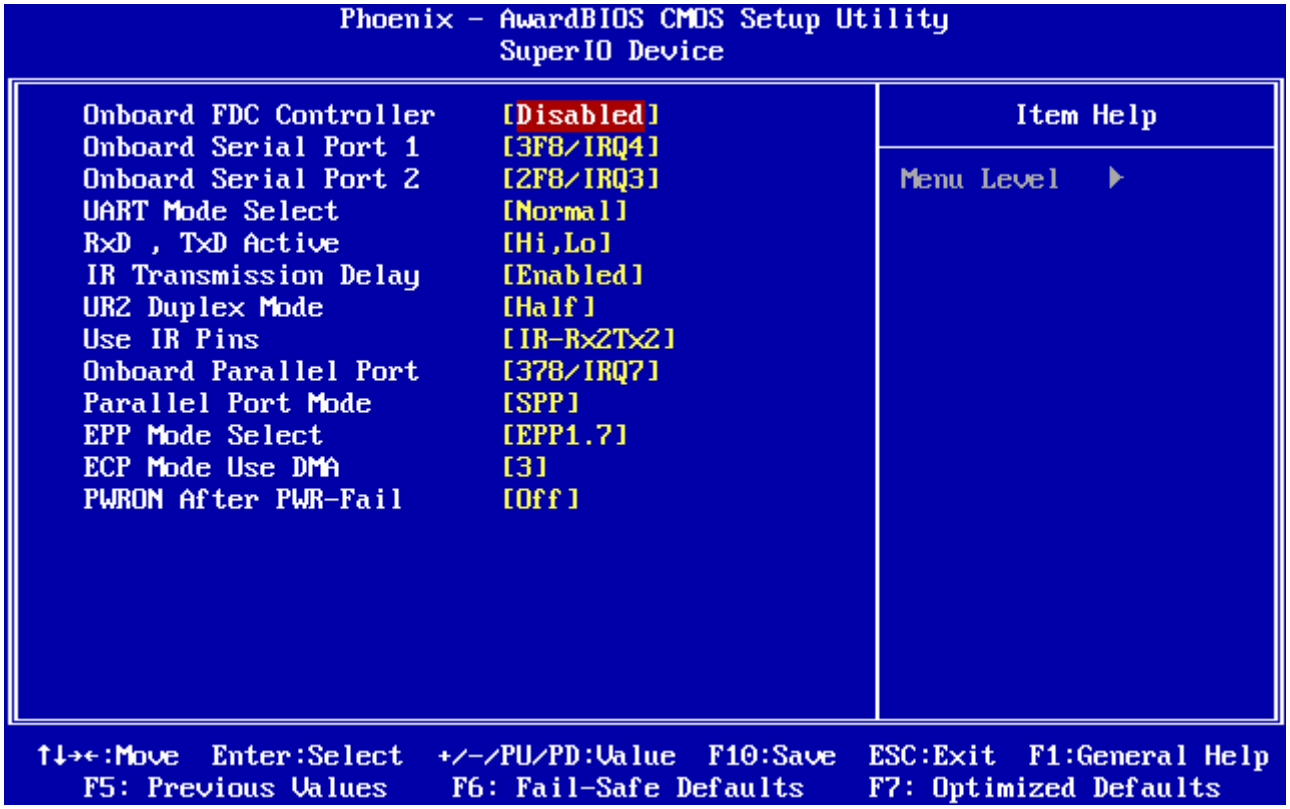
Item	Options	Description
SATA Mode	IDE AHCI	It allows you to select the operation mode for SATA controller.
On-Chip Serial ATA	Disabled, Auto, Combined Mode, Enhanced Mode, SATA Only	It provides access to set the mode of the On-Chip SATA devices.
SATA PORT Speed Settings	Disabled Force GEN I Force GEN II	This item allows you to select the speed of SATA ports.
PATA IDE Mode	Secondary	This item shows the PATA IDE mode.

3.5.4.2 Onboard Device



Item	Options	Description
Azalia/AC97 Audio Select	Auto Azalia AC97 Audio All Disabled	This item allows you to select the Audio codec.
Onboard LAN Boot ROM	Enabled Disabled	This item allows you to enabled the LAN Boot ROM.

3.5.4.3 Super IO Device



Item	Options	Description
Onboard FDC Controller	Enabled Disabled	Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you are not going to use FDC or the system has no floppy drive, select Disabled in this field.
Onboard Serial Port 1 Onboard Serial Port 2	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3 AUTO	Select an address and corresponding interrupt for the first and second serial ports.
UART Mode Select	IrDA ASKIR Normal	Select UART2 mode as standard serial port or IR port.
RxD , TxD Active	Hi,Hi Hi,Lo Lo,Hi Lo,Lo	This item allows you to determine the active of RxD, TxD level.
IR Transmission Delay	Enabled Disabled	This item allows you to enable/disable the IR Transmission Delay.
UR2 Duplex Mode	Half Full	Select the value required by the IR device connected to the IR port. Full-duplex mode permits simultaneous two-direction transmission. Half-duplex mode permits transmission in one direction only at a time.
Use IR Pins	RxD2,TxD2 IR-Rx2Tx2	This item allows you to determine the pin definition.
Onboard Parallel Port	Disabled	Select a matching address and interrupt for the

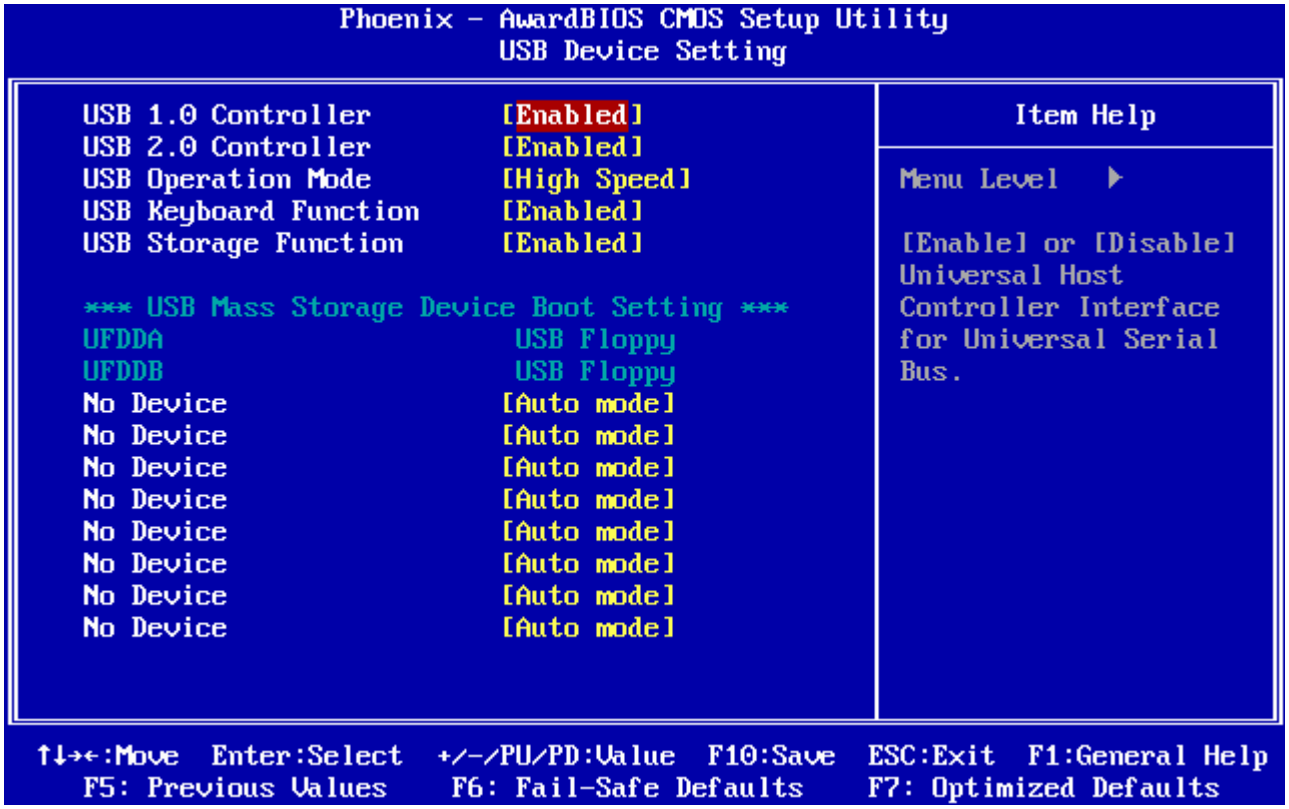
	378/IRQ7 278/IRQ5 3BC/IRQ7 Floppy	physical parallel (printer) port.
Parallel Port Mode	SPP EPP ECP ECP+EPP Normal	Select an operating mode for the onboard parallel port. Select Compatible or Extended unless you are certain both your hardware and software support EPP or ECP mode.
EPP Mode Select	EPP1.9 EPP1.7	Select EPP port type 1.7 or 1.9.
ECP Mode Use DMA	1 3	Select a DMA channel for the port.
PWRON After PWR-Fail	Off On Former-Sts	This item is to set whether to run Ac Loss Auto Restart or off

3.5.4.4 Watch Dog Timer

This option will determine watch dog timer.

The choices: Disabled, 10, 20, 30, 40 Sec, 1, 2, 4 Min.

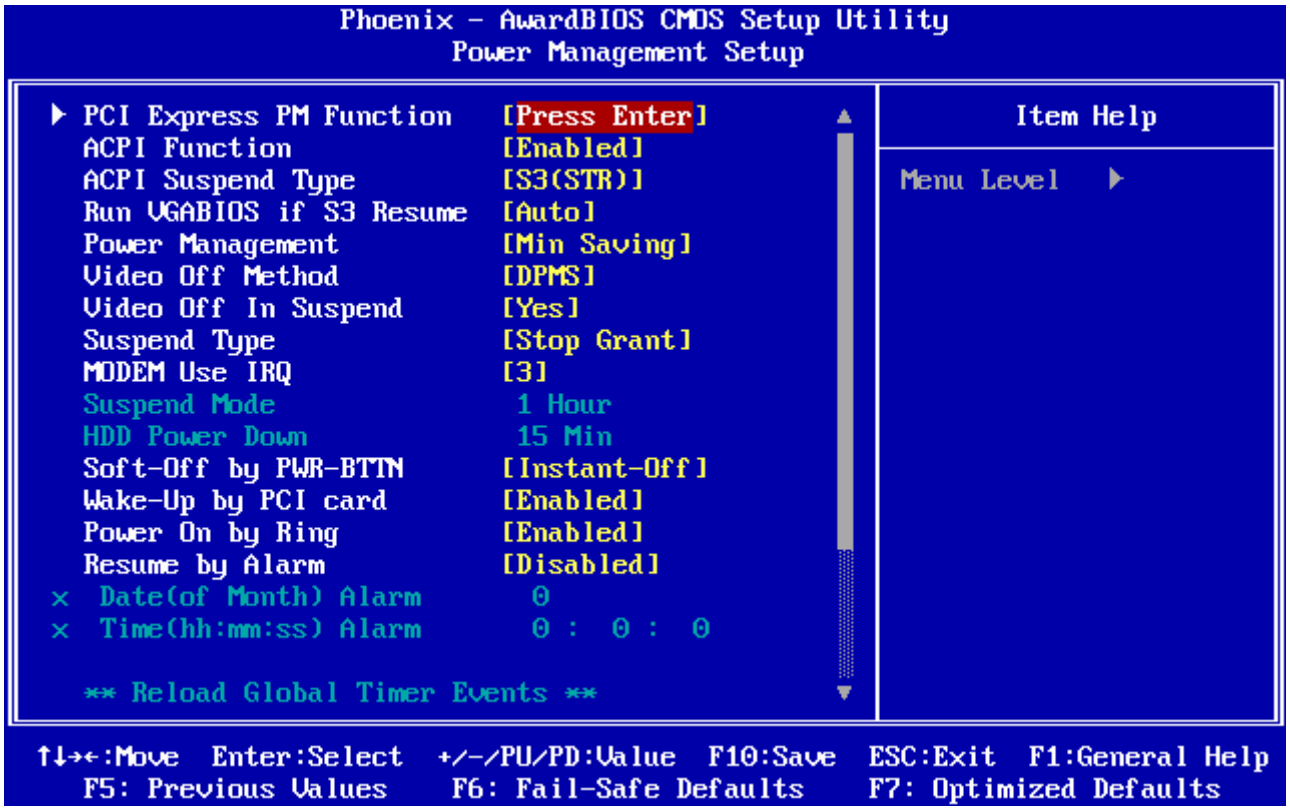
3.5.4.5 USB Device Setting



Item	Options	Description
USB 1.0 Controller	Disabled Enabled	This item enables you to use the onboard USB 1.0 controller to communicate with your USB devices
USB 2.0 Controller	Disabled Enabled	This item enables you to use the onboard USB 2.0 controller to communicate with your USB devices
USB Operation Mode	Full/Low Speed High Speed	This item allows you to select the USB mode.
USB Keyboard Function	Disabled Enabled	This BIOS feature determines if support for the USB keyboard should be provided by the operating system or the BIOS.
USB Storage Function	Disabled Enabled	This BIOS feature determines if support for the USB Storage should be provided by the operating system or the BIOS.

3.5.5 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.



3.5.5.1 PCI Express PME Function

This item allows you to enable/disable the PCI Express PME Function.

The choices: Enabled, Disabled.

3.5.5.2 ACPI Function

This item allows you to enable/disable the ACPI function.

The choices: Enabled, Disabled.

3.5.5.3 ACPI Suspend Type

This item will set which ACPI suspend type will be used.
The choices: S1 (POS), S3 (STR).S1&S3.

3.5.5.4 Run VGABIOS if S3 Resume

There are 3 modes for you to decide to operate VGABIOS or not when the ACPI suspend type is S3.
The choices: Auto, Yes, No.

3.5.5.5 Power Management

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

Item	Description
User Defined	Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr. except for HDD Power Down which ranges from 1 min. to 15 min. and disable.
Min. Saving	Minimum power management, HDD Power Down = 15 Min,
Max. Saving	Maximum power management, HDD Power Down =1 Min,

3.5.5.6 Video Off Method

This determines the manner in which the monitor is blanked.
The choices: Blank Screen, V/H SYNC+Blank, DPMS.

3.5.5.7 Video Off In Suspend

This determines the manner in which the monitor is blanked.
The choice: No, Yes.

3.5.5.8 Suspend Type

This function allows to select Suspend type.
The choices: Stop Grant, PwrOn Suspend.

3.5.5.9 MODEM Use IRQ

This determines the IRQ in which the MODEM can use.
The choices: NA, 3, 4, 5, 7, 9, 10, 11.

3.5.5.10 Suspended Mode

It specifies the length of time of system inactivity while in full power on state before the computer enters suspend mode and motivates the enable 'Wake Up Events In Doze & Standby' / 'PM Events'.
The choices: Disabled, 1, 2, 4, 8, 12, 20, 30, 40 mins, 1 hr.

3.5.5.11 HDD Power Down

When enable and after the set time of system inactivity, the hard disk drive will be powered down while all other devices remain active.
The choices: Disabled, 1 ~ 15 mins.

3.5.5.12 Soft-Off by PWR-BTTN

Pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has “hung”.(Only could working on ATX Power supply)
The choices: Delay 4 Sec, Instant-Off.

3.5.5.13 Wake Up by PCI Card

This will enable the system to wake up through PCI Card peripheral.
The choices: Enable, Disabled.

3.5.5.14 Power On By Ring

This determines whether the system boot up if there’s an incoming call from the Modem.
The choices: Enable, Disabled.

3.5.5.15 Resume By Alarm

This function is for setting date and time for your computer to boot up.
The choices: Enabled, Disabled.

3.5.5.16 Date<of Month>/Time<hh:mm:ss> Alarm

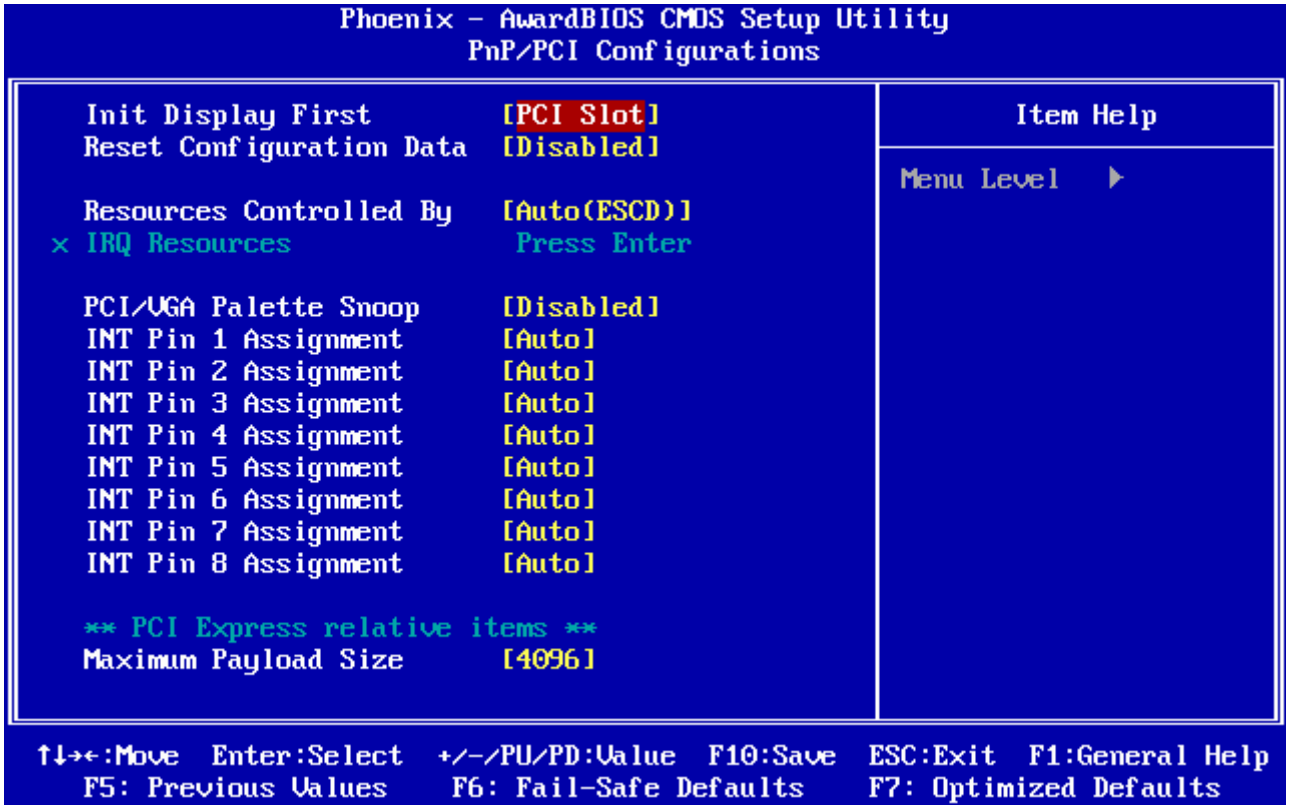
After enabled “Resume By Alarm”, set the specific date/hour/minute/second specified in these fields.
The choices: Alarm Date: 01-31, Every Day / Alarm Hour: 00-23 /
Alarm Minute: 00-59/ Alarm Second: 00-59

3.5.5.17 Primary/Secondary IDE 0/1, FDD, COM, LPT PORT, PCI PIRQ[A-D]#

Reload Global Timer events are I/O events whose occurrence can prevent the system from entering a power saving mode or can awake the system from such a mode. In effect the system remain alert for anything which occurs to a device which is configured as Enabled, even when the system is in a power down mode.
The choices: Enabled, Disabled.

3.5.6 PnP / PCI Configuration

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.



3.5.6.1 Init Display First

It allows you to select whether to boot the system using the AGP graphics card or the PCI graphics card. This is particularly important if you have AGP and PCI graphics cards but only one monitor.

The choices: PCI Slot, Onboard, PCIEx.

3.5.6.2 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

The choices: Enabled, Disabled.

3.5.6.3 Resources Controlled By

The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. If you set this field to “manual” choose specific resources by going into each of the sub menu that follows this field (a sub menu is preceded by a “➢”).
The choices: Auto (ESCD), Manual.

3.5.6.4 IRQ Resources

When resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.

3.5.6.4.1 IRQ-3/4/5/7/9/10/11/12/14/15 Assigned to

This item allows you to determine the IRQ assigned to the ISA bus and is not available to any PCI slot. Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.
The choices: PCI Device, Reserved.

3.5.6.5 PCI / VGA Palette Snoop

Leave this field at Disabled.
The choices: Enabled, Disabled.

3.5.6.6 INT Pin 1/2/3/4/5/6/7/8 Assignment

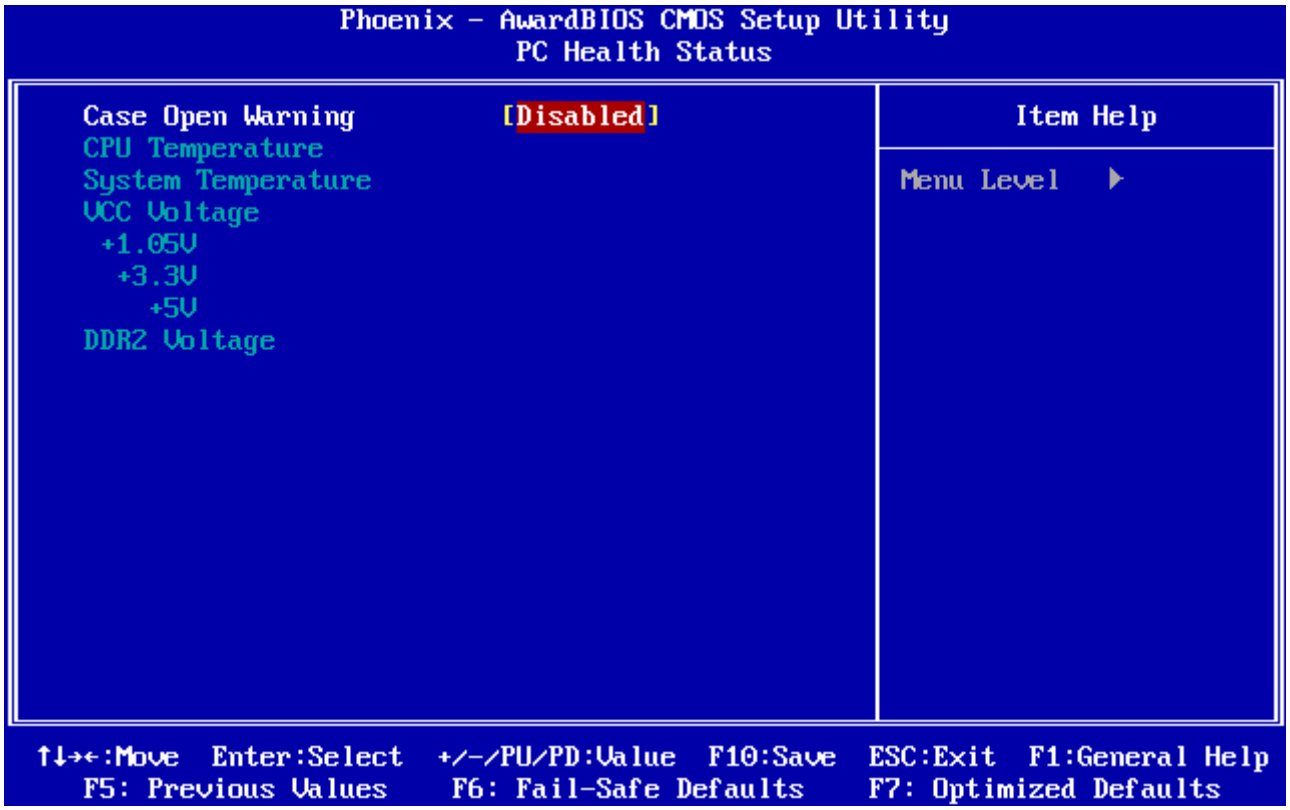
This feature allows you to assign the PCI IRQ numbers for PCI slots. Selecting the default, Auto, allows the PCI controller to automatically allocate the IRQ numbers.
The choices: Auto, 3, 4, 5, 7, 9, 10, 11, 12, 14, 15.

3.5.6.7 Maximum Payload Size

This setting defines the maximum payload size.
The choices: 128, 256, 512, 1024, 2048, 4096.

3.5.7 PC Health Status

This section shows the status of your CPU, Fan & System.



3.5.7.1 Case Open Warning

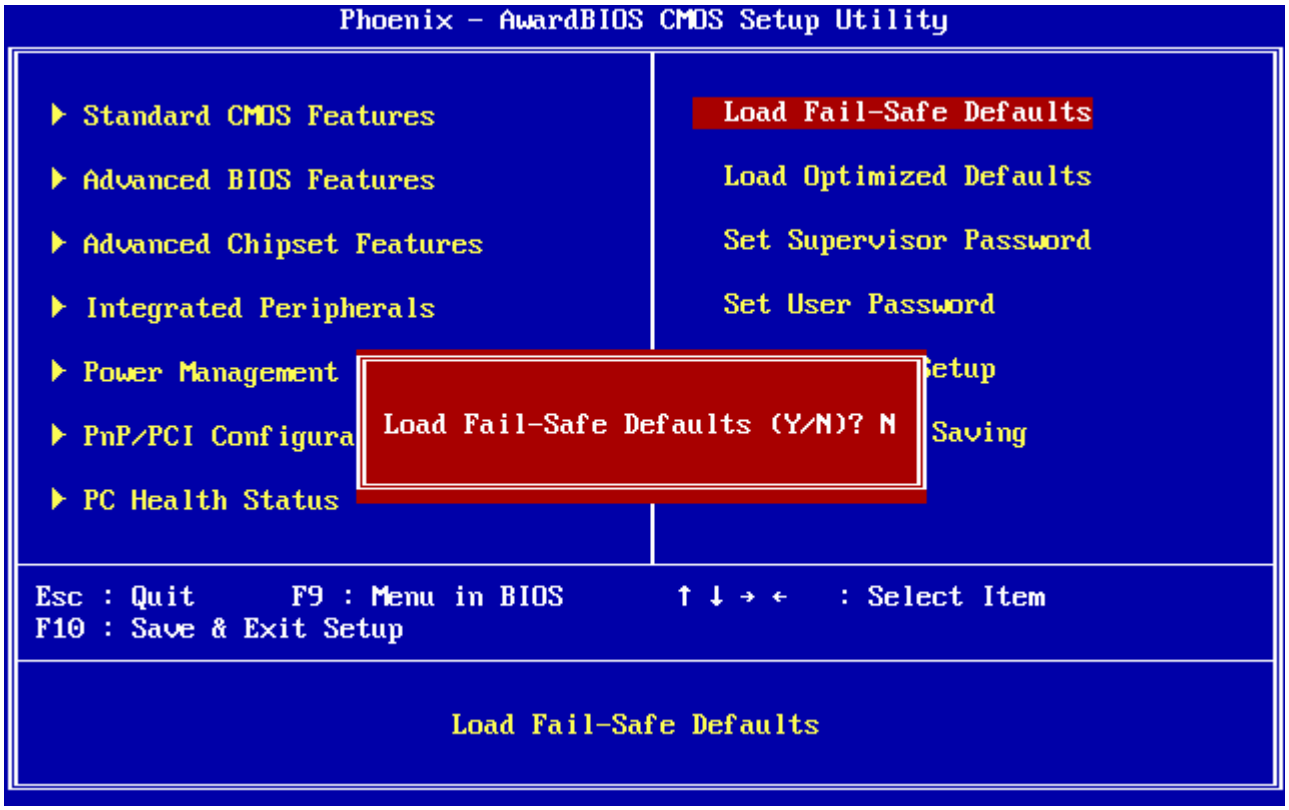
The setting will show a warning when the case has been open.

The choices: Enabled, Disabled

3.5.8 Load Fail-Safe Defaults

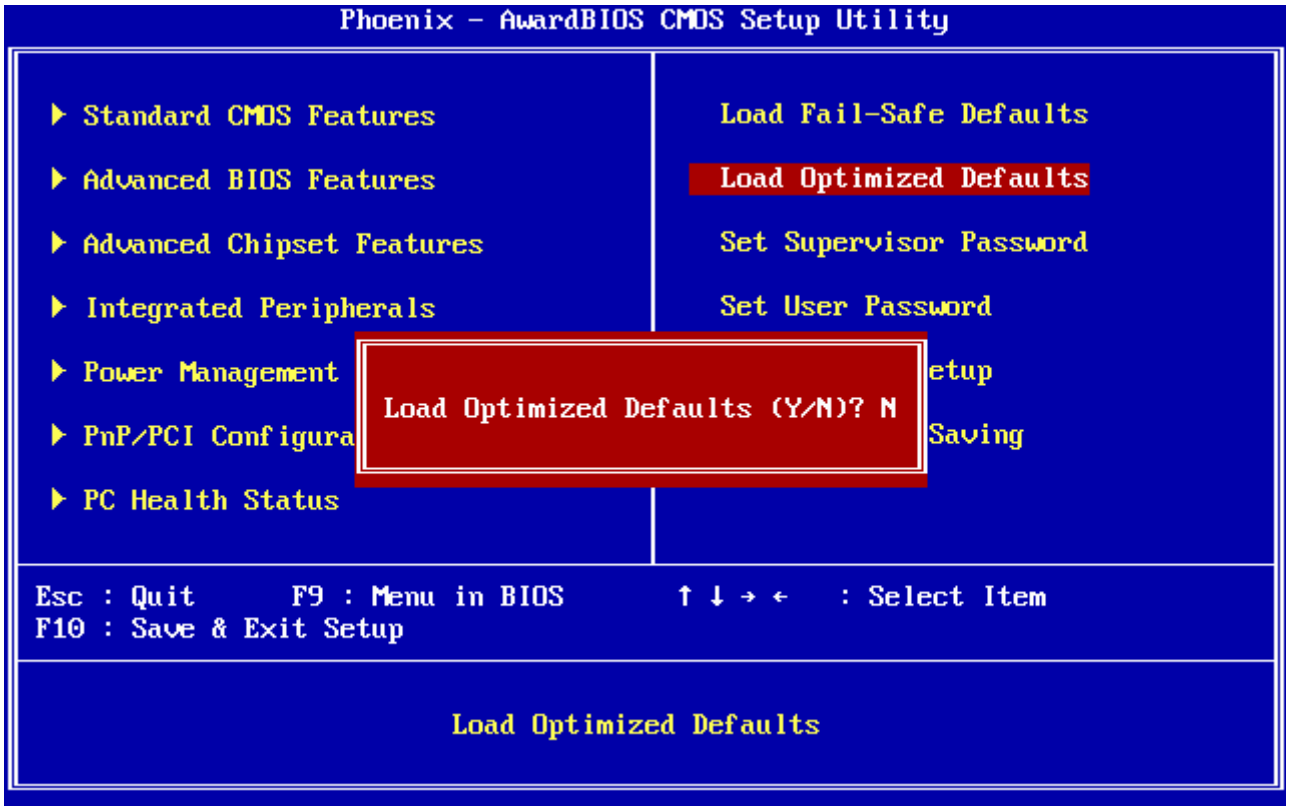
Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

Press <Y> to load the BIOS default values for the most stable, minimal-performance system operations.



3.5.9 Load Optimized Defaults

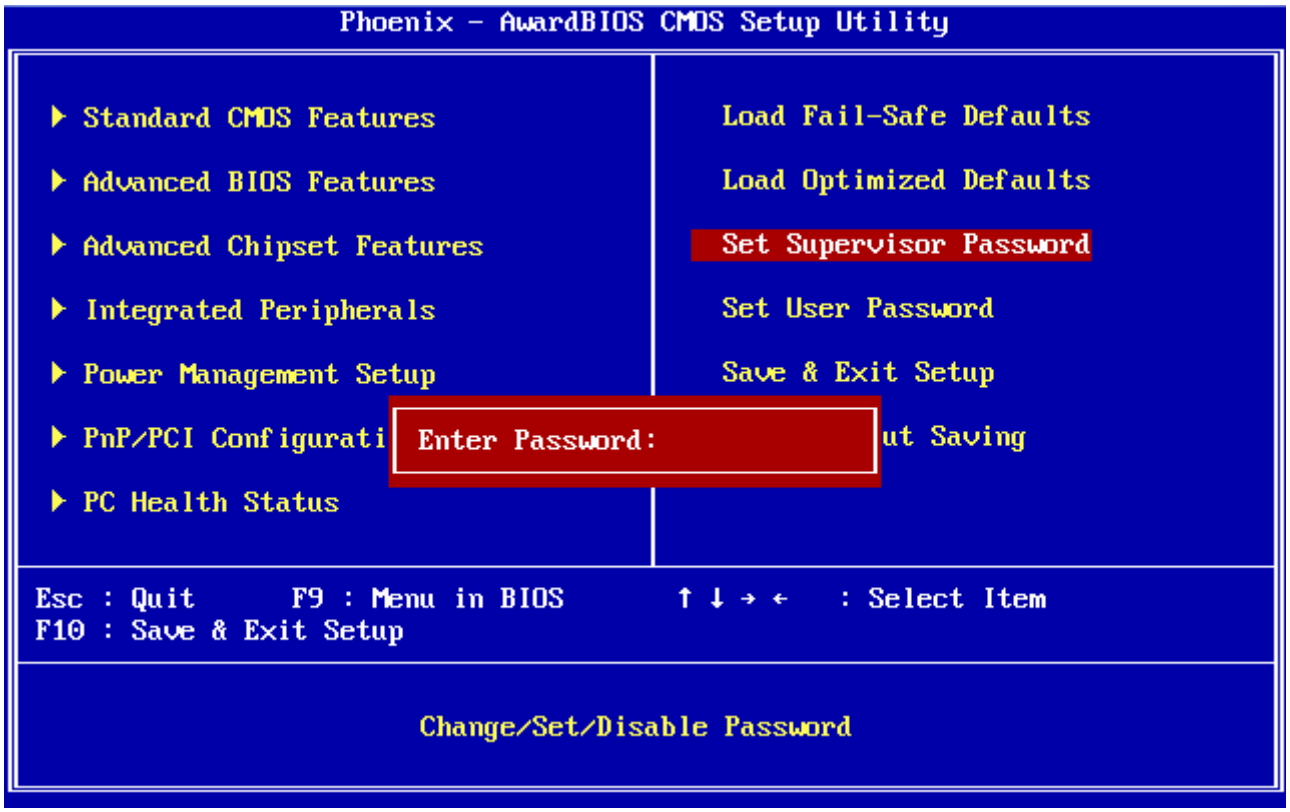
Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.
Press <Y> to load the default values setting for optimal performance system operations.



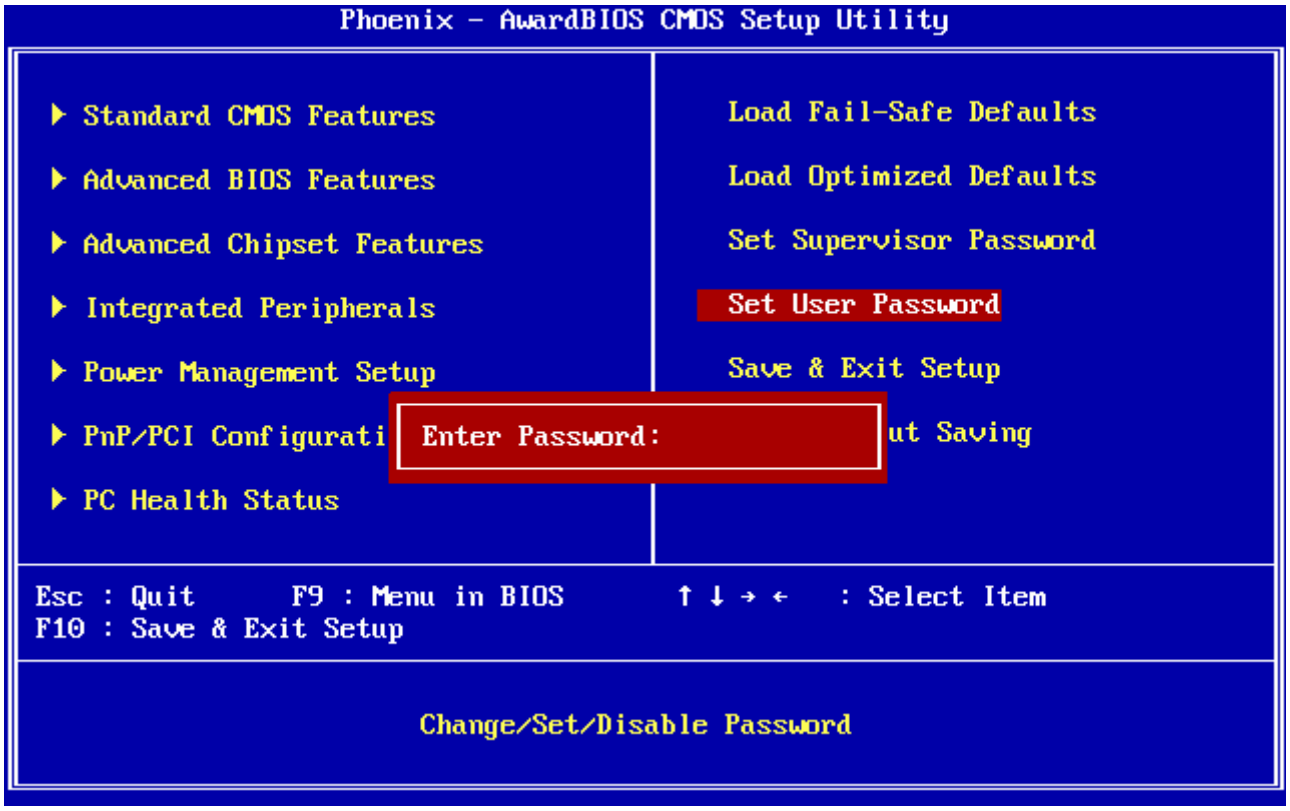
3.5.10 Set Supervisor / User Password

You can set either supervisor or user password, or both of them.

Supervisor Password: able to enter/change the options of setup menus.



User Password: able to enter but no right to change the options of setup menus.



Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

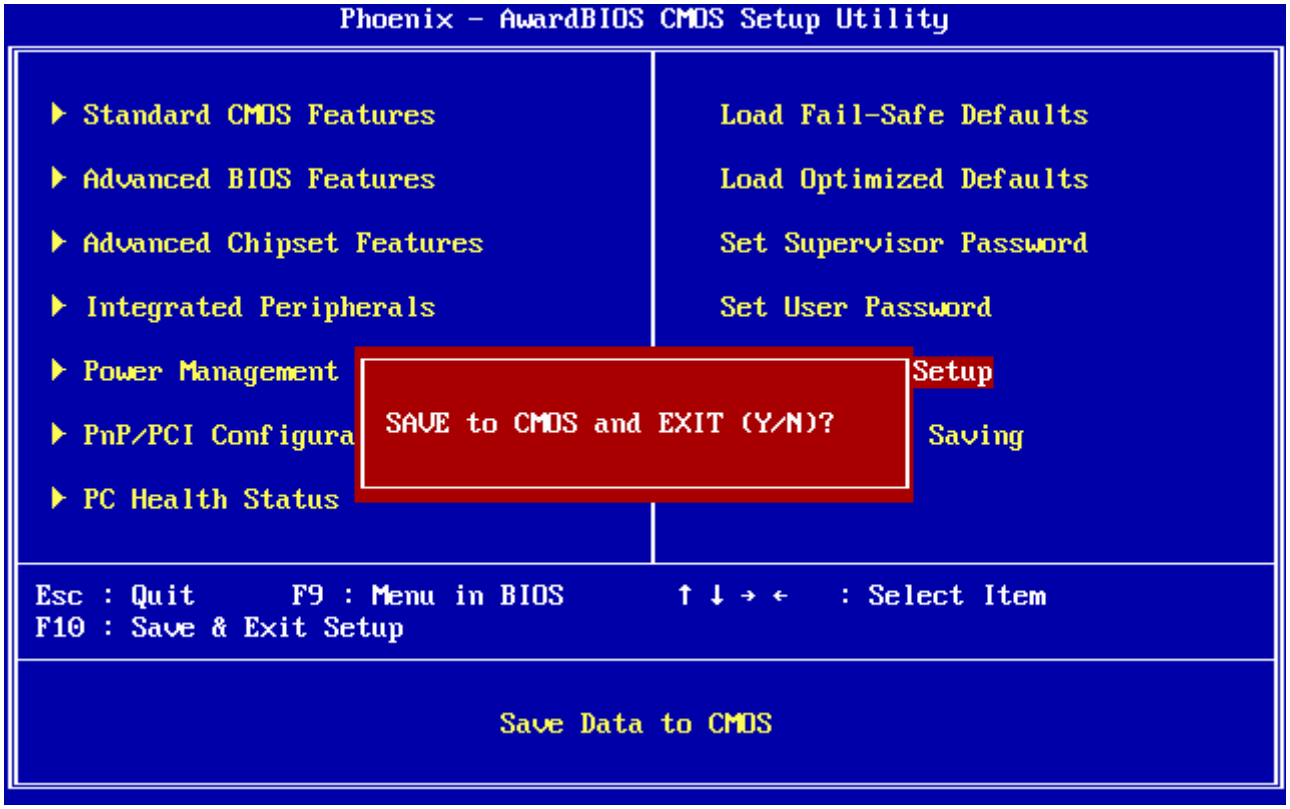
When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration. Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer. You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to "System", the password will be required both at boot and at entry to Setup. If set to "Setup", prompting only occurs when trying to enter Setup.

3.5.11 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

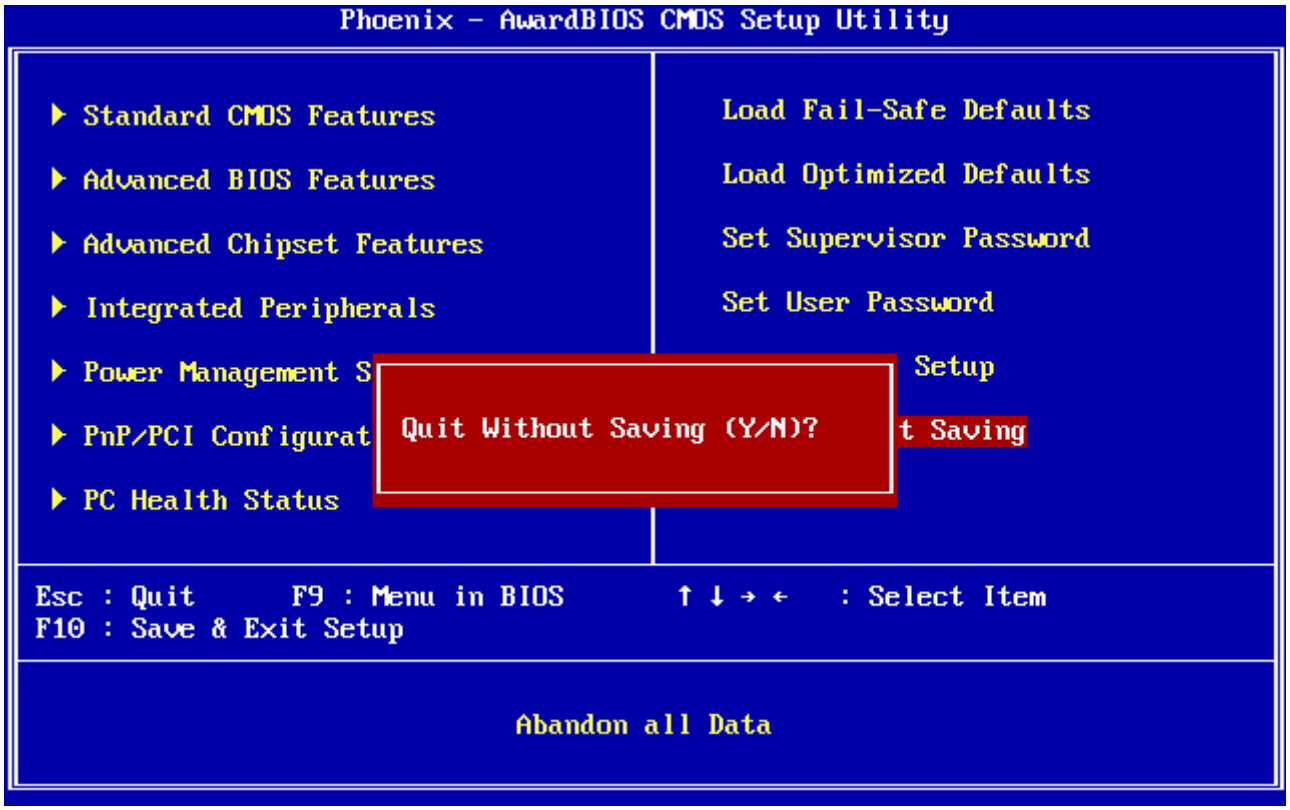
Enter <Y> to store the selection made in the menus in CMOS, a special section in memory that stays on after turning the system off. The BIOS configures the system according to the Setup selection stored in CMOS when boot the computer next time.

The system is restarted after saving the values.



3.5.12 Exit Without Save

Abandon all CMOS value changes and exit setup, and the system is restarted after exiting.



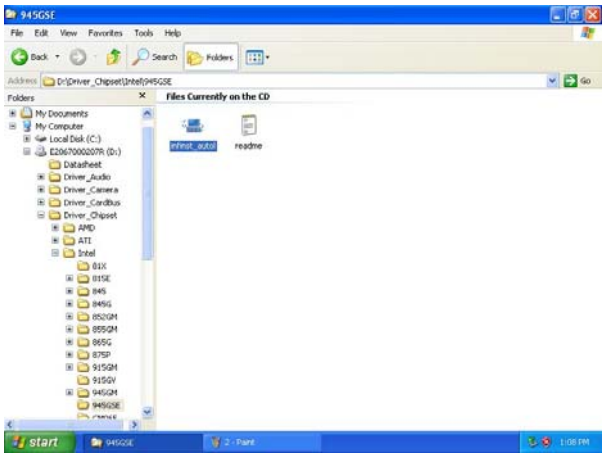
4. Drivers Installation

Note: Installation procedures and screen shots in this section are for your reference and may not be exactly the same as shown on your screen.

4.1 Install Chipset Driver (For Intel 945GSE)

Insert the Supporting DVD-ROM to DVD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\ Driver_Chipset\ Intel\ 945GSE**.

Note: The installation procedures and screen shots in this section are based on Windows XP operation system. If the warning message appears while the installation process, click Continue to go on.



Step1. Locate 「\Driver_Chipset\Intel\ 945GM\ \infinst_autol.exe」.

Step 2. Click **Next**.

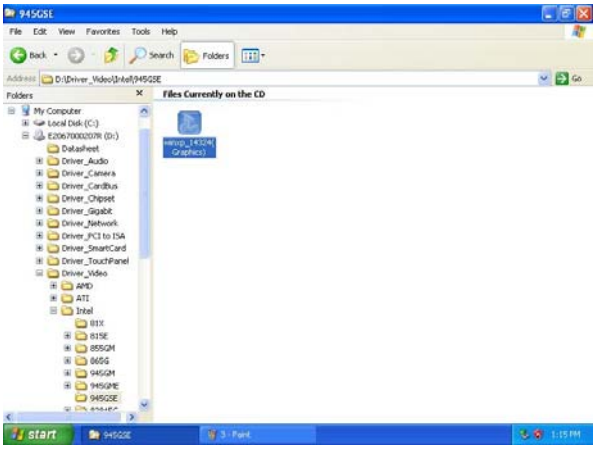
Step 3. Click **Next**.

Step 4. Click **Finish** to complete setup.

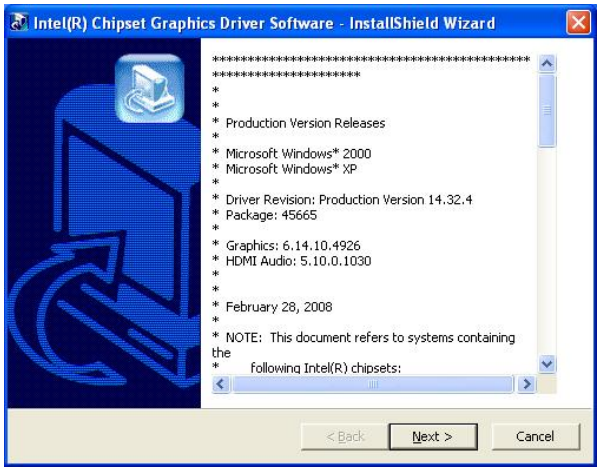
4.2 Install Display Driver (For Intel 945GSE)

Insert the Supporting DVD-ROM to DVD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\ Driver_Video\ Intel\ 945GSE**.

Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



Step 1. Locate「Driver_Video\Intel\ 945GSE\winxp_14324(Graphics).exe」.



Step 2. Click **Next**.

Step 3. Click **Next**.

Step 4. Click **Yes**.

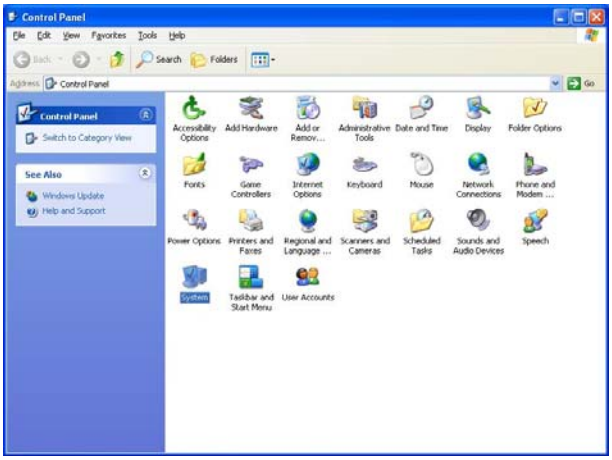
Step 5. Click **Finish** to complete setup.

4.3 Install Ethernet Driver (For Realtek RTL8101L)

Insert the Supporting DVD-ROM to DVD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to

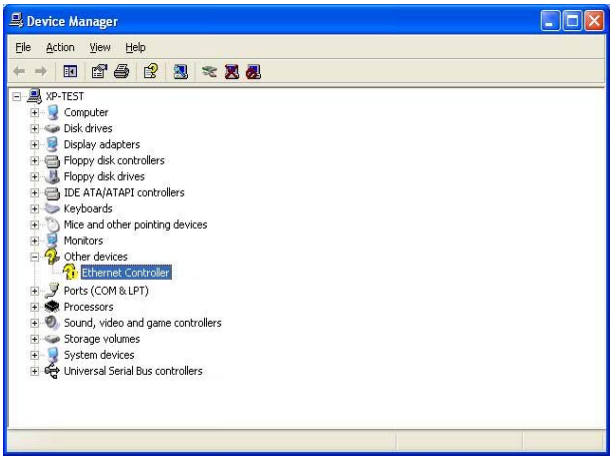
\ Driver_Gigabit\ Realtek\ RTL8101L

Note: The installation procedures and screen shots in this section are based on Windows XP operation system.

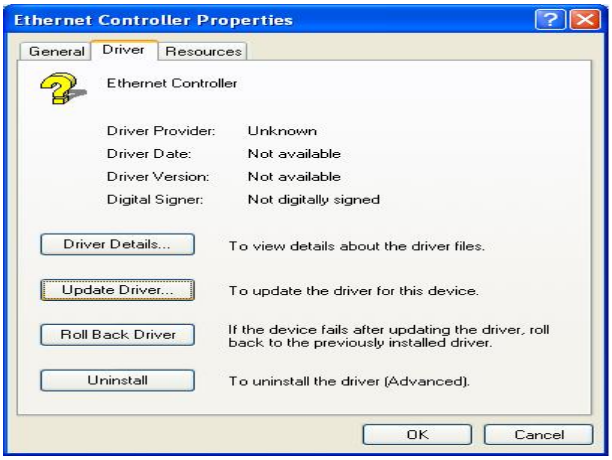


Step 1. Click **Start** of the task bar, then the **System** of **Performance and Maintenance** in **Control Panel**.

Step 2. Click **Device Manager** of **Hardware**.

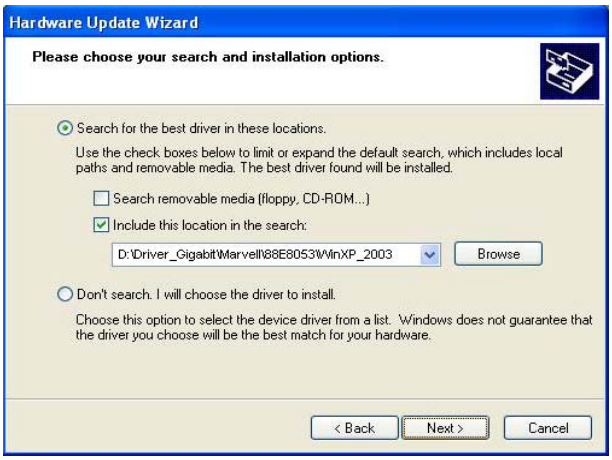


Step 3. Double click **Ethernet Controller**.

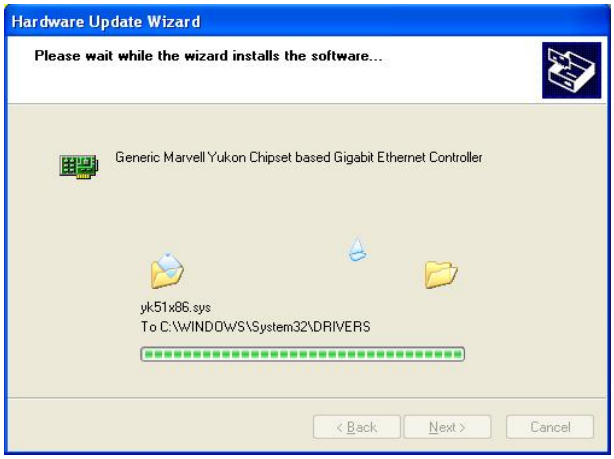


Step 4. Click **Update Driver**.

Step 5. Select the **Advanced** item and click **Next**.

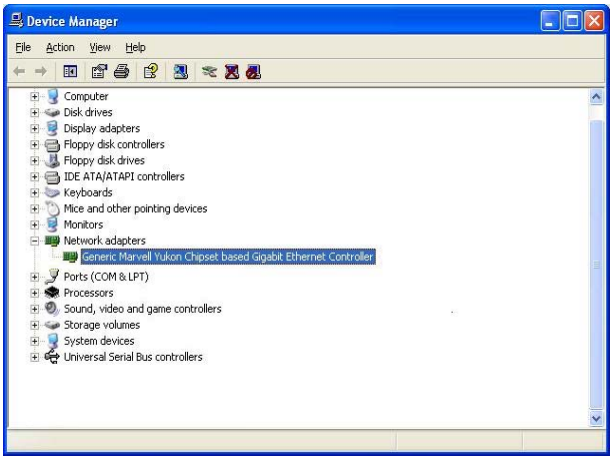


Step 6. Select the specific location to **Next**.



Step 7. The wizard runs the setup automatically.

Step 8. Click **Finish** to complete the installation.



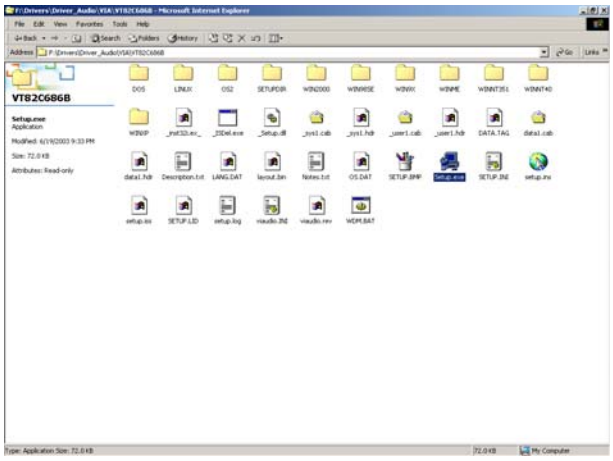
Step 9. Repeat the Step 1 ~ Step 3 to confirm the Generic Marvell is ready.

4.4 Install Audio Driver (For Realtek ALC655)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Avalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\ Driver_Audio\ Intel\ 6300ESB \ ALC655.**

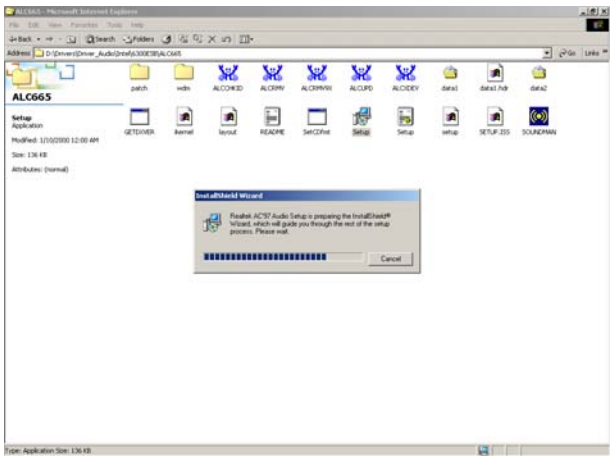
Note: The installation procedures and screen shots in this section are based on Windows 2000 operation system.

Step 3. Select **Yes** to the next step.



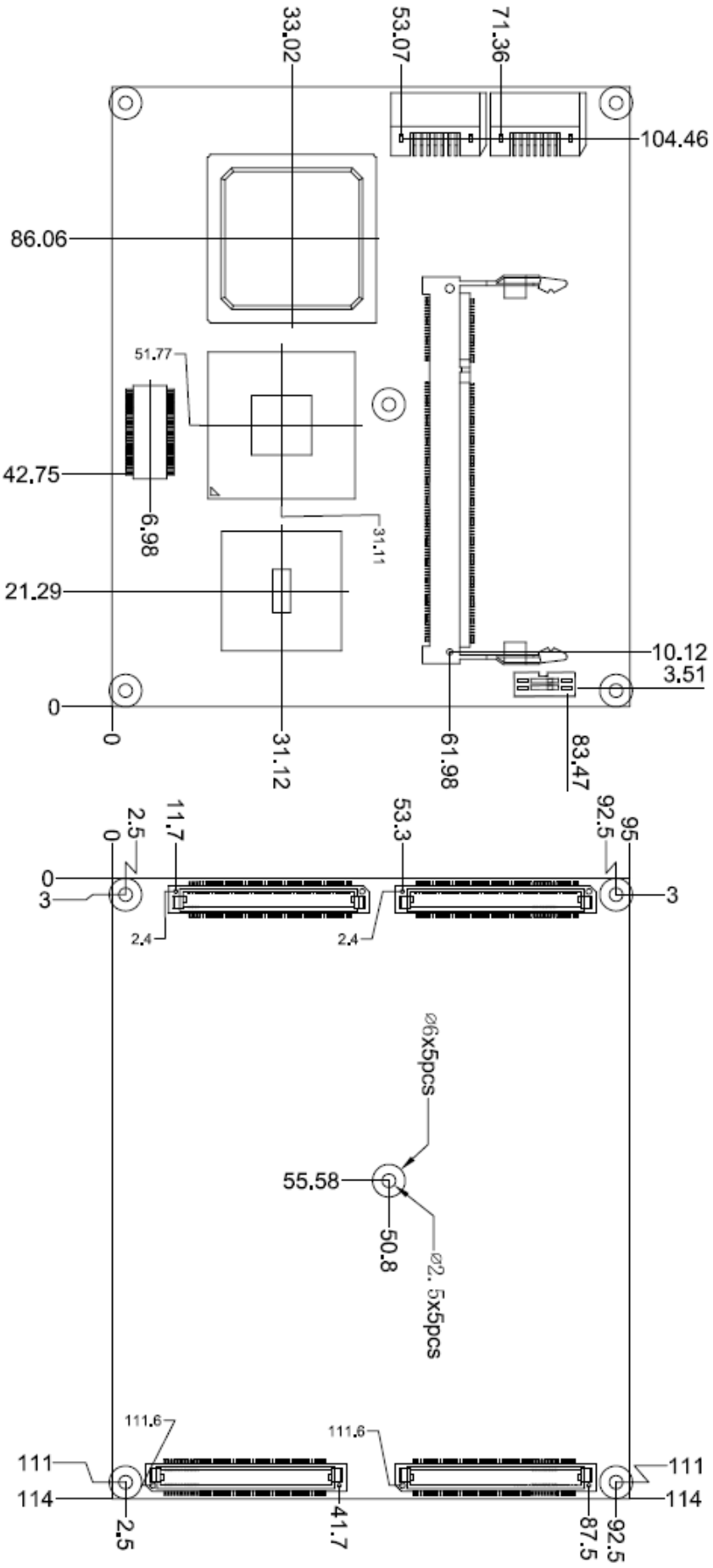
Step 1. Locate 「\Driver_Audio\Intel\ 6300ESB ALC655\setup.exe」.

Step 4. Click **Finish** to complete the setup.



Step 2. The program executes the Setup automatically.

5. Mechanical Drawing


33.02
53.07
71.36
104.46
86.06
51.77
42.75
6.98
31.11
21.29
10.12
3.51
0
0
31.12
61.98
83.47
2.5
11.7
53.3
92.5
95
0
3
3
2.4
2.4
Ø6x5pcs
55.58
50.8
Ø2.5x5pcs
111.6
111.6
111
114
111
114
2.5
41.7
87.5
92.5

Unit: mm

Appendix A: AWARD BIOS POST Messages

Overview

During the Power On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.
If a message is displayed, it will be accompanied by:
PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

Post Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and the EISA BIOS.

1. CMOS BATTERY HAS FAILED

CMOS battery is no longer functional. It should be replaced.

2. CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

3. DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

4. DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

5. DISPLAY SWITCH IS SET INCORRECTLY

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

6. DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

7. EISA Configuration Checksum Error
PLEASE RUN EISA CONFIGURATION UTILITY

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the card is installed firmly in the slot.

8. EISA Configuration Is Not Complete
PLEASE RUN EISA CONFIGURATION UTILITY

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

9. ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

10. ERROR INITIALIZING HARD DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

11. FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

12. Invalid EISA Configuration
PLEASE RUN EISA CONFIGURATION UTILITY

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

13. KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

14. Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

15. Memory parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

16. MEMORY SIZE HAS CHANGED SINCE LAST BOOT

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

17. Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

18. OFFENDING ADDRESS NOT FOUND

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

19. OFFENDING SEGMENT:

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

20. PRESS A KEY TO REBOOT

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

21. PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

22. RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

23. Should Be Empty But EISA Board Found
PLEASE RUN EISA CONFIGURATION UTILITY

A valid board ID was found in a slot that was configured as having no board ID.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

24. Should Have EISA Board But Not Found
PLEASE RUN EISA CONFIGURATION UTILITY

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

25. Slot Not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

26. SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT ...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

27. Wrong Board In Slot
PLEASE RUN EISA CONFIGURATION UTILITY

The board ID does not match the ID stored in the EISA non-volatile memory.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

28. FLOPPY DISK(S) fail (80) → Unable to reset floppy subsystem.
29. FLOPPY DISK(S) fail (40) → Floppy Type dismatch.
30. Hard Disk(s) fail (80) → HDD reset failed.
31. Hard Disk(s) fail (40) → HDD controller diagnostics failed.
32. Hard Disk(s) fail (20) → HDD initialization error.
33. Hard Disk(s) fail (10) → Unable to recalibrate fixed disk.
34. Hard Disk(s) fail (08) → Sector Verify failed.
35. Keyboard is locked out - Unlock the key.

BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

36. Keyboard error or no keyboard present.

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

37. Manufacturing POST loop.

System will repeat POST procedure infinitely while the P15 of keyboard controller is pull low. This is also used for M/B burn in test.

38. BIOS ROM checksum error - System halted.

The checksum of ROM address F0000H-FFFFFH is bad.

39. Memory test fail.

BIOS reports the memory test fail if the onboard memory is tested error.

40. POST Codes

Please take reference to Phoenix-Award website for the latest post codes.

http://www.phoenix.com/en/OEM-ODM/Customer+Services/BIOS/AwardBIOS/Award+Error+Codes.htm

40.1Normal POST Code

Note: EISA POST codes are typically output to port address 300h. ISA POST codes are output to port address 80h.

Code (hex)	Name	Description
C0	Turn Off Chipset and CPU test	OEM Specific-Cache control cache Processor Status (1FLAGS) Verification. Tests the following processor status flags: Carry, zero, sign, overflow, the BIOS sets each flag, verifies They are set, then turns each flag off and verifies it is off. Read/Write/Verify all CPU registers except SS, SP, and BP with data pattern FF and 00. RAM must be periodically refreshed to keep the memory from decaying. This function ensures that the memory refresh function is working properly.
C1	Memory Presence	First block memory detect OEM Specific-Test to size on-board memory. Early chip set initialization Memory presence test OEM chip set routines clear low 64K of memory Test first 64K memory.
C2	Early Memory Initialization	OEM Specific- Board Initialization
C3	Extend Memory DRAM select	OEM Specific- Turn on extended memory Initialization Cyrix CPU initialization, Cache initialization
C4	Special Display Handling	OEM Specific- Display/Video Switch handling so that switch handling display switch errors never occurs
C5	Early Shadow	OEM specific- Early shadow enable for fast boot
C6	Cache presence test	External cache size detection
CF	CMOS Check	CMOS checkup
B0	Spurious	If interrupt occurs in protected mode.
B1	Unclaimed NMI	If unmasked NMI occurs, display Press F1 to disable NMI, F2 reboot.
BF	Program Chip Set	To program chipset from defaults values

E1-EF	Setup Pages	E1- Page 1, E2 - Page 2, etc.
1	Force load Default to chipset	Chipset defaults program
2	Reserved	

Code (hex)	Name	Description
3	Early Superio Init	Early Initialized the super IO
4	Reserved	
5	Blank video	Reset Video controller
6	Reserved	
7	Init KBC	Keyboard controller init
8	KB test	Test the Keyboard
9	Reserved	
A	Mouse Init	Initialized the mouse
B	Onboard Audio init	Onboard audio controller initialize if exist
C	Reserved	
D	Reserved	
E	CheckSum Check	Check the intergraty of the ROM, BIOS and message
F	Reserved	
10	Auto detec EEPROM	Check Flash type and copy flash write/erase routines to 0F000h segments
11	Reserved	
12	Cmos Check	Check Cmos Circuitry and reset CMOS
13	Reserved	
14	Chipset Default load	Program the chipset registers with CMOS values
15	Reserved	
16	Clock Init	Init onboard clock generator
17	Reserved	
18	Identify the CPU	Check the CPU ID and init L1/L2 cache
19	Reserved	
1A	Reserved	
1B	Setup Interrupt Vector Table	Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize INT 00h-1Fh according to INT_TBL
1C	Reserved	
1D	Early PM Init	First step initialize if single CPU onboard
1E	Reserved	
1F	Re-initial KB	Re-init KB
20	Reserved	
21	HPM init	If support HPM, HPM get initialized here

22	Reserved	
23	Test CMOS Interface and battery Status	Verifies CMOS is working correctly, detects bad battery. If failed, load CMOS defaults and load into chipset
24	Reserved	
25	Reserved	
26	Reserved	
27	KBC final Init	Final Initial KBC and setup BIOS data area
28	Reserved	
29	Initialize Video Interface	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter.
2A	Reserved	
2B	Reserved	
2C	Reserved	
2D	Video memory test	Test video memory, write sign-on message to screen. Setup shadow RAM - Enable shadow according to Setup.
2E	Reserved	
2F	Reserved	
30	Reserved	
31	Reserved	
32	Reserved	
33	PS2 Mouse setup	Setup PS2 Mouse and reset KB
34	Reserved	
35	Test DMA Controller 0	Test DMA Controller 0
36	Reserved	
37	Test DMA Controller 1	Test DMA Controller 1
38	Reserved	
39	Test DMA Page Registers	Test DMA Page Registers.
3A	Reserved	
3B	Reserved	
3C	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.
3D	Reserved	
3E	Test 8259-1 Mask Bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.
3F	Reserved	
40	Test 8259-2 Mask Bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines.
41	Reserved	
42	Reserved	

Code (hex)	Name	Description
43	Test Stuck 8259's Interrupt Bits Test 8259 Interrupt Functionality	Turn off interrupts then verify no interrupt mask register is on. Force an interrupt and verify the interrupt occurred.
44	Reserved	
45	Reserved	
46	Reserved	
47	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If not, execute ISA tests an clear EISA mode flag.
48	Reserved	
49	Size Base and Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
4A	Reserved	
4B	Reserved	
4C	Reserved	
4D	Reserved	
4E	Test Base and Extended Memory	Test base memory from 256K to 640K and extended memory above 1MB using various patterns. NOTE: This test is skipped in EISA mode and can be skipped with ESC key in ISA mode.
4F	Reserved	
50	USB init	Initialize USB controller
51	Reserved	
52	Memory Test	Test all memory of memory above 1MB using Virtual 8086 mode, page mode and clear the memory
53	Reserved	
54	Reserved	
55	CPU display	Detect CPU speed and display CPU vendor specific version string and turn on all necessary CPU features
56	Reserved	
57	PnP Init	Display PnP logo and PnP early init
58	Reserved	
59	Setup Virus Protect	Setup virus protect according to Setup
5A	Reserved	
5B	Awdflash Load	If required, will auto load Awdflash.exe in POST
5C	Reserved	
5D	Onboard I/O Init	Initializing onboard superIO

Code (hex)	Name	Description
5E	Reserved	
5F	Reserved	
60	Setup enable	Display setup message and enable setup functions
61	Reserved	
62	Reserved	
63	Initialize & Install Mouse	Detect if mouse is present, initialize mouse, install interrupt vectors.
64	Reserved	
65	PS2 Mouse special	Special treatment to PS2 Mouse port
66	Reserved	
67	ACPI init	ACPI sub-system initializing
68	Reserved	
69	Setup Cache Controller	Initialize cache controller.
6A	Reserved	
6B	Setup Entering	Enter setup check and auto- configuration check up
6C	Reserved	
6D	Initialize Floppy Drive & Controller	Initialize floppy disk drive controller and any drives.
6E	Reserved	
6F	FDD install	Install FDD and setup BIOS data area parameters
70	Reserved	
71	Reserved	
72	Reserved	
73	Initialize Hard Drive & Controller	Initialize hard drive controller and any drives.
74	Reserved	
75	Install HDD	IDE device detection and install
76	Reserved	
77	Detect & Initialize Serial/Parallel Port	Initialize any serial and parallel ports (also game port).
78	Reserved	
79	Reserved	
7A	Detect & Initialize Math Coprocessor	Initialize math coprocessor.
7B	Reserved	
7C	HDD Check for Write protection	HDD check out

Code (hex)	Name	Description
7D	Reserved	
7E	Reserved	
7F	POST error check	Check POST error and display them and ask for user intervention
80	Reserved	
81	Reserved	
82	Security Check	Ask password security (optional).
83	Write CMOS	Write all CMOS values back to RAM and clear screen.
84	Pre-boot Enable	Enable parity checker. Enable NMI, Enable cache before boot.
85	Initialize Option ROMs	Initialize any option ROMs present from C8000h to EFFFFh. NOTE: When FSCAN option is enabled, ROMs initialize from C8000h to F7FFFh.
86	Reserved	
87	Reserved	
88	Reserved	
89	Reserved	
8A	Reserved	
8B	Reserved	
8C	Reserved	
8D	Reserved	
8E	Reserved	
8F	Reserved	
90	Reserved	
91	Reserved	
92	Reserved	
93	Boot Medium detection	Read and store boot partition head and cylinders values in RAM
94	Final Init	Final init for last micro details before boot
95	Special KBC patch	Set system speed for boot. Setup NumLock status according to Setup
96	Boot Attempt	Set low stack Boot via INT 19h.
FF	Boot	

40.2Quick POST Codes

Code (hex)	Name	Description
65	Init onboard device	Early Initialized the super IO. Reset Video controller. Keyboard controller init Test the Keyboard Initialized the mouse Onboard audio controller initialize if exist. Check the intergraty of the ROM, BIOS and message Check Flash type and copy flash write/erase routines to 0F000h segments Check Cmos Circuitry and reset CMOS Program the chipset registers with CMOS values Init onboard clock generator
66	Early Sytem setup	Check the CPU ID and init L1/L2 cache. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and 10 initialize INT 00h-1Fh according to INT_TBL First step initialize if single CPU onboard. Re-init KB If support HPM, HPM get initialized here.
67	KBC and CMOS Init	Verifies CMOS is working correctly, detects bad battery. If failed, load CMOS defaults and load into chipset. Final Initial KBC and setup BIOS data area.
68	Video Init	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter. Test video memory, write sign-on message to screen. Setup shadow RAM - Enable shadow according to Setup.
69	8259 Init	Init 8259 channel 1 and mask IRQ 9
6A	Memory test	Quick Memory Test
6B	CPU Detect and IO init	CPU vendor specific version string and turn on all necessary CPU features Display PnP logo and PnP early init Setup virus protect according to Setup. If required, will auto load Awdflash.exe in POST Initializing onboard superIO
6C	Reserved	
6D	Reserved	
6E	Reserved	
6F	Reserved	
70	Setup Init	Display setup message and enable setup functions Detect if mouse is present, initialize mouse, install interrupt vectors. Special treatment to PS2 Mouse port ACPI sub-system initializing
71	Setup Cache Controller	Initialize cache controller.

Code (hex)	Name	Description
72	Install FDD	Enter setup check and auto11 configuration check up Initialize floppy disk drive controller and any drives. Install FDD and setup BIOS data area parameters
73	Install FDD	Initialize hard drive controller and any drives. IDE device detection and install Initialize any serial and parallel ports (also game port).
74	Detect & Initialize Math Coprocessor	Initialize math coprocessor.
75	HDD Check for Write protection	HDD check out
76	Reserved	
77	Display POST error	Check POST error and display them and ask for user intervention Ask password security (optional).
78	CMOS and Option ROM Init	Write all CMOS values back to RAM and clear screen. Enable parity checker Enable NMI, Enable cache before boot. Initialize any option ROMs present from C8000h to EFFFFh. NOTE: When FSCAN option is enabled, ROMs initialize from C8000h to F7FFFh.
79	Reserved	
7A	Reserved	
7B	Reserved	
7C	Reserved	
7D	Boot Medium detection	Read and store boot partition head and cylinders values in RAM
7E	Final Init	Final init for last micro details before boot
7F	Special KBC patch	Set system speed for boot. Setup NumLock status according to Setup.
80	Boot Attempt	Set low stack Boot via INT 19h.
FF	Boot	

40.3S4 POST Codes

Code (hex)	Name	Description
5A	Early Chipset Init	Early Initialized the super IO. Reset Video controller. Keyboard controller init. Test the Keyboard Initilized the mouse
5B	Cmos Check	Check Cmos Circuitry and reset CMOS
5C	Chipset default Prog	Program the chipset registers with CMOS values. Init onboard clock generator
5D	Identify the CPU	Check the CPU ID and init L1/L2 cache Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and INT 00h-1Fh according to INT_TBL. First step initialize if single CPU Onboard. Re-init KB If support HPM, HPM get initialized Here.
5E	Setup Interrupt Vector Table	Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and INT 00h-1Fh according to INT_TBL. First step initialize if single CPU Onboard. Re-init KB If support HPM, HPM get initialized here.
5F	Test CMOS Interface and Battery status	Verifies CMOS is working correctly, detects bad battery. If failed, load CMOS defaults and load into chipset.
60	KBC final Init	Final Initial KBC and setup BIOS data area
61	Initialize Video Interface	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter.
62	Video memory test	Test video memory, write sign-on Test video memory, write sign-on message to screen. Setup shadow RAM - Enable shadow according to Setup.
63	Setup PS2 mouse and test DMA	Setup PS2 Mouse and reset KB Test DMA channel 0
64	Test 8259	Test 8259 channel 1 and mask IRQ 9
65	Init Boot Device	Detect if mouse is present, initialize mouse, install interrupt vectors. Special treatment to PS2 Mouse port ACPI sub-system initializing Initialize cache controller.
66	Install Boot Devices	Enter setup check and auto-configuration check up Initialize floppy disk drive controller and any drives. Install FDD and setup BIOS data area Parameters Initialize hard drive controller and any drives. IDE device detection and install
67	Cache Init	Cache init and USB init
68	PM init	PM initialization
69	PM final Init and issue SMI	Final init Before resume
FF	Full on	

40.4BootBlock POST Codes

Code (hex)	Name	Description
1	Base memory test	Clear base memory area (0000:0000--9000:ffffh)
5	KB init	Initialized KBC
12	Install interrupt vectors	Install int. vector (0-77), and initialized 00-1fh to their proper place
0D	Init Video	Video initializing
41	Init FDD	Scan floppy and media capacity for onboard superIO
FF	Boot	Load boot sector