Specification for Approval

Product No. : FG12864146B-FFS-01

Customer : _____

Prepared by	Checked by	Approved by
YangXiaocong	**Liwentao**	**Yaofuheng**

Customer Approval	☑ Accept ○ Reject Comment:  Approved by: 2024-06-10

Your confirmation of this specification is very important! It's undoubted this attached specification will be regarded as your approval once you confirmed our LCM sample. Also, further mass production will subject to this specification .

DOCUMENT REVISION HISTORY

Sample Version	DOC. Version	DATE	DESCRIPTION	CHANGED BY
A0	00	2024-05-29	First Design	YXC

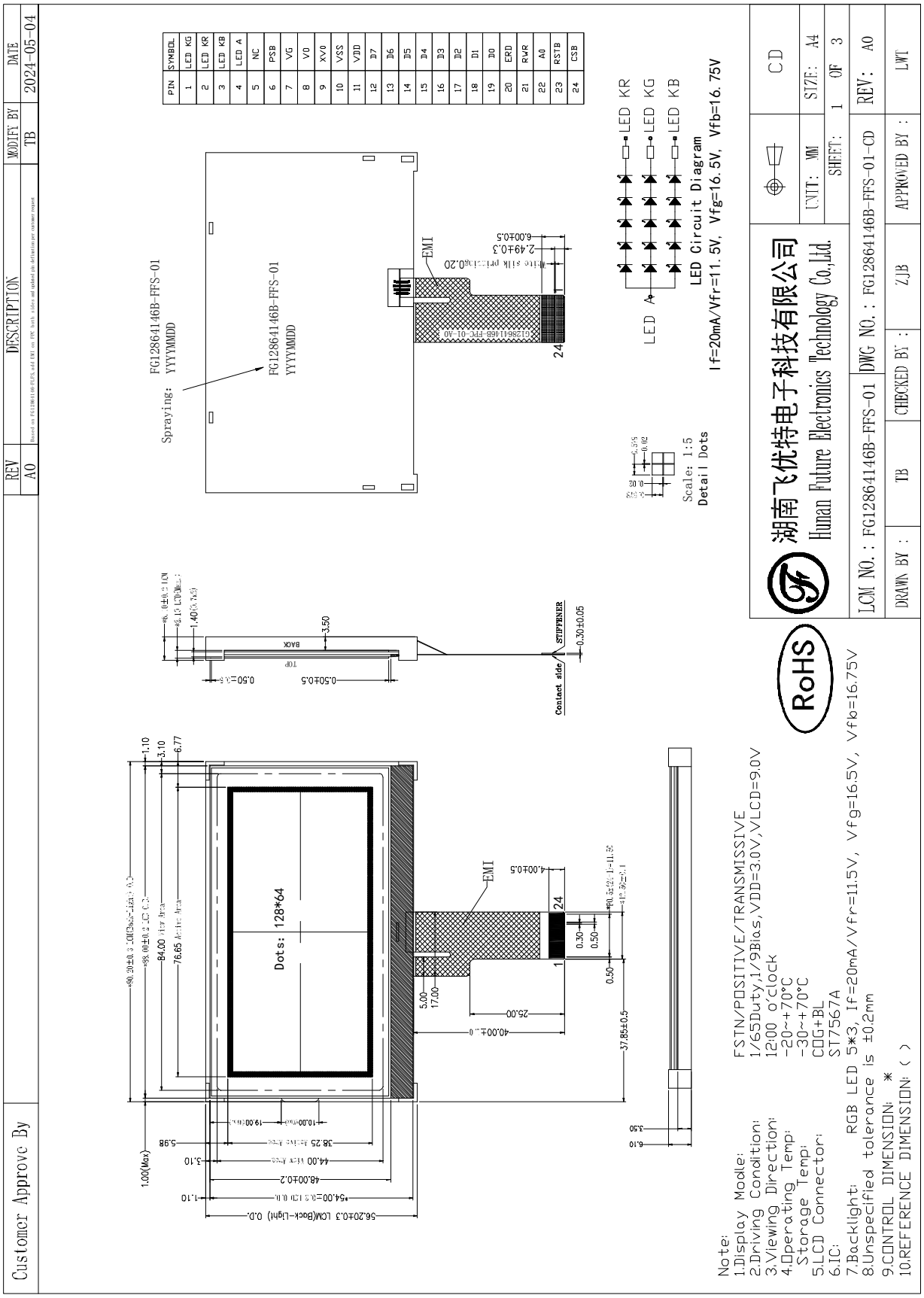
Directory

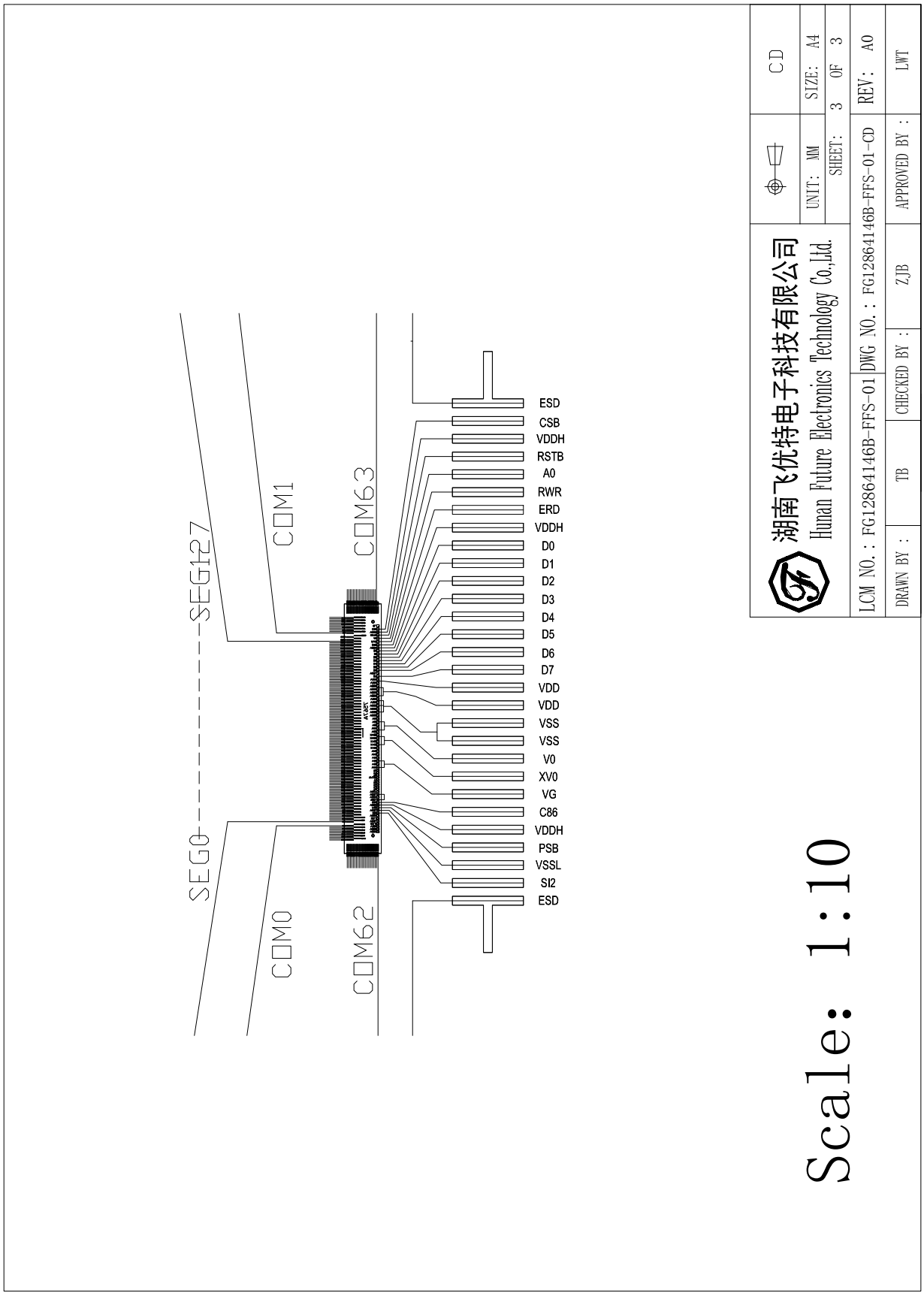
1 FUNCTION & FEATURES

ITEM	Normal dimensions
Display Format	128*64 DOTS
Module dimension	90.2(W)*56.2(H)*6.1(T)MM
Viewing area	84(W)*44(H) MM
Duty/bias	1/65DUTY,1/9BIAS
LCD mode	FSTN/POSITIVE/TRANSMISSIVE
Viewing direction	12:00 O'clock

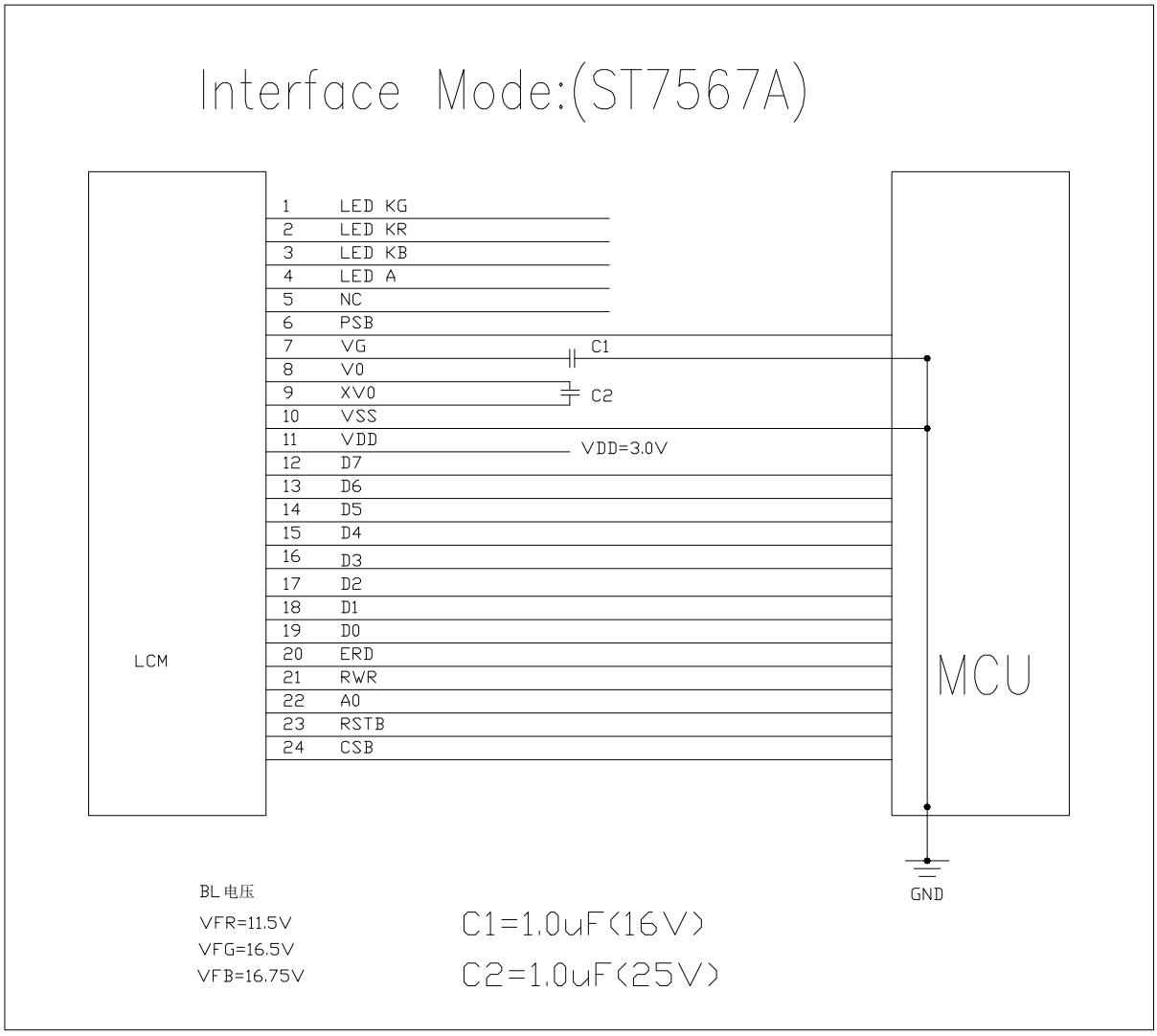
2 BLOCK DIAGRAM

3 DIMENSIONAL CD DRAWING




SEG0
SEG127
COM0
COM1
COM62
COM63
ESD
CSB
VDDH
RSTB
A0
RWR
ERD
VDDH
D0
D1
D2
D3
D4
D5
D6
D7
VDD
VDD
VSS
VSS
V0
XV0
VG
C86
VDDH
PSB
VSSL
SI2
ESD
湖南飞优特电子科技有限公司
Hunan Future Electronics Technology Co.,Ltd.
CD
UNIT: MM
SIZE: A4
SHEET: 3 OF 3
LCM NO.: FG12864146B-FFS-01
DWG NO.: FG12864146B-FFS-01-CD
REV: A0
DRAWN BY : TB
CHECKED BY : ZJB
APPROVED BY : LWT
Scale: 1:10

4 POWER SUPPLY



5 PIN DESCRIPTION

<table>
<tr><th>Pin no.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>LED KG</td><td>BL Ground.</td></tr>
<tr><td>2</td><td>LED KR</td><td>BL Ground.</td></tr>
<tr><td>3</td><td>LED KB</td><td>BL Ground.</td></tr>
<tr><td>4</td><td>LED A</td><td>BL Power .</td></tr>
<tr><td>5</td><td>NC</td><td>NC</td></tr>
<tr><td>6</td><td>PSB</td><td>PSB selects the interface type: Serial or Parallel.</td></tr>
<tr><td>7</td><td>VG</td><td>VG is the LCD driving voltage for segment circuits.</td></tr>
<tr><td>8</td><td>V0</td><td>V0 is the LCD driving voltage for common circuits at negative frame.</td></tr>
<tr><td>9</td><td>XV0</td><td>XV0 is the LCD driving voltage for common circuits at positive frame.</td></tr>
<tr><td>10</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>11</td><td>VDD</td><td>Power .</td></tr>
<tr><td>12-19</td><td>D7-D0</td><td>When using 8-bit parallel interface: (6800 or 8080 mode)
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When CSB is non-active (CSB="H"), D[7:0] pins are high impedance.
When using serial interface: 4-line SPI, 3-line SPI or I2C serial interface
D[0]=SCL: Serial clock input.
D[1]=SDA_IN: Serial data input.
D[2:3]=SDA_OUT: Serial data output.
D[1:3] must be connected together as SDA.
D[4:7]=(1,1,1,1): ID Pin. D[4:7] should fix to "H" or "L" by VDDH or VSSL.
ID[0:3] can be read 4-bit ID only for serial interface from D[4:7].</td></tr>
<tr><td>20</td><td>ERD</td><td>Read/Write execution control pin. When PSB is "H",
<table>
<tr><th>C86</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W="H": When E is "H", D[7:0] are in output mode.
R/W="L": Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is "L", D[7:0] are in output mode.</td></tr>
</table>
ERD is used to decide slave address (SA0) in I2C serial interface.
ERD is not used in 3-Line and 4-Line SPI interface and should fix to "H" by VDD1 or VDDH.</td></tr>
<tr><td>21</td><td>RWR</td><td>Read/Write execution control pin. When PSB is "H",
<table>
<tr><th>C86</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W="H": read.
R/W="L": write.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
RWR is used to decide slave address (SA1) in I2C serial interface.
RWR is not used in 3-line and 4-line SPI interface and should fix to "H" by VDD1 or VDDH.</td></tr>
<tr><td>22</td><td>A0</td><td>It determines whether the access is related to data or command.
A0="H" : Indicates that signals on D[7:0] are display data.
A0="L" : Indicates that signals on D[7:0] are command.</td></tr>
<tr><td>23</td><td>RSTB</td><td>Hardware reset input pin. When RSTB is "L", internal initialization is executed and the internal registers will be initialized.</td></tr>
<tr><td>24</td><td>CSB</td><td>Chip select input pin. Interface access is enabled when CSB is "L".
When CSB is non-active (CSB="H"), D[7:0] pins are high impedance.</td></tr>
</table>

6 MAXIMUM ABSOLUTE LIMIT (T=25℃)

Item	Symbol	Standard value	Unit
supply voltage	V_{DD}	-0.3~4	V
LCD power supply voltage	V0-XV0	-0.3~18	V
Input Voltage	VIN	-0.3 to VDD1+0.3	V
Operating temperature	Topr	-20~+70	°C
Storage temperature	Tstg	-30~+70	°C

7 ELECTRICAL CHARACTERISTICS

7.1 DC Characteristics(T=30°C~+85℃，VSS=0V)

Item	Symbol	Min	Type	Max	Unit	Test condition
Operating Voltage	VDD	-	3.0	-	V	
Input voltage	VIL	VSS1	-	0.3VDD1	V	-
	VIH	0.7VDD1	-	VDD1	V	
Output voltage	VOL	VSS1	-	0.2VDD1	V	-
	VOH	0.8VDD1	-	VDD1	V	-
LCD driving voltage	VLCD	8.8	9.0	9.2	V	-

Note：VSS=0V.

7.2 Backlight Specifications Absolute maximum rating(Ta=25°C)

Item	Symbol	Min	Typ	Max	Unit	Condition
Forward voltage	VFR	-	11.5	-	V	If=20mA
Forward voltage	VFG	-	16.5	-	V	If=20mA
Forward voltage	VFB	-	16.75	-	V	If=20mA
Color	RGB					

7.3 Electro-Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark	Note
Viewing angle range		θ (Cr ⩾2)	Φ = 90⁰	--	25	---	deg	FIG 5.	6
			Φ= 270⁰	--	35	---	deg	FIG 5.	6
			Φ = 0⁰	--	35	---	deg	FIG 5.	6
			Φ= 180⁰	--	35	---	deg	FIG 5.	6
Response time		Tr	θ=0⁰ Φ=0⁰ Ta=25℃	---	250	---	ms	FIG.3	4
		Tf		---	200	---	ms	FIG.3	4
Contrast ratio		Cr		---	---	---	---	FIG 4.	1
Luminance uniformity		δ RGB		75	---	---	%	FIG 4.	3
Surface Luminance		Lv		---	150	---	cd/m²	FIG 4.	2
CIE(x,y) chromaticity	White	x	θ=0⁰ Φ=0⁰ Ta=25℃	---	---	---	---	FIG 4.	5
		y		---	---	---	---		

Note 1. Contrast Ratio(CR) is defined mathematically as For more information see FIG 4.:

$$\textbf{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels } \mathbf{(P_1, P_2, P_3, P_4, P_5)}}{\text{Average Surface Luminance with all black pixels } \mathbf{(P_1, P_2, P_3, P_4, P_5)}}$$

Note 2. Surface luminance is the center point across the LCD surface 500mm from the surface with all pixels displaying white. For more information see FIG 4.

Lv = Average Surface Luminance with all white pixels **(P_1, P_2, P_3, P_4, P_5)**

Note 3. The uniformity in surface luminance , δ WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the maximum luminance of 5 points luminance by minimum luminance of 5 points luminance. For more information see FIG 4.

$$\delta_{WHITE} = \frac{\textbf{Minimum} \text{ Surface Luminance with all white pixels } \mathbf{(P_1, P_2, P_3, P_4, P_5)}}{\textbf{Maximum} \text{ Surface Luminance with all white pixels } \mathbf{(P_1, P_2, P_3, P_4, P_5)}}$$

Note 4. Response time is the time required for the display to transition from White to black(Rise Time, Tr) and from black to white(Decay Time, Tf). For additional information see FIG 3.

Note 5. CIE (x, y) chromaticity,The x,y value is determined by measuring luminance at each test position 1 through 5,and then make average value

Note 6. Viewing angle is the angle at which the contrast ratio is greater than 2,for TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 5.

FIG.1 Optical Characteristic Measurement Equipment and Method

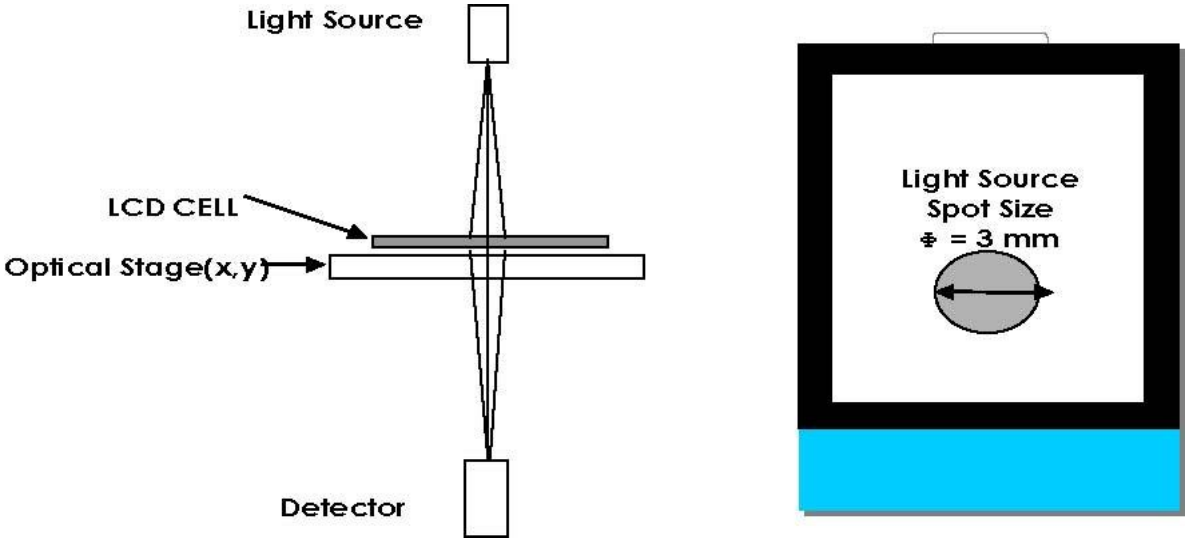


FIG.2 Measuring method for optical characteristics in Reflective mode

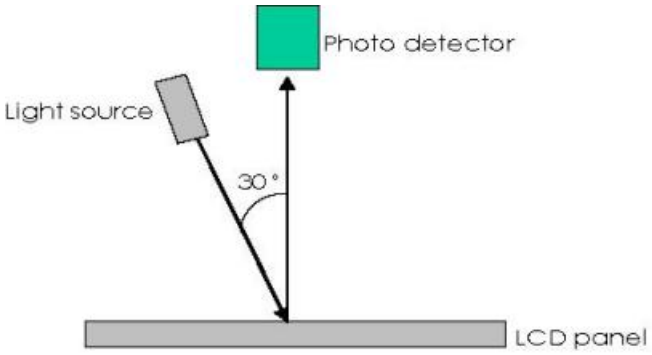
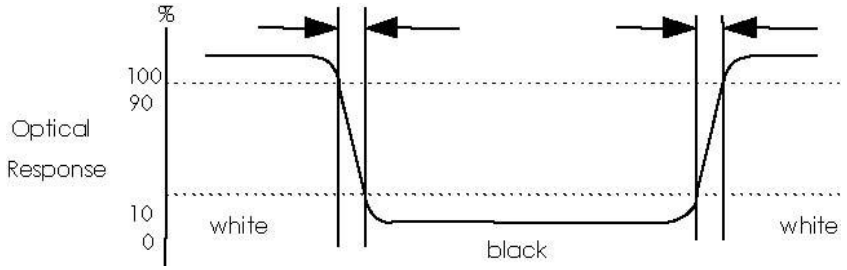


FIG. 3 The definition of Response Time

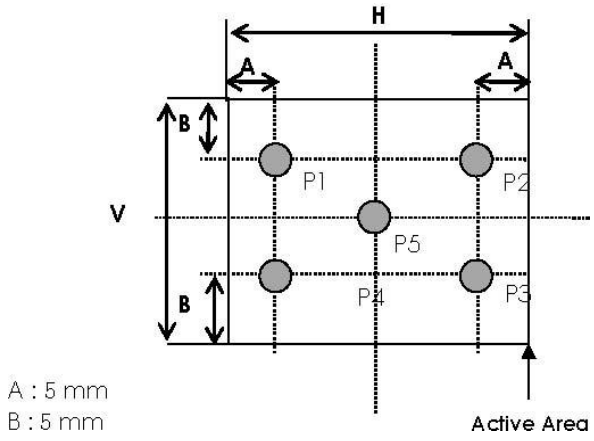
The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.



The values specified are at an approximate distance 500 mm from the LCD surface at a viewing angle of and equal to 0° . Measurement condition : back-light source , with polarizer

FIG. 4 Measuring method for Contrast ratio,surface luminance, Luminance uniformity , CIE (x, y) chromaticity

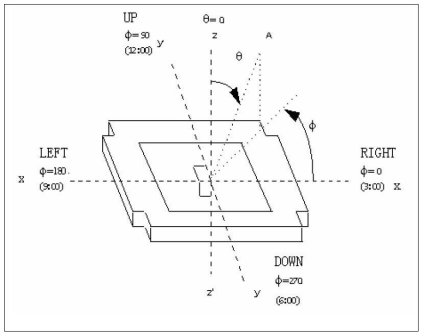
<measuring point for luminance variation> <measuring point for surface luminance>



Light source spot size =2mm , H,V : Active Area,
measurement device is TOPCON luminance meter BM-7

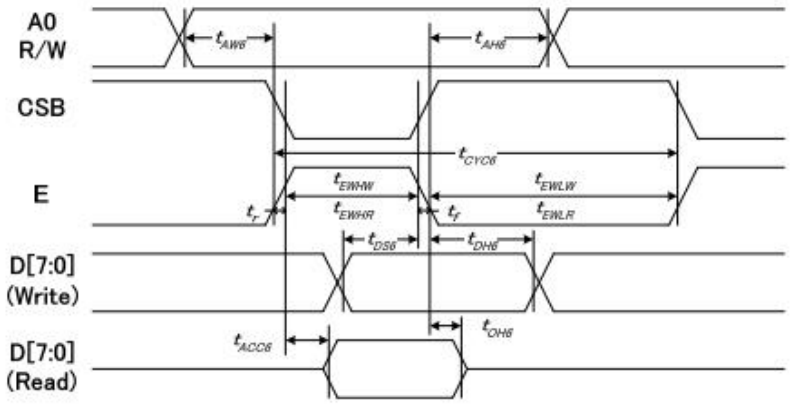
FIG. 5 The definition of viewing angle

<dimension of viewing angle range>



7.4 AC Characteristics

14-1 System Bus Timing for 6800 Series MPU



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		10	—	
System cycle time	E	tCYC6		240	—	
Enable L pulse width (WRITE)		tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)		tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140	—	
Write data setup time	D[7:0]	tDS6		40	—	
Write data hold time		tDH6		10	—	
Read data access time		tACC6	CL = 16 pF	—	70	
Read data output disable time		tOH6	CL = 16 pF	5	50	

(VDD1 = 2.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		400	—	
Enable L pulse width (WRITE)		tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)		tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
Write data setup time	D[7:0]	tDS6		40	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 16 pF	—	140	
Read data output disable time		tOH6	CL = 16 pF	10	100	

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		640	—	
Enable L pulse width (WRITE)		tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)		tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
Write data setup time	D[7:0]	tDS6		80	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 16 pF	—	240	
Read data output disable time		tOH6	CL = 16 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC6 - tEWLW - tEWHW) for (tr + tf) ≦ (tCYC6 - tEWLR - tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being "L" and E.

8 Instruction Description

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
(2) Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
(3) Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
(4)Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
(5) Read Status	0	1	0	MX	D	RST	0	0	0	0	Read IC Status
(6) Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
(7) Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
(8) SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
(9) Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
(10) All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
(11) Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
(12) Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
(13) END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
(14) RESET	0	0	1	1	1	0	0	0	1	0	Software reset
(15) COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
(16) Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
(17) Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
(18) Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
(19) Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL=0: 4X BL=1: 5X
	0	0	0	0	0	0	0	0	0	BL	
(20) Power Save	0	0	Compound Command								Display OFF + All Pixel ON
(21) NOP	0	0	1	1	1	0	0	0	1	1	No operation
(22) Set N-Line	0	0	1	0	0	0	0	1	0	1	Set N-Line inversion
	0	0	0	0	0	NL4	NL3	NL2	NL1	NL0	
(23) Release N-Line	0	0	1	0	0	0	0	1	0	0	Exit N-Line inversion
(24) SPI Read Status	0	1	1	1	1	1	1	1	0	0	SPI read status command
	0	1	0	MX	D	RST	ID3	ID2	ID1	ID0	
(25) SPI Read DDRAM	0	1	1	1	1	1	1	1	0	1	SPI read DDRAM command
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
EXTENSION COMMAND SET											
Extension Command Set	0	0	1	1	1	1	1	1	1	Mode	Mode=1: Enter extension command table Mode=0: Exit extension command table
(1) High Power Mode ON	0	0	0	1	1	0	1	0	1	1	Enter high power mode
(2) High Power Mode OFF	0	0	0	1	1	0	0	1	0	0	Exit high power mode
(3) Display Setting Mode	0	0	0	1	1	1	-	-	DSM	0	Complex command DSM=1: Enter display setting DSM=0: Exit display setting When DSM=1, Set duty(DT[3:0]), bias(BA[2:0]), frame rate(FR[2:0])
	0	0	1	1	0	1	DT3	DT2	DT1	DT0	
	0	0	1	0	0	1	0	BA2	BA1	BA0	
	0	0	1	0	0	1	1	FR2	FR1	FR0	

Note: 1. Symbol "-" means this bit can be "H" or "L".
2. Do not use instructions not listed in these tables.

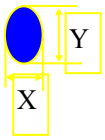
9 QUALITY SPECIFICATIONS

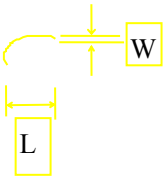
9.1 Defect classification

Classify	Item		Note	AQL
Major	Display state	Short or open circuit	1	0.65
		Contrast defect (dim, ghost)		
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction	2	
		Wrong Back-light	7	
	Non-display	Flat cable or pin reverse	9	
		Wrong or missing component	10	
Minor	Display state	Background color deviation	2	1.5
		Black spot and dust	3	
		Line defect	4	
		Scratch		
		Rainbow	5	
		Pin hole	6	
	Polarizer	Bubble and foreign material	3	
		Scratch	4	
	PCB	Scratch	4	
	Soldering	Poor connection	8	
	Wire	Poor connection	9	

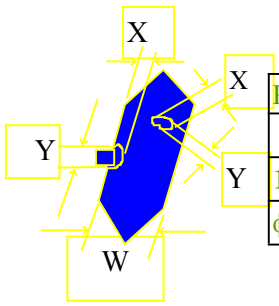
9.2 Note on defect classification

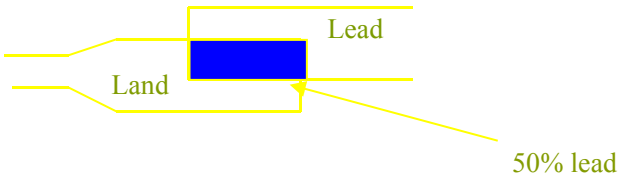
<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td rowspan="6">1</td><td>Short or open circuit</td><td rowspan="6">Not allow</td></tr>
<tr><td>LC leakage</td></tr>
<tr><td>Flickering</td></tr>
<tr><td>No display</td></tr>
<tr><td>Wrong viewing direction</td></tr>
<tr><td>Wrong Back-light</td></tr>
<tr><td rowspan="2">2</td><td>Contrast defect</td><td rowspan="2">Refer to approval sample</td></tr>
<tr><td>Background color deviation</td></tr>
<tr><td>3</td><td>Point defect,
Black spot, dust
(incl. Polarizer)

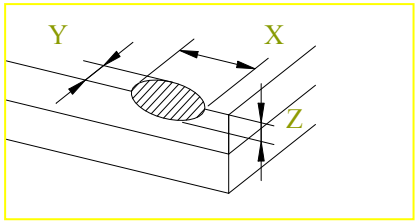
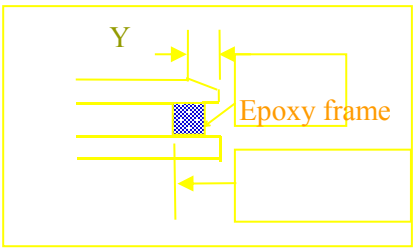
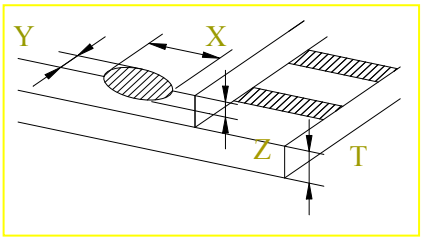
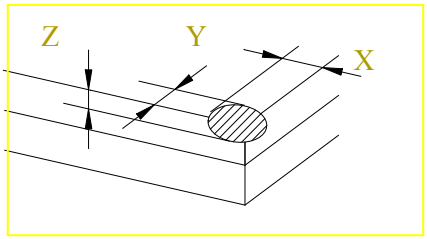
ϕ = (X+Y)/2</td><td> 

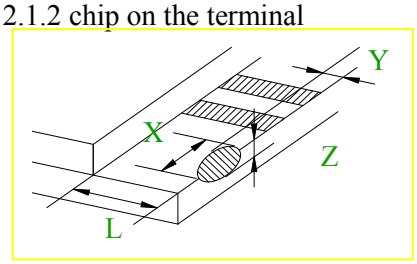
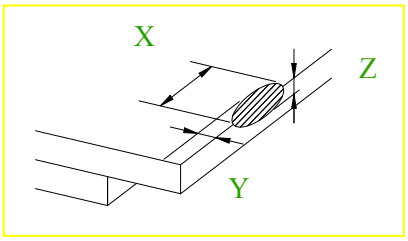
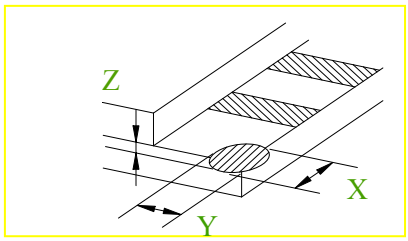
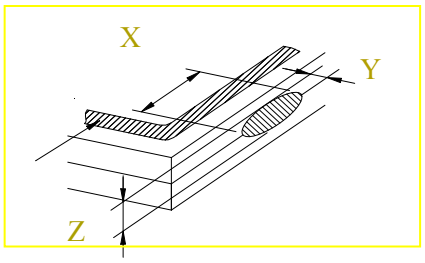
<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>ϕ≤0.10</td><td>Disregard</td></tr>
<tr><td rowspan="2">0.10<ϕ≤0.15</td><td>Positive:3</td></tr>
<tr><td>Negative:2</td></tr>
<tr><td rowspan="2">0.15<ϕ≤0.2</td><td>Positive:2</td></tr>
<tr><td>Negative:1</td></tr>
<tr><td>ϕ>0. 2</td><td>0</td></tr>
</table>
Unit：mm</td></tr>
<tr><td>4</td><td>Line defect</td><td> 

<table>
<tr><th colspan="2">Line</th><th>Acceptable Qty.</th></tr>
<tr><td>L</td><td>W</td><td></td></tr>
<tr><td>---</td><td>0.015≥W</td><td>Disregard</td></tr>
<tr><td>3.0≥L</td><td>0.03≥W</td><td rowspan="2">2</td></tr>
<tr><td>2.0≥L</td><td>0.05≥W</td></tr>
<tr><td>1.0≥L</td><td>0.1＞W</td><td>1</td></tr>
<tr><td>---</td><td>0.05<W</td><td>Applied as point defect</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>5</td><td>Rainbow</td><td>Not more than two color changes across the viewing area.</td></tr>
</table>

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>6</td><td>Segment
pattern
W = Segment width
ϕ = (X+Y)/2</td><td>(1) Pin hole
ϕ < 0.10mm is acceptable.
 

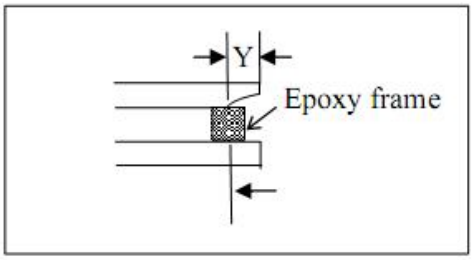
<table>
<tr><th>Point Size</th><th>Acceptable Qty</th></tr>
<tr><td>ϕ≤1/4W</td><td>Disregard</td></tr>
<tr><td>1/4W< ϕ≤1/2W</td><td>1</td></tr>
<tr><td>ϕ>1/2W</td><td>0</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>7</td><td>Back-light</td><td>(1) The color of backlight should correspond its specification.
(2) Not allow flickering</td></tr>
<tr><td>8</td><td>Soldering</td><td>(1) Not allow heavy dirty and solder ball on PCB.
(The size of dirty refer to point and dust defect)
(2) Over 50% of lead should be soldered on Land.
 
</td></tr>
<tr><td>9</td><td>Wire</td><td>(1) Copper wire should not be rusted
(2) Not allow crack on copper wire connection.
(3) Not allow reversing the position of the flat cable.
(4) Not allow exposed copper wire inside the flat cable.</td></tr>
<tr><td>10</td><td>PCB</td><td>(1) Not allow screw rust or damage.
(2) Not allow missing or wrong putting of component.</td></tr>
</table>

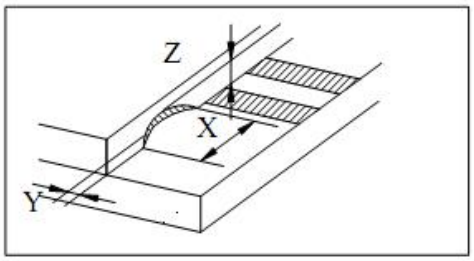
11	LCD	2.1.1 chip on the surface     <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>>1/8A</td><td>≤0.3mm</td><td>≤1/2T</td></tr><tr><td rowspan="2">≤1/8A</td><td>Not enter into epoxy frame</td><td>≤T</td></tr><tr><td>Not enter into the inner edge of epoxy</td><td>≤1/2T</td></tr></table>

11	LCD	2.1.2 chip on the terminal    X | Y | Z >1/8A | ≤0.3mm | ≤1/2T ≤1/8A | ≤1/2L | ≤T ≤1/8A 且≤1mm | ≤L | ≤T ≤1/8A 且≤2mm | ≤L | ≤1/2T Note: the distance between crack and contact pad must be greater than the width of 1st contact pad
		2.1.3chip out on between side 

11

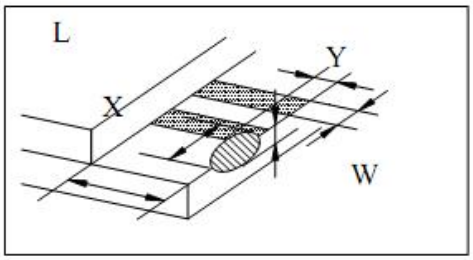
LCD



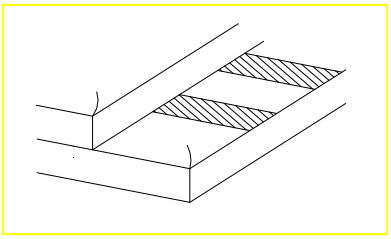
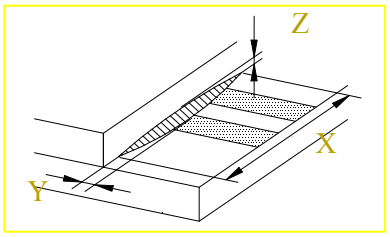


X	Y	Z
≤ 1/8A	Not enter into epoxy frame	Z≤2T
	Not enter into 1/2 epoxy frame	Z≤1/2T

2.1.4 including corner chip and side chip



X	Y	Z
>1/8A	≤1/6L	≤1/2T
≤1/8A	≤1/3L	
≤1/4W	≤2/3L	

<table>
<tr>
<td rowspan="2">11</td>
<td rowspan="2">LCD</td>
<td>2.2 Chip out
 
1) Chip out is that crackles extend to inner edge .
2) Crackles round epoxy frame will be rejected.
3) Chip out on the terminal will be rejected: Z=T length >1mm
or Z<T length >2mm
4) The chip out at ITO will be rejected.</td>
</tr>
<tr>
<td>2.3 Poor cutting
 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>>1/8A</td><td>≤0.3</td><td>≤1/2T</td></tr>
<tr><td>≤ 1/8A</td><td>According to drawing</td><td>1/2T≤Z≤T</td></tr>
</table>
Any one out of the specification will be rejected.</td>
</tr>
</table>

9.3. Reliability of LCM

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+70℃， 72hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30℃， 72hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage current)and the high thermal stress for a long time.	+70℃72hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage current)and the low thermal stress for a long time.	-20℃， 72hrs	1,2
High Temperature/ Humidity Operation	Endurance test applying the electric stress (voltage current)and the high thermal with high humidity stress for a long time.	+60℃， 90%RH,96hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage current)during a cycle of low and high thermal stress.	-20℃， 30min->25℃， 5min-> 70C,30min =1 cycle 10 cycles	

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25^{0} C, 0%RH.

Note 3: Test performed on product itself, not inside a container.

10.Guarantee

Our products could meet requirements of the environment.

RoHS is introduce European Union Directive 2011/65/EU， RoHS2.0 Requirements and Update.