





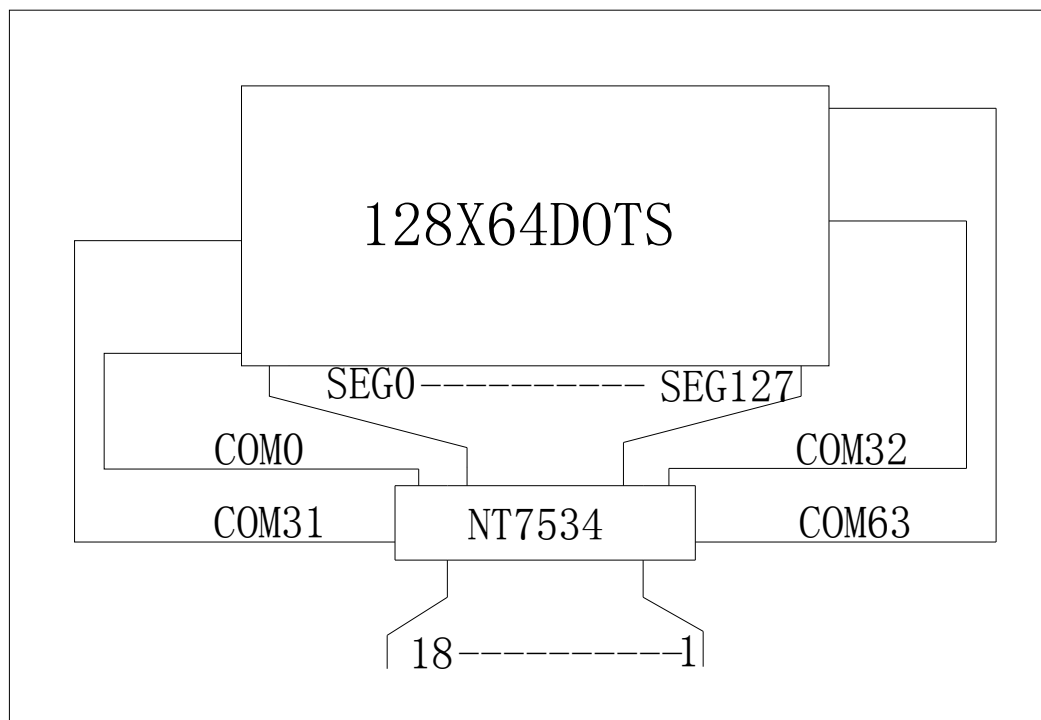
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## 1 FUNCTION & FEATURES

ITEM	Normal dimensions
Display Format	128*64 DOTS
Module dimension	76.10(W)*53.80 (H)*6.00(T_Max)MM
Viewing area	70.70(W)*38.80 (H) MM
Duty/bias	1/65DUTY,1/9BIAS
LCD mode	FFSTN/NEGATIVE/TRANSMISSVE
Viewing direction	6:00 O'clock

## 2 BLOCK DIAGRAM

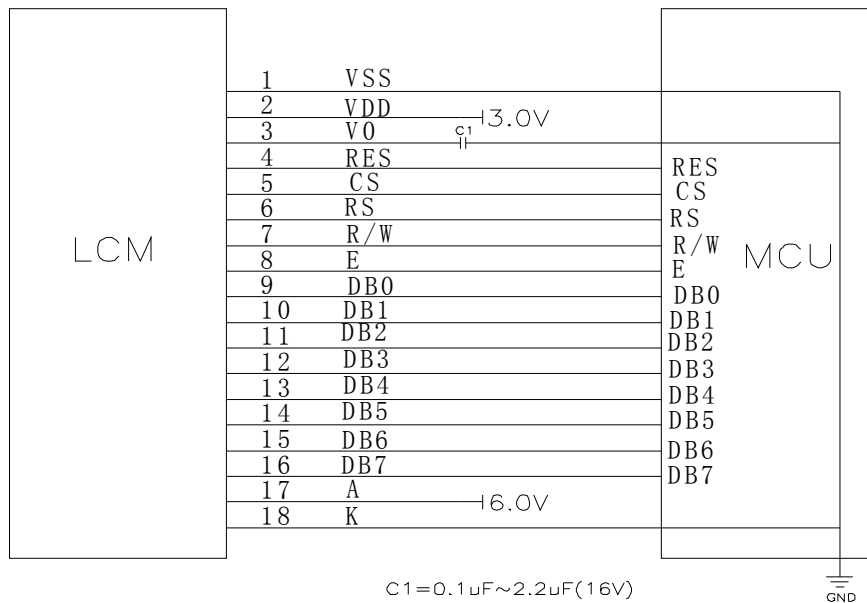


# 3 DIMENSIONAL CD DRAWING

Customer Approve By: \_\_\_\_\_

REV.	DESCRIPTION OF MODIFY	MODIFY BY:	DATE
A0	1. ST. DESIGN	DZQ	2011.09.08
A1	更改LCD为9.5寸	DZQ	2011.09.30
A2	更改PCB尺寸	DZQ	2011.10.11
A3	改善背光反射膜颜色	LHZ	2018-8-13
A4	改模式为FTN和BL电压及颜色	XWZ	2019-3-19

## 4 POWER SUPPLY



## 5 PIN DESCRIPTION

Pin no.	Symbol	Function
1	VSS	Ground. These pads must be connected to each other
2	VDD	Power supply input. These pads must be connected to each other
3	V0	V0 is the LCD driving voltage for common circuits at negative frame.
4	RST	When /RES is set to "L", the settings are initialized. The reset operation is performed by the /RES signal level
5	CS	This is the chip select signal. When /CS1= "L" and CS2= "H", then the chip select becomes active, and data/command I/O is enabled.
6	RS	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.
7	R/W	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/W = "H": Read When R/W = "L": Write
8	E	When connected to an 8080 MPU, it is active LOW. This pad is connected to the /RD signal of the 8080MPU, and the

		<p>NT7534 data bus is in an output status when this signal is “L” .</p> <p>When connected to a 6800 Series MPU, this is active HIGH.</p> <p>This is used as an enable clock input of the 6800 series MPU</p>
9-16	DB0-DB7	<p>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.</p> <p>When the serial interface is selected (P/S=“L”), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance.</p> <p>When the chip select is inactive, D0 to D7 are set to high impedance.</p>
17	A	BL Power supply
18	K	BL Ground.

## 6 MAXIMUM ABSOLUTE LIMIT (T=25 )

Item	Symbol	Standard value	Unit
supply voltage	V <sub>DD</sub>	-0.3~3.2	V
LCD driving voltage	V <sub>LCD</sub>	-0.3~9.5	V
Operating temperature	Topr	20~+70	°C
Storage temperature	Tstg	-30~+80	°C

## 7

### 7.1 DC Characteristics(T=25°C, VSS=0V)

Item	Symbol	Min	Type	Max	Unit	Test condition
Operating voltage	VDD	2.9	3.0	3.1	V	VDD-VSS
Input voltage	VIL	VSS	-	0.3VDD	V	-
	VIH	0.7VDD	-	VDD	V	
Output voltage	VOL	VSS	-	0.2VDD	V	-
	VOH	0.8VDD	-	VDD	V	-
LCD driving voltage	VLCD	9.3	9.5	9.7	V	V0 -VSS

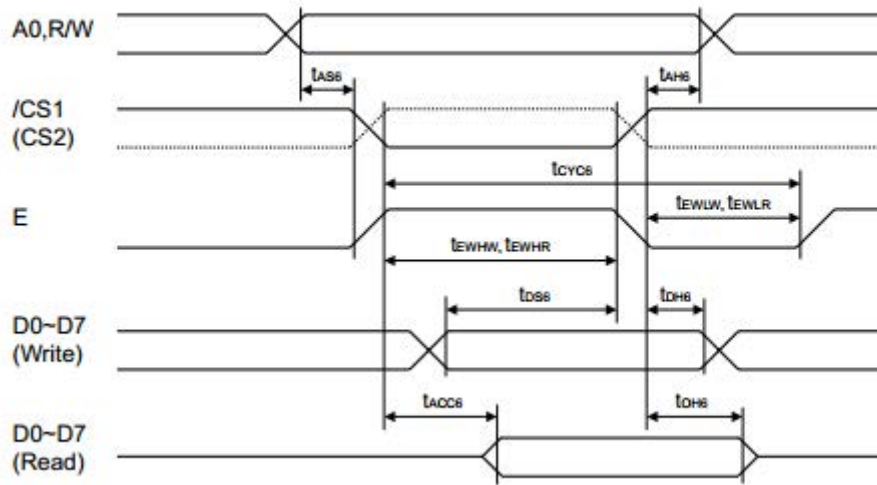
Note: VSS=0V.





### 7.3 AC Characteristics

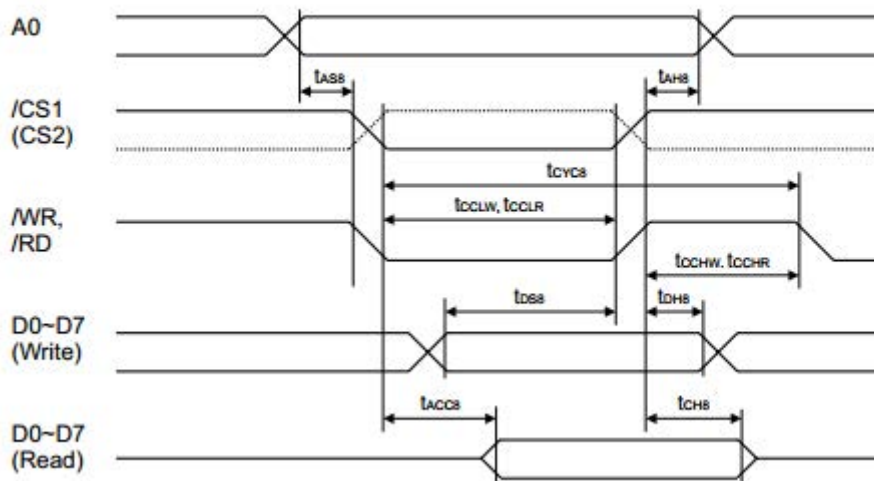
System Buses Read/Write Characteristics (for 6800 Series MPU)



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

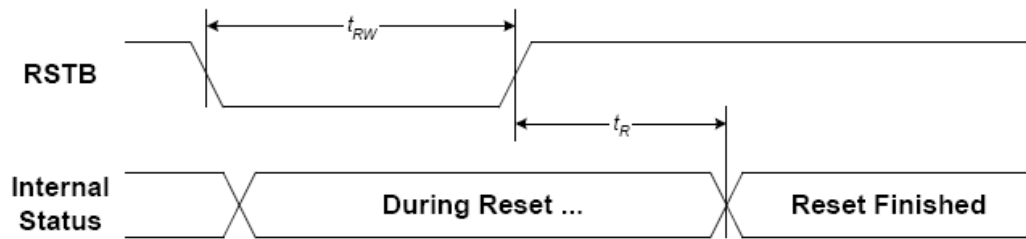
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$t_{ahs}$	Address hold time	0	-	-	ns	A0, R/W
$t_{ase}$	Address setup time	0	-	-	ns	
$t_{cyc}$	System cycle time	240	-	-	ns	
$t_{ewhw}$	Control high pulse width (write)	90	-	-	ns	E
$t_{ewhr}$	Control high pulse width (read)	120	-	-	ns	E
$t_{ewlw}$	Control low pulse width (write)	100	-	-	ns	E
$t_{ewlr}$	Control low pulse width (read)	60	-	-	ns	E
$t_{oss}$	Data setup time	40	-	-	ns	D0-D7
$t_{ohs}$	Data hold time	10	-	-	ns	
$t_{accs}$	/RD access time	-	-	140	ns	D0-D7 CL = 100pF
$t_{ohs}$	Output disable time	5	-	50	ns	

System Buses Read/Write Characteristics (for 8080 Series MPU)



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T <sub>AH8</sub>	Address hold time	0	-	-	ns	A0
T <sub>AS8</sub>	Address setup time	0	-	-	ns	
t <sub>CYC8</sub>	System cycle time	240	-	-	ns	
t <sub>CCLW</sub>	Control low pulse width (write)	90	-	-	ns	/WR
t <sub>CCLR</sub>	Control low pulse width (read)	120	-	-	ns	/RD
t <sub>CCHW</sub>	Control high pulse width (write)	100	-	-	ns	/WR
t <sub>CCHR</sub>	Control high pulse width (read)	60	-	-	ns	/RD
T <sub>DS8</sub>	Data setup time	40	-	-	ns	D0~D7
T <sub>DH8</sub>	Data hold time	10	-	-	ns	
t <sub>ACC8</sub>	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T <sub>CH8</sub>	Output disable time	5	-	50	ns	

**Hardware Reset Timing**


Item	Symbol	Condition	Min.	Max.	Unit
Reset time	t <sub>R</sub>		—	1.0	us
Reset "L" pulse width	t <sub>RW</sub>		1.0	—	

## 8 Instruction Description

Command	A0	/RD	/WR	Code								Hex	Function	
				D7	D6	D5	D4	D3	D2	D1	D0			
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0	1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h 7Fh	Specifies RAM display line for COM0	
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h B8h	Set the display data RAM page in Page Address register	
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address				00h 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register	
	0	1	0	0	0	0	0	Lower Column Address						
(5) Read Status	0	0	1	Status				0	0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM	
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM	
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0	1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0	1	A6h A7h	Normal indication when low, but full indication when high
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0	1	A4h A5h	Select normal display (0) or entire display on
(11) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0	1	A2h A3h	Sets LCD driving voltage bias ratio
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	0	E0h	Increments column address counter during each write
(13) End	0	1	0	1	1	1	0	1	1	1	0	0	EEh	Releases the Read-Modify-Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	0	E2h	Resets internal functions
(15) Common Output Mode Select	0	1	0	1	1	0	0	0	1	*	*	*	C0h CFh	Select COM output scan direction *: invalid data
(16) Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h 2Fh	Select the power circuit operation mode	
(17) V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h 27h	Select internal resistor ratio Rb/Ra mode	
(18) Electronic Volume mode Set Electronic Volume Register Set	0	1	0	1	0	0	0	0	0	0	1	0	81h	
	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register	
(19) Set Static Indicator ON/OFF Set Static Indicator Register	0	1	0	1	0	1	0	1	1	0	0	1	ACH ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
	0	1	0	*	*	*	*	*	*	Mode			XX	Sets the flash mode
(20) Power Save	0	1	0	-	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	0	E3h	Command for non-operation

Command	A0	/RD	/WR	Code								Hex	Function	
				D7	D6	D5	D4	D3	D2	D1	D0			
(22) Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0	1	E4h E5h	Select the oscillation frequency
(23) Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0	1	82h 83h	Enter/Release the partial display mode
(24) Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode	
(25) Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode	
(26) Partial Start Line Set Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	0	D3h	Enter Partial Start Line Set
	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line	
(27) N-Line Inversion Set Number of Line Set	0	1	0	1	0	0	0	0	1	0	1	0	85h	Enter N-Line inversion
	0	1	0	*	*	*	Number of Line						XX	Sets the number of line used for N-Line inversion
(28) N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	0	84h	Exit N-Line Inversion
(29) DC/DC Clock Set DC/DC Clock Division Set	0	1	0	1	1	1	0	0	1	1	0	0	E6h	Set DC/DC Clock Frequency
	0	1	0	1	1	0	0	Clock Division			XX	Set the Division of DC/DC Clock Frequency		
(30) Test Command	0	1	0	1	1	1	1	*	*	*	*	0	F1h FFh	IC test command. Do not use!
(31) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	0	F0h	Command of test mode reset

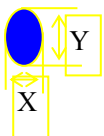
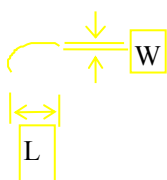
Note: Do not use any other command, or system malfunction may result.

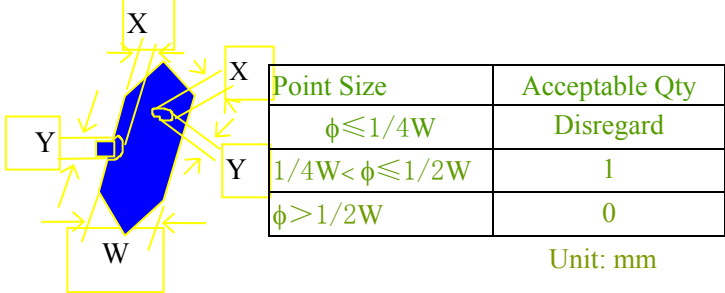
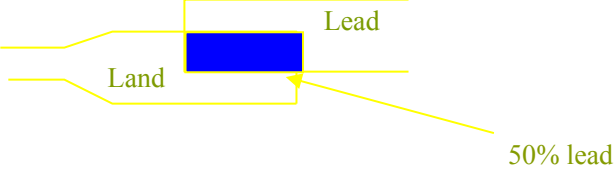
## **9 QUALITY SPECIFICATIONS**

### **9.1 Defect classification**

Classify	Item		Note	AQL
Major	Display state	Short or open circuit	1	0.65
		Contrast defect (dim, ghost)		
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction	2	
		Wrong Back-light	7	
	Non-display	Flat cable or pin reverse	9	
		Wrong or missing component	10	
	Minor	Display state	Background color deviation	
Black spot and dust			3	
Line defect			4	
Scratch				
Rainbow			5	
Pin hole			6	
Polarizer		Bubble and foreign material	3	
		Scratch	4	
PCB		Scratch	4	
Soldering		Poor connection	8	
Wire		Poor connection	9	

**9.2 Note on defect classification**

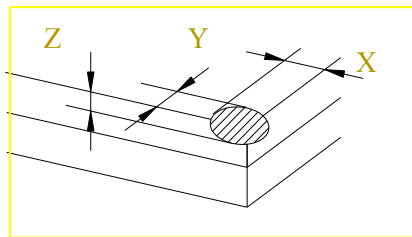
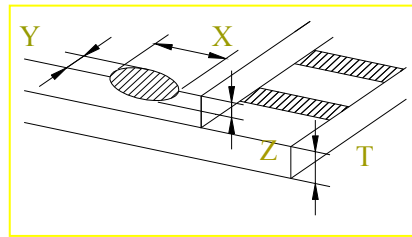
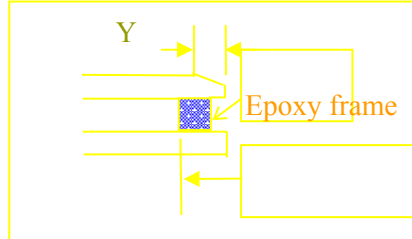
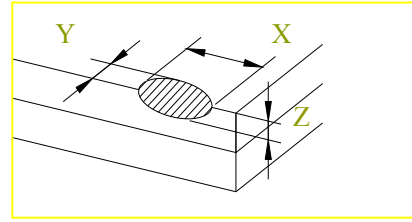
No.	Item	Criterion																			
1	Short or open circuit	Not allow																			
	LC leakage																				
	Flickering																				
	No display																				
	Wrong viewing direction																				
	Wrong Back-light																				
2	Contrast defect	Refer to approval sample																			
	Background color deviation																				
3	Point defect, Black spot, dust (incl. Polarizer)  $\phi = (X+Y)/2$	 <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Point Size</th> <th>Acceptable Qty.</th> </tr> </thead> <tbody> <tr> <td><math>\phi \leq 0.10</math></td> <td>Disregard</td> </tr> <tr> <td rowspan="2"><math>0.10 &lt; \phi \leq 0.15</math></td> <td>Positive: 3</td> </tr> <tr> <td>Negative: 2</td> </tr> <tr> <td rowspan="2"><math>0.15 &lt; \phi \leq 0.2</math></td> <td>Positive: 2</td> </tr> <tr> <td>Negative: 1</td> </tr> <tr> <td><math>\phi &gt; 0.2</math></td> <td>0</td> </tr> </tbody> </table> <p style="text-align: right;">Unit: mm</p>	Point Size	Acceptable Qty.	$\phi \leq 0.10$	Disregard	$0.10 < \phi \leq 0.15$	Positive: 3	Negative: 2	$0.15 < \phi \leq 0.2$	Positive: 2	Negative: 1	$\phi > 0.2$	0							
Point Size	Acceptable Qty.																				
$\phi \leq 0.10$	Disregard																				
$0.10 < \phi \leq 0.15$	Positive: 3																				
	Negative: 2																				
$0.15 < \phi \leq 0.2$	Positive: 2																				
	Negative: 1																				
$\phi > 0.2$	0																				
4	Line defect   <table border="1" style="margin-left: 20px;"> <thead> <tr> <th colspan="2">Line</th> <th>Acceptable Qty.</th> </tr> <tr> <th>L</th> <th>W</th> <th></th> </tr> </thead> <tbody> <tr> <td>---</td> <td><math>0.015 \geq W</math></td> <td>Disregard</td> </tr> <tr> <td><math>3.0 \geq L</math></td> <td><math>0.03 \geq W</math></td> <td rowspan="2">2</td> </tr> <tr> <td><math>2.0 \geq L</math></td> <td><math>0.05 \geq W</math></td> </tr> <tr> <td><math>1.0 \geq L</math></td> <td><math>0.1 &gt; W</math></td> <td>1</td> </tr> <tr> <td>---</td> <td><math>0.05 &lt; W</math></td> <td>Applied as point defect</td> </tr> </tbody> </table> <p style="text-align: right;">Unit: mm</p>	Line		Acceptable Qty.	L	W		---	$0.015 \geq W$	Disregard	$3.0 \geq L$	$0.03 \geq W$	2	$2.0 \geq L$	$0.05 \geq W$	$1.0 \geq L$	$0.1 > W$	1	---	$0.05 < W$	Applied as point defect
Line		Acceptable Qty.																			
L	W																				
---	$0.015 \geq W$	Disregard																			
$3.0 \geq L$	$0.03 \geq W$	2																			
$2.0 \geq L$	$0.05 \geq W$																				
$1.0 \geq L$	$0.1 > W$	1																			
---	$0.05 < W$	Applied as point defect																			
5	Rainbow	Not more than two color changes across the viewing area.																			

No.	Item	Criterion								
6	Segment pattern $W = \text{Segment width}$ $\phi = (X+Y)/2$	(1) Pin hole $\phi < 0.10\text{mm}$ is acceptable.  <table border="1" data-bbox="935 510 1394 680"> <thead> <tr> <th>Point Size</th> <th>Acceptable Qty</th> </tr> </thead> <tbody> <tr> <td><math>\phi \leq 1/4W</math></td> <td>Disregard</td> </tr> <tr> <td><math>1/4W &lt; \phi \leq 1/2W</math></td> <td>1</td> </tr> <tr> <td><math>\phi &gt; 1/2W</math></td> <td>0</td> </tr> </tbody> </table> <p style="text-align: right;">Unit: mm</p>	Point Size	Acceptable Qty	$\phi \leq 1/4W$	Disregard	$1/4W < \phi \leq 1/2W$	1	$\phi > 1/2W$	0
Point Size	Acceptable Qty									
$\phi \leq 1/4W$	Disregard									
$1/4W < \phi \leq 1/2W$	1									
$\phi > 1/2W$	0									
7	Back-light	(1) The color of backlight should correspond its specification. (2) Not allow flickering								
8	Soldering	(1) Not allow heavy dirty and solder ball on PCB. (The size of dirty refer to point and dust defect) (2) Over 50% of lead should be soldered on Land. 								
9	Wire	(1) Copper wire should not be rusted (2) Not allow crack on copper wire connection. (3) Not allow reversing the position of the flat cable. (4) Not allow exposed copper wire inside the flat cable.								
10	PCB	(1) Not allow screw rust or damage. (2) Not allow missing or wrong putting of component.								

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LCD

2.1.1 chip on the surface

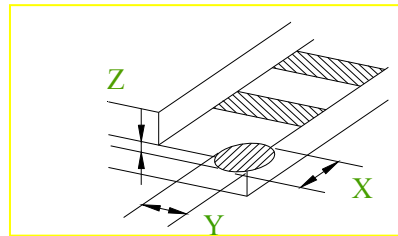
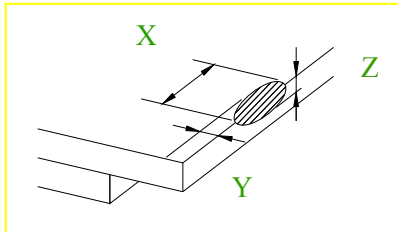
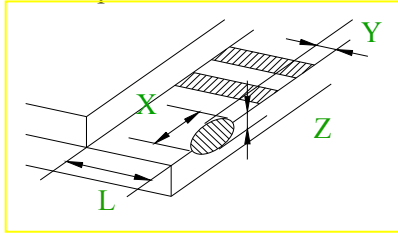


X	Y	Z
$>1/8A$	$\leq 0.3\text{mm}$	$\leq 1/2T$
$\leq 1/8A$	Not enter into epoxy frame	$\leq T$
	Not enter into the inner edge of epoxy	$\leq 1/2T$

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LCD

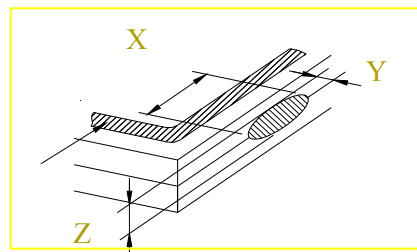
2.1.2 chip on the terminal



X	Y	Z
$> 1/8A$	$\leq 0.3\text{mm}$	$\leq 1/2T$
$\leq 1/8A$	$\leq 1/2L$	$\leq T$
$\leq 1/8A$ 且 $\leq 1\text{mm}$	$\leq L$	$\leq T$
$\leq 1/8A$ 且 $\leq 2\text{mm}$	$\leq L$	$\leq 1/2T$

Note: the distance between crack and contact pad must be greater than the width of 1<sup>st</sup> contact pad

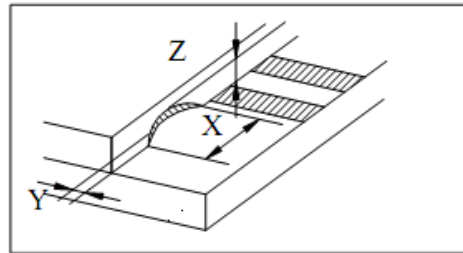
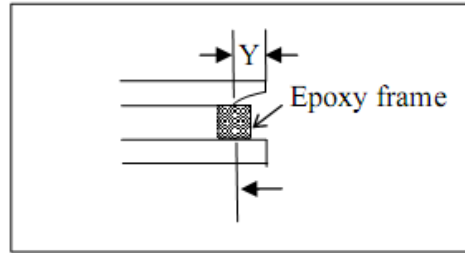
2.1.3 chip out on between side





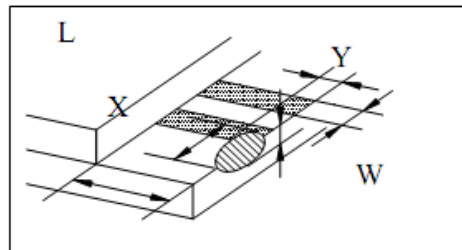
11

LCD

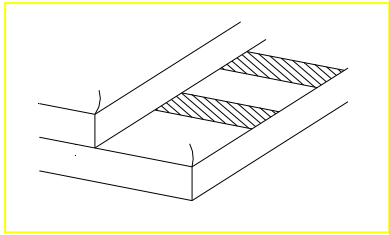
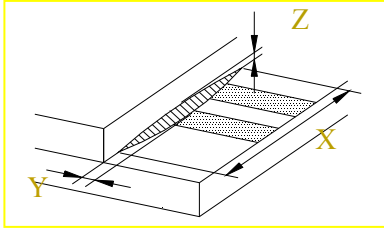


X	Y	Z
$\leq 1/8A$	Not enter into epoxy frame	$Z \leq 2T$
	Not enter into 1/2 epoxy frame	$Z \leq 1/2T$

2.1.4 including corner chip and side chip



X	Y	Z
$>1/8A$	$\leq 1/6L$	$\leq 1/2T$
$\leq 1/8A$	$\leq 1/3L$	
$\leq 1/4W$	$\leq 2/3L$	

<p>11</p>	<p>LCD</p>	<p>2.2 Chip out</p>  <ol style="list-style-type: none"> <li>1) Chip out is that crackles extend to inner edge .</li> <li>2) Crackles round epoxy frame will be rejected.</li> <li>3) Chip out on the terminal will be rejected: <math>Z=T</math> length <math>&gt;1\text{mm}</math> or <math>Z&lt;T</math> length <math>&gt;2\text{mm}</math></li> <li>4) The chip out at ITO will be rejected.</li> </ol>							
		<p>2.3 Poor cutting</p>  <table border="1" data-bbox="810 1227 1294 1422"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td><math>&gt;1/8A</math></td> <td><math>\leq 0.3</math></td> <td><math>\leq 1/2T</math></td> </tr> <tr> <td><math>\leq 1/8A</math></td> <td>According to drawing</td> <td><math>1/2T \leq Z \leq T</math></td> </tr> </tbody> </table> <p>Any one out of the specification will be rejected.</p>	X	Y	Z	$>1/8A$	$\leq 0.3$	$\leq 1/2T$	$\leq 1/8A$
X	Y	Z							
$>1/8A$	$\leq 0.3$	$\leq 1/2T$							
$\leq 1/8A$	According to drawing	$1/2T \leq Z \leq T$							

### 9.3. Reliability of LCM

Reliability test condition:

Item	Condition	Time (hrs)	Assessment
High temp. Storage	+80°C	72	No abnormalities in functions and appearance
High temp. Operating	+70°C	72	
Low temp. Storage	-30°C	72	
Low temp. Operating	-20°C	72	
Humidity	40°C/ 90%RH	72	
Temp. Cycle	-10°C ← 25°C → +60°C (1 hour ← 5 min → 1 hour)	10cycles	