

IB898

**Intel® Atom™ E3800 SoC Series
3.5" Disk Size SBC**

USER'S MANUAL

Version 1.0

Acknowledgments

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Introduction

Product Description

IB898 is a 3.5-inch single board computer based on the Intel® Atom™ E3800 series processors. It supports One DDR3L SODIMM sockets for a maximum memory capacity of 4GB.

IB898 features the Intel® Gen7 w/4EUs graphics engines and has both CRT and DisplayPort video display interface, and 24-bit LVDS dual channel interface with the use of the NXP PTN3460 device.

Onboard connections are available for two SATAII ports, two COM ports, one USB 3.0 ports, three USB2.0 ports, audio, three Mini PCI-e(x1) slots,

IB898 Features:

- Supports Atom™ E3800 series SoC processors
- One DDR3L SO-DIMM, 1066 MHz, Max. 4GB memory
- Integrated graphics for VGA, DP displays
- 2 x SATA II connectors
- 2x COM port connectors
- 1 x Mini-PCIe(x1) slot (*w/ USB/mSATA support*)
- 2 x Mini-PCIe(x1) slot
- 1x GbE (RJ-45) connectors
- 24-bit dual channel LVDS

Specifications

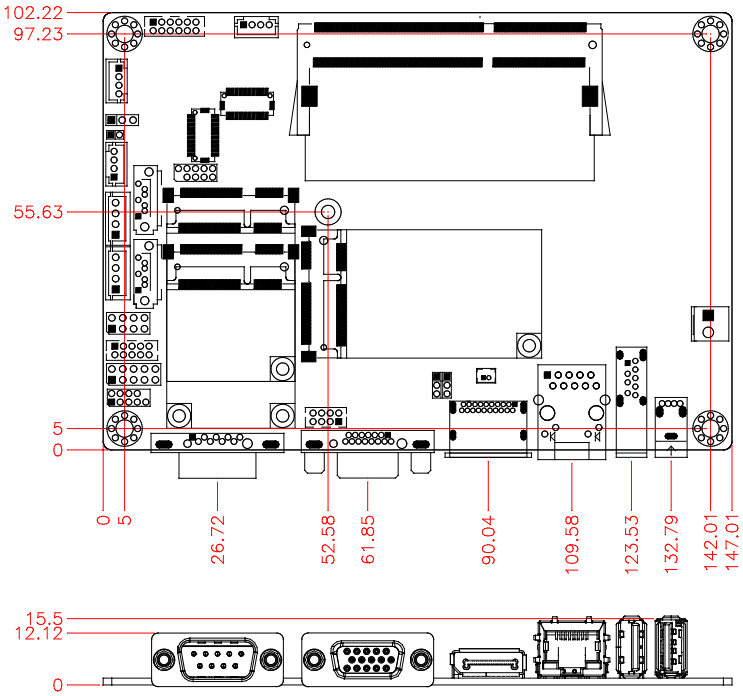
Product Name	IB898 [default silk screen model # on PCB is IB898]
Form Factor	3.5" disk size SBC
SoC Type/Speed	Intel® Atom™ DC E3825 /1MB cache/1.33 GHz (IB898-I25) Intel® Atom™ SC E3815 /512KB cache/1.46 GHz (IB898-I15) FCBGA1170, Type-3, 25mmx27mm, 22nm, Tj= -40° C to +110° C ; **All SoC Skus will be on D-0 stepping »
BIOS	AMI BIOS
Memory	Intel® Atom™ SoC integrated memory controller, supports DDR3L(1.35V) only; 1x DDR3 SO-DIMM socket; Max. DDR3L- 1066 @4GB (Non-ECC, Un-buffered)
VGA	Intel® Gen7 w/ 4 EUs graphics engines (Gfx freq @542MHz/792MHz [Turbo]); Supports DX 11, OGL 3.0, OCL 1.1, OGLES 2.0, DisplayPort x 1 [Support to 2560x1200@60Hz] CRT x 1 [Support to 1920x1080@60Hz]
LVDS	24-bit dual channel via NXP PTN3460 thru eDP [Supports up to 1920x1200@60Hz]
LAN	Intel I210IT PCIe Gigabit LAN [9x9mm @64-QFN , -40° C to +85° C]
USB	Intel® Atom™ SoC built-in USB host controller Support USB 2.0 x 4 ports; USB 3.0 x 1 port, USB 2.0 Hub x 4 ports (Thru Renesas uPD720115K8)
Serial ATA Ports	Intel® Atom™ SoC built-in SATA II controller, supports 2 ports
Audio	Intel® Atom™ SoC built-in HD Audio controller + Realtek ALC269QHD Codec w/ class-D speaker amplifier(2.3W per channel @ 5V P/S) [7mm x 7mm @ 48-QFN] ; support 2-channel audio out + amp
LPC I/O	<u>Nuvoton NCT5523D [64-pin LQFP, 7x7x1.4mm]</u> COM #1 (RS232/422/485) [EXAR SP339EER1 x 1 for jumper-less] COM #2 (RS-232 only) Hardware Monitor: 2x Thermal inputs; 2x Voltage monitoring
Digital IO	4 in & 4 out
Expansion Slots	Mini PCI-e socket x3 (2x Full-sized + 1x Half-sized , all with USB signal from USB Hub) **Full-sized MiniPCIe(1x) # 1 support mSATA also **
Edge Connector	DB9 for COM1, DB15 for VGA, DisplayPort, RJ45 for GbE LAN USB 2.0 vertical connector x 1 (from SoC) USB 3.0 vertical connector x 1 (from SoC)
Onboard Header/Connector	2x4 header for front panel (PWR, LED, RESET) DF11 2x4 header for 2x USB 2.0 (from USB Hub) DF20 socket connector x2 for 24-bit dual channel LVDS 4-pin box header for backlight/brightness control (PWM mode) DF11 2x6 box header x1 for Audio; 4-pin box header for speaker DF11 2x5 box header for COM2 2x5 pin header for LPC (80-port card debugging purpose) Mini PCI-e(1x) connector x3 SATA connector x2 for SATA device 4-pin power connector x2 (JST type, For SATA device) 2-pin connector 1 for power input
Watchdog Timer	Yes (256 segments, 0, 1, 2...255 sec/min)
Power Connector	12V only DC-in thru onboard 2-pin connector
Others	iSMART 3.1 [EuP/ErP ; Auto-scheduler ; Power resume] Heat-spreader / Heatsink for fanless purpose Mounting holes for heatsink / heat spreader are at least 5 holes
OS supporting	- Windows 8.1 / Embedded; Windows 7 / Embedded; Linux
RoHS 2.0 / CE /FCC/ LVD	Yes / Yes / Yes / Class B
Operating system	-40° C to +85° C
Board Size	102mm x 147mm

Checklist

Your IB898 package should include the items listed below.

- The IB898 SBC
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility

Board Dimensions



Installations

This section provides information on how to use the jumpers and connectors on the IB898 in order to set up a workable system. The topics covered are:

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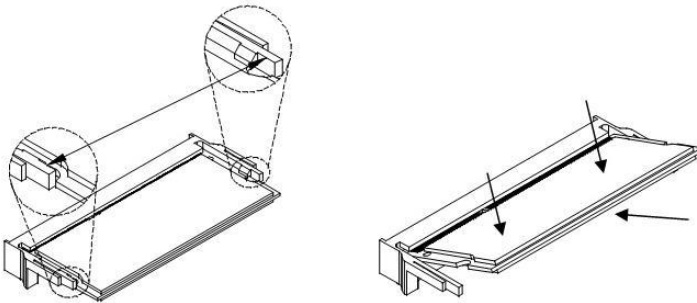
Installing the Memory

The IB898 board supports **one** DDR3L memory socket for a maximum total memory of 4GB in DDR3L memory type.

Installing and Removing Memory Modules

To install the DDR3L modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR3L module so that the key of the DDR3L module aligned with that on the memory slot.
2. Gently push the DDR3L module in an upright position until the clips of the slot close to hold the DDR3L module in place when the DDR3L module touches the bottom of the slot.
3. To remove the DDR3L module, press the clips with both hands.



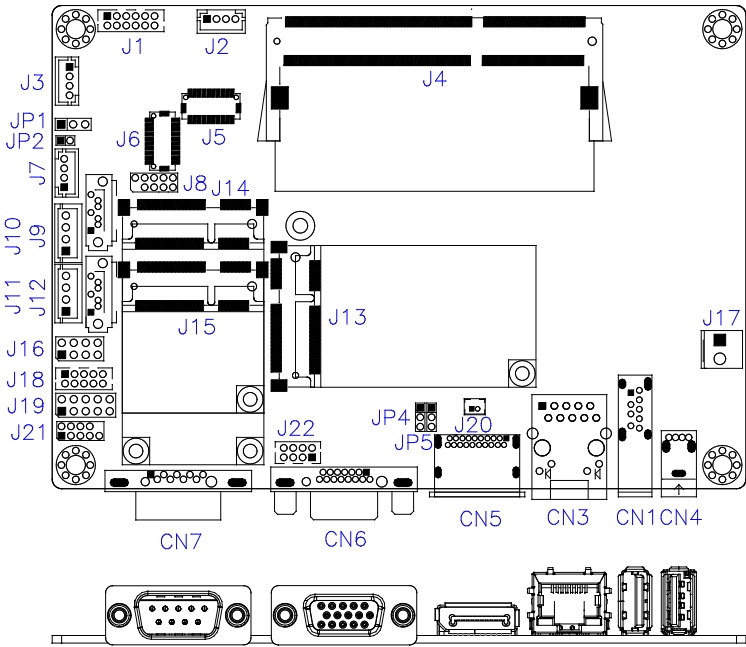
**** Channel-A slot must be installed with memory module for booting up****

Setting the Jumpers

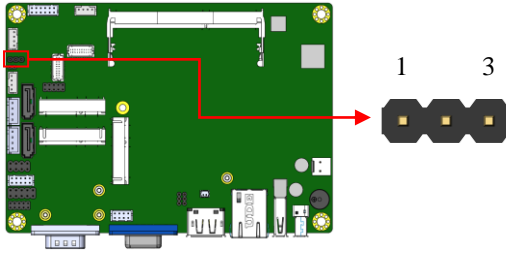
Jumpers are used on IB898 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on IB898 and their respective functions.

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JP4: Clear CMOS Contents	10
JP5: Clear ME Contents.....	10

Jumper Locations on IB898

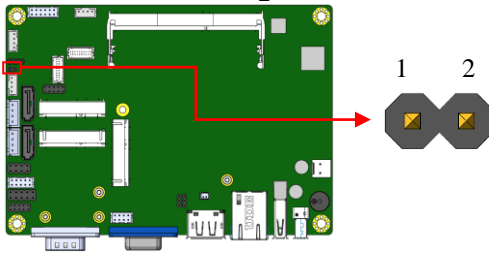


JP1: LVDS Panel Power Selection



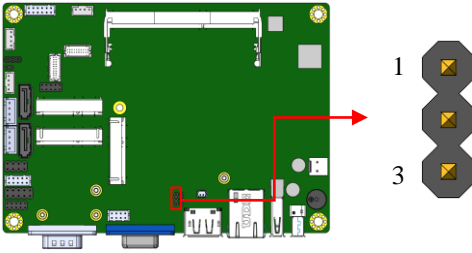
JP1	Setting	Panel Voltage
	Pin 1-2 Short/Closed	3.3V (default)
	Pin 2-3 Short/Closed	5V

JP2: LVDS Panel Brightness Control Selection



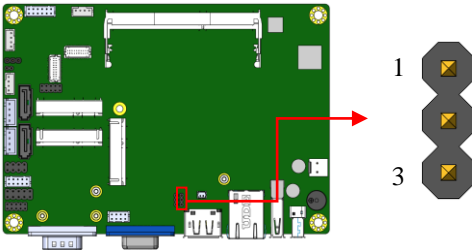
JP2	Brightness Control (PWM mode)
Open	3.3V
Close	5V(Default)

JP4: Clear CMOS Contents



JP4	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear CMOS

JP5: Clear ME Contents



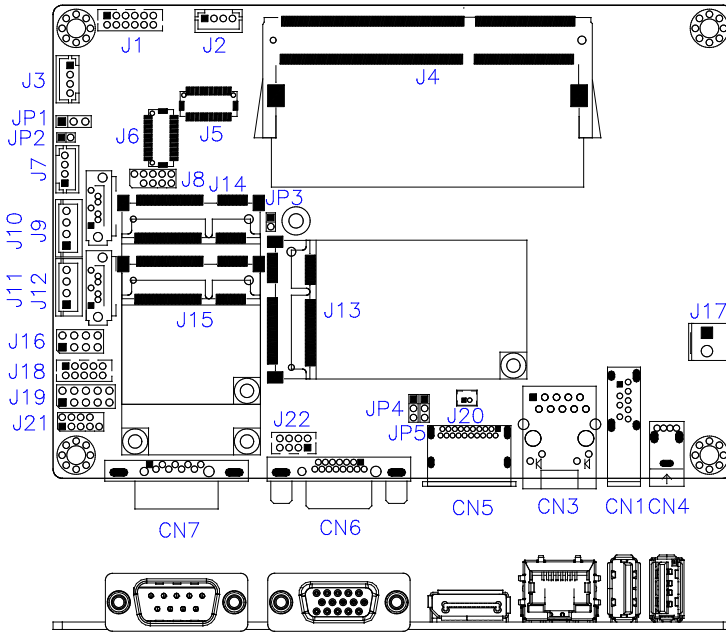
JP5	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear ME Register

Connectors on IB898

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INSTALLATIONS

Connector Locations on IB898



CN1: USB3.0 Connector

CN3: Gigabit LAN Connector

CN3: Intel® I210IT Connector

CN4: USB2.0 Connector

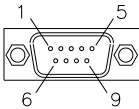
CN5: DP Connector

CN6: CRT Connector

CN7: DB9 Connector (COM1)

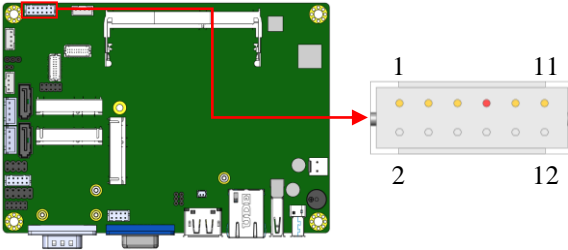
Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	6	DSR, Data set ready
RXD, Receive data	2	7	RTS, Request to send
TXD, Transmit data	3	8	CTS, Clear to send
DTR, Data terminal ready	4	9	RI, Ring indicator
GND, ground	5	10	Not Used

COM1 is jumper-less for RS-232, RS-422 and RS-485 and is to be configured with BIOS Selection.



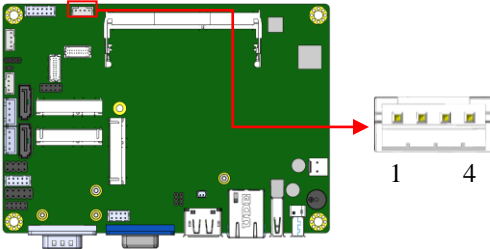
Pin #	Signal Name		
	RS-232	R2-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC
10	NC	NC	NC

J1: Audio Connector (DF11-12DP-2DSA)

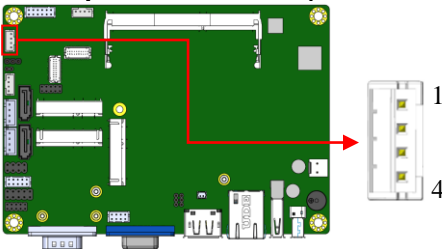


Signal Name	Pin #	Pin #	Signal Name
LINEOUT_R	2	1	LINEOUT_L
Ground	4	3	JD_FRONT
LINEIN_R	6	5	LINEIN_L
Ground	8	7	JD_LINEIN
MIC-R	10	9	MIC_L
Ground	12	11	JD_MIC1

J2: MCU Flash Connector (factory use only)

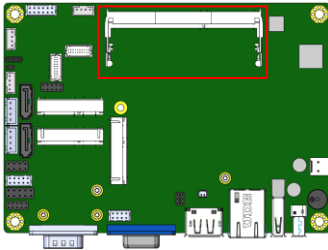


J3: Amplifier Connector (JST B4B-PH-K-S)



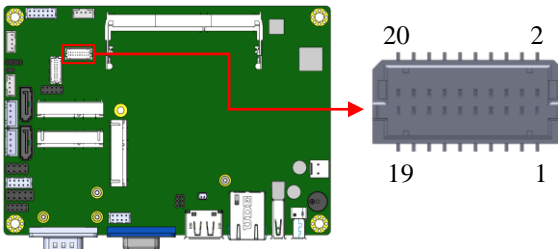
Pin #	Signal Name
1	OUTL+
2	OUTL-
3	OUTR-
4	OUTR+

J4: DDR3L SO-DIMM Sockets

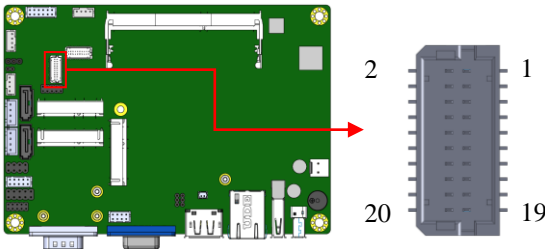


J5, J6: LVDS Connectors (DF20G-20DP-1V)

J5: First Channel LVDS



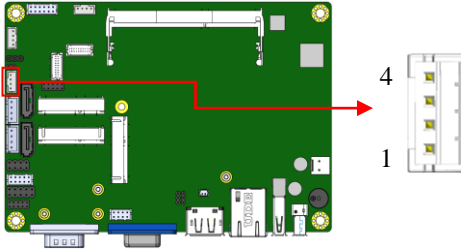
J6: Second Channel LVDS



Signal Name	Pin #	Pin #	Signal Name
TX0N	2	1	TX0P
Ground	4	3	Ground
TX1N	6	5	TX1P
Ground	8	7	Ground
TX2N	10	9	TX2P
Ground	12	11	Ground
CLKN	14	13	CLKP
Ground	16	15	Ground
TX3N	18	17	TX3P
Power(1A)	20	19	Power

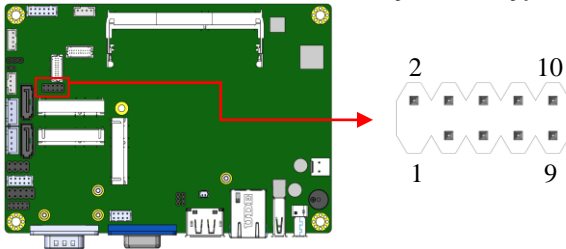
INSTALLATIONS

J7: LCD Backlight Connector (JST B4B-PH-K-S)

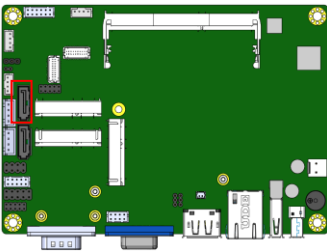


Pin #	Signal Name
1	+12V(1A)
2	Backlight Enable
3	Brightness Control
4	Ground

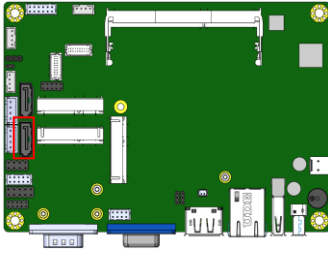
J8: SPI Flash Connector (factory use only)



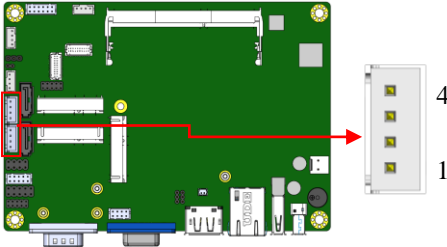
J9: SATAII /share mSATA/ Connectors



J12: SATAII Connectors



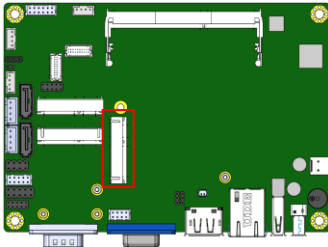
J10, J11: SATA HDD Power Connectors (JST B4B-XH-A)



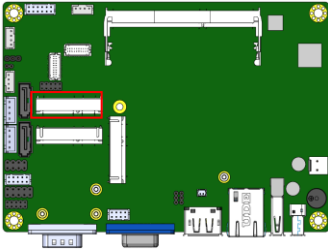
Pin #	Signal Name
1	+5V(1A)
2	Ground
3	Ground
4	+12V(1A)

**** It is recommend to connect with 2.5" storage device only from J10/J11****

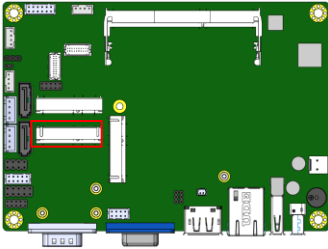
J13: Mini PCIE Connector (Full Size)



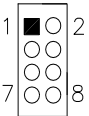
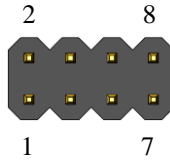
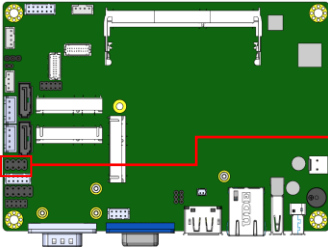
J14: Mini PCIE Connector (share mSATA)



J15: Mini PCIE Connector (Half Size)

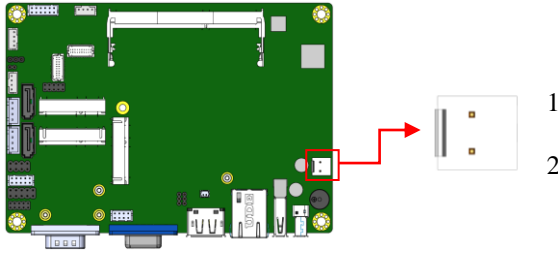


J16: Front Panel Function Connector (2.54mm)



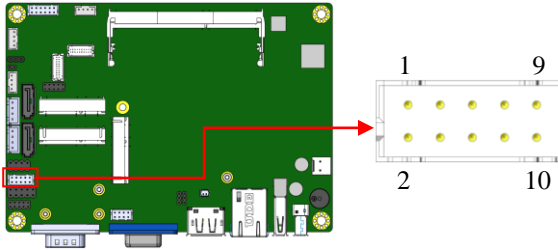
Signal Name	Pin #	Pin #	Signal Name
Power BTN	1	2	Power BTN
HDD LED+	3	4	HDD LED-
Reset BTN	5	6	Reset BTN
Power LED+	7	8	Power LED-

J17: Board Input Power Connector (HK_WAFER396-2S-WV)



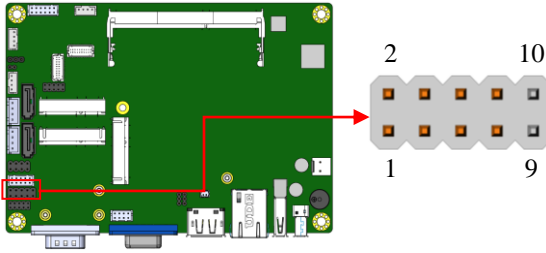
Pin #	Signal Name
1	VCC12
2	GND

J18: COM2/RS232 Serial Port (DF11-10DP-2DSA)



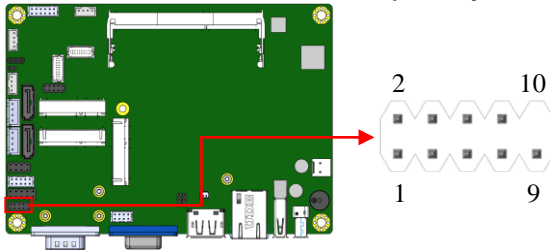
Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	2	RXD, Receive data
TXD, Transmit data	3	4	Data terminal ready
GND, ground	5	6	DSR, Data set ready
RTS, Request to send	7	8	CTS, Clear to send
RI, Ring indicator	9	10	Not Used

J19: Digital I/O Connector (2.54mm)

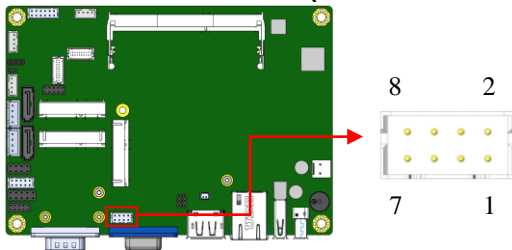


Signal Name	Pin #	Pin #	Signal Name
GND	1	2	VCC(500mA)
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J21: Debug 80 Port Connector (factory use only)



J22: USB 2.0 Connector (DF11-8DP-2DSA)



Signal Name	Pin #	Pin #	Signal Name
Vcc	1	2	Ground
D0-	3	4	D1+
D0+	5	6	D1-
Ground	7	8	Vcc

BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

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BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also provides password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the key immediately allows you to enter the Setup utility. If you are a little bit late pressing the key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

Press to Enter Setup

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

Main Settings

Aptio Setup Utility – Copyright © 2013 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
System Date			[Tue 04/20/2015]		Choose the system default language
System Time			[13:52:06]		→ ← Select Screen
					↑ ↓ Select Item
					Enter: Select
					+ - Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit
					ESC: Exit

System Date

Set the Date. Use Tab to switch between Data elements.

System Time

Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility – Copyright © 2013 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	Onboard LAN PXE Rom		[Disabled]		
	▶ ACPI Settings				→ ← Select Screen
	▶ LVDS Configuration				↑ ↓ Select Item
	▶ iSmart Controller				Enter: Select
	▶ Super IO Configuration				+ - Change Opt.
	▶ H/W Monitor				F1: General Help
	▶ CPU Configuration				F2: Previous Values
	▶ IDE Configuration				F3: Optimized Defaults
	▶ USB Configuration				F4: Save & Exit
					ESC: Exit

Onboard LAN PXE ROM

Controls the execution of UEFI and Legacy PXE OpROM.

ACPI Settings

Aptio Setup Utility – Copyright © 2013 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
	ACPI Settings				
	Enable ACPI Auto Configuration		Disabled		→ ← Select Screen
	Enable Hibernation		Enabled		↑ ↓ Select Item
	ACPI Sleep State		S3 (Suspend to RAM)		Enter: Select
					+ - Change Opt.
					F1: General Help
					F2: Previous Values
					F3: Optimized Defaults
					F4: Save & Exit
					ESC: Exit

Enabled ACPI Auto Configuration

Enables or Disables BIOS ACPI Auto Configuration.

Enable Hibernation

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State

Select ACPI sleep state the system will enter when the SUSPEND button is pressed.

LVDS Configuration

Aptio Setup Utility – Copyright © 2013 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
LVDS Configuration					→ ← Select Screen
LVDS Control			Enabled	↑ ↓ Select Item	
Panel Color Depth			24 BIT	Enter: Select	
LVDS Channel Type			Single	+- Change Opt.	
Panel Type			1024 x 768	F1: General Help	
Brightness Control			Enabled	F2: Previous Values	
Brightness Percent			100%	F3: Optimized Defaults	
PWM Clock			200Hz	F4: Save & Exit	
					ESC: Exit

iSMART Controller

Aptio Setup Utility – Copyright © 2013 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
iSMART Controller					→ ← Select Screen
Power-On after Power failure			Disable	↑ ↓ Select Item	
Temperature Guardian			Disable	Enter: Select	
Schedule Slot 1			None	+- Change Opt.	
Schedule Slot 2			None	F1: General Help	
					F2: Previous Values
					F3: Optimized Defaults
					F4: Save & Exit
					ESC: Exit

Power-On after Power failure

This field sets the system power status whether *Disable* or *Enable* when power returns to the system from a power failure situation.

Temperature Guardian

Generate the reset signal when system hangs up on POST.

Schedule Slot 1 / 2

Setup the hour/minute for system power on.

Super IO Configuration

Aptio Setup Utility - Copyright © 2013 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
Super IO Configuration					
EuP/ErP standby power control			Keep standby power	→ ← Select Screen	
▶ Serial Port 1 Configuration				↑ ↓ Select Item	
▶ Serial Port 2 Configuration				Enter: Select	
				+- Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	

EuP/ErP standby power control

EuP/ErP control on S5[Keep standby power] Enable all of the standby power and ignore EuP/ErP specification .[Ethernet Only]
 Only provide the standby power for Ethernet chip.[No standby power] Shutdown all of the standby power.

Serial Port 1 Configuration

Set parameters of serial port 1(COMA)

Serial Port 2 Configuration

Set parameters of serial port 2(COMB)

H/W Monitor

Aptio Setup Utility – Copyright © 2013 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
PC Health Status					→ ← Select Screen
	SYS temp		+33.0 C		↑ ↓ Select Item
	CPU temp		+40.5 C		Enter: Select
	Vcore		+0.776 V		+ - Change Opt.
	+1.35V		+1.352 V		F1: General Help
	USB3		+3.376 V		F2: Previous Values
	VCC3V		+3.312 V		F3: Optimized Defaults
	CPU Shutdown Temperature		Disabled		F4: Save & Exit
					ESC: Exit

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status

Shutdown Temperature

This field enables or disables the Shutdown Temperature

Disabled (default)

70 °C/158 F

75 °C/167 F

80 °C/176 F

85 °C/185 F

90 °C/194 F

95 °C/203 F

CPU Configuration

This section shows the CPU configuration parameters.

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Main	Advanced	Chipset	Boot	Security	Save & Exit
CPU Configuration					
▶ Socket 0 CPU Information					
CPU Speed		1334 MHz		→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
64-bit		Supported			

Socket 0 CPU Information

Socket specific CPU Information.

IDE Configuration
SATA Devices Configuration.

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Main	Advanced	Chipset	Boot	Security	Save & Exit
IDE Configuration					
Serial-ATA (SATA)		Enabled			
SATA Speed Support		Gen2			
SATA Mode		AHCI Mode			
Serial-ATA Port 0		Enabled			
SATA Port0 HotPlug		Disabled			
Serial-ATA Port 1		Enabled		→ ← Select Screen	
SATA Port1 HotPlug		Disabled		↑ ↓ Select Item	
SATA Port0		Not Present		Enter: Select	
SATA Port1		Not Present		+- Change Field	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Default	
				F4: Save ESC: Exit	

Serial-ATA(SATA)

Enabled / Disabled Serial ATA

SATA Speed Support

SATA Speed Support Gen1 or Gen2

SATA Mode

Select IDE / AHCI Mode

Serial –ATA Port 0

Enabled / Disabled Serial Port 0

SATA Port0 HotPlug

Enabled / Disabled SATA Port 0 HotPlug

Serial –ATA Port 1

Enabled / Disabled Serial Port 1

SATA Port1 HotPlug

Enabled / Disabled SATA Port 1 HotPlug

USB Configuration

Aptio Setup Utility - Copyright © 2013 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
USB Configuration					
USB Module Version		8.11.03			
USB Devices: 1Keyboard, 2 Hubs					
Legacy USB Support		Enabled		← → Select Screen	
XHCI Hand-off		Enabled		↑ ↓ Select Item	
EHCI Hand-off		Enabled		Enter: Select	
USB Mass Storage Driver Support		Enabled		+- Change Field	
USB hardware delays and time-outs:					
USB Transfer time-out		20 sec		F1: General Help	
Device reset time-out		20 sec		F2: Previous Values	
Device power-up delay		Auto		F3: Optimized Default	
F4: Save ESC: Exit					

Legacy USB Support

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

XHCI Hand-off

This is a workaround for OSeS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off

This is a workaround for OSeS without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB Mass Storage Driver Support

Enable/Disable USB Mass Storage Driver Support.

USB Transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

Device reset time-out

USB mass storage device start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

Chipset Settings

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Main	Advanced	Chipset	Boot	Security	Save & Exit
▶ North Bridge				→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	

North Bridge

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Main	Advanced	Chipset	Boot	Security	Save & Exit
Memory Information					→ ← Select Screen
Total Memory		4096 MB (LPDDR3)			↑ ↓ Select Item
Memory Slot0		4096 MB (LPDDR3)			Enter: Select
Memory Slot2		Not Present			+ - Change Opt.
					F1: General Help
					F2: Previous Values
					F3: Optimized Defaults
					F4: Save & Exit
					ESC: Exit

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

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Main	Advanced	Chipset	Boot	Security	Save & Exit
Password Description					
If ONLY the Administrator's password is set, then this only limit access to Setup and is only asked for when entering Setup.					
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights					
The password length must be in the following range:					
Minimum length			3		
Maximum length			20		
Administrator Password					
User Password					
					→ ← Select Screen
					↑ ↓ Select Item
					Enter: Select
					+ - Change Opt.
					F1: General Help
					F2: Previous Values
					F3: Optimized Defaults
					F4: Save & Exit
					ESC: Exit

Administrator Password

Set Administrator Password.

User Password

Set User Password.

Boot Settings

This section allows you to configure the boot settings.

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Main	Advanced	Chipset	Boot	Security	Save & Exit
Boot Configuration					
Setup Prompt Timeout			1		
Bootup NumLock State			On		
Quiet Boot			Disabled		
Fast Boot			Disabled		
Boot mode select			LEGACY		
FIXED BOOT ORDER Priorities					
Boot Option # 1			Hard Disk		
Boot Option # 2			CD/DVD		
Boot Option # 3			USB Hard Disk		
Boot Option # 4			USB CD/DVD		
Boot Option # 5			USB Key		
Boot Option # 6			USB Floppy		
Boot Option # 7			USB Lan		
Boot Option # 8			Network		

→ ← Select Screen
 ↑ ↓ Select Item
 Enter: Select
 +- Change Field
 F1: General Help
 F2: Previous Values
 F3: Optimized Default
 F4: Save & Exit
 ESC: Exit

Setup Prompt Timeout

Number of seconds to wait for setup activation key.
 65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables or disables Quiet Boot option.

Fast Boot

Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Boot mode select

Select boot mode LEGACY/UEFI.

Save & Exit Settings

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Main	Advanced	Chipset	Boot	Security	Save & Exit
Save Changes and Exit					
Discard Changes and Exit					
Save Changes and Reset					
Discard Changes and Reset					
Save Options					→ ← Select Screen
Save Changes					↑ ↓ Select Item
Discard Changes					Enter: Select
					+ - Change Opt.
Restore Defaults					F1: General Help
Save as User Defaults					F2: Previous Values
Restore User Defaults					F3: Optimized Defaults
					F4: Save & Exit
					ESC: Exit
Boot Override					

Save Changes and Exit

Exit system setup after saving the changes.

Discard Changes and Exit

Exit system setup without saving any changes.

Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset system setup without saving any changes.

Save Changes

Save Changes done so far to any of the setup options.

Discard Changes

Discard Changes done so far to any of the setup options.

Restore Defaults

Restore/Load Defaults values for all the setup options.

Save as User Defaults

Save the changes done so far as User Defaults.

Restore User Defaults

Restore the User Defaults to all the setup options.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

Intel Chipset Software Installation Utility	36
Intel Baytrail Graphics Driver Installation.....	37
Realtek High Definition Audio Driver Installation	38
LAN Drivers Installation	39
Intel Trusted Execution Engine Installation.....	40
Intel® USB 3.0 Drivers	41

IMPORTANT NOTE:

After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the DVD that comes with the board. Click **Intel** and then **Intel(R) Baytrail Chipset Drivers**. Click **Intel(R) Chipset Software Installation Utility**.



2. When the Welcome screen to the Intel Chipset Device Software appears, click **Next** to continue.
3. Click **Yes** to accept the software license agreement and proceed with the installation process. Click **Next** to continue.
4. The Setup process is now complete. Click **Finish** to restart the computer and for changes to take effect.

Intel Baytrail Graphics Driver Installation

1. Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) Baytrail Chipset Drivers*. Click *Intel(R) Baytrail Graphics Driver*.



2. When the Welcome screen appears, click *Next* to continue.
3. Click *Yes* to accept the license agreement and continue the installation. Click *Next* to continue.
4. Setup complete. Click *Finish* to restart the computer and for changes to take effect.

Realtek High Definition Audio Driver Installation

Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) Baytrail Chipset Drivers*. Click *Realtek High Definition Audio Driver*.



2. On the Welcome screen, click *Next* to proceed with the installation.
3. InstallShield Wizard is complete. Click *Finish* to restart the computer and for changes to take effect.

LAN Drivers Installation

1. Insert the DVD that comes with the board. Click *LAN Card* and then click *Intel LAN Controller Drivers*. Click *Intel(R) I21x Gigabit Network Drivers*.



2. When the Welcome screen appears, click *Next* to continue.
3. Click *Next* to agree with the license agreement.
4. When the Setup Options screen appears, click *Next* to continue.
5. The wizard is ready to begin installation. Click *Install* to begin the installation.
6. When InstallShield Wizard is complete, click *Finish*.

Intel Trusted Execution Engine Installation

Note :Windows 7 OS only

Important Notes

- 4) Intel TXE PV Firmware is signed by Intel
- PV POR configuration is signed Intel TXE FW and Production Silicon
 - Signed Intel TXE FW and Pre Production Silicon is supported for development needs only

Combination of unsigned Intel TXE Firmware and Production Silicon is not supported and will result in unexpected behavior

- 5) For Windows 7 OS only:
Intel® Trusted Execution Engine Interface (Intel® TXEI) Driver uses KMDF (WDF) 1.1.1, which is built-in on Windows 8 and Windows 8.1. However, Windows 7 doesn't have it. Please install Kernel-Mode Driver Framework (KMDF) version 1.1. Otherwise, yellow bang appears on Intel TXEI device upon installation. Please follow instructions in this [link: KB2685811](#)

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All products, computer systems, dates and figures specifications are preliminary based on current expectations, and are subject to change without notice.

Intel Confidential



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1. Insert the DVD that comes with the board. Click *Intel* and then *Intel(R) Baytrail Chipset Drivers*. Click *Intel(R) TXE Drivers*.



2. On the Setup Welcome screen, click *Next* to proceed with the installation process.

3. Click *Next* accept the license agreement and continue the installation, click *Next* to continue.

4. Installation of the Intel Trusted Execution Engine is now complete. Click *Finish* to restart the computer and for changes to take effect.

Intel® USB 3.0 Drivers

1. Insert the DVD that comes with the board. Click **Intel** and then **Intel(R) Baytrail Chipset Drivers**. Click **Intel(R) USB 3.0 Drivers**.



2. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click **Next**.

3. Click **Yes** to agree with the license agreement and continue the installation.

4. On the Readme File Information screen, click **Next** to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

5. When the Setup Progress screen appears, click **Next**. Setup complete. Click **Finish** to restart the computer and for changes to take effect.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0000h-006Fh	PCI bus
0020h-0021h	Programmable interrupt controller
0024h-0025h	Programmable interrupt controller
0028h-0029h	Programmable interrupt controller
002Ch-002Dh	Programmable interrupt controller
0030h-0031h	Programmable interrupt controller
0034h-0035h	Programmable interrupt controller
0038h-0039h	Programmable interrupt controller
003Ch-003Dh	Programmable interrupt controller
0040h-0043h	System timer
0050h-0053h	System timer
0070h-0077h	System CMOS/real time clock
0078h-0CF7h	PCI bus
00A0h-00A1h	Programmable interrupt controller
00A4h-00A5h	Programmable interrupt controller
00A8h-00A9h	Programmable interrupt controller
00ACh-00ADh	Programmable interrupt controller
00B0h-00B1h	Programmable interrupt controller
00B4h-00B5h	Programmable interrupt controller
00B8h-00B9h	Programmable interrupt controller
00BCh-00BDh	Programmable interrupt controller
03B0h-03BBh	Intel(R) Atom(TM) Processor E3800 Series/Intel(R) Celeron(R) Processor N2920/J1900
03C0h-03DFh	Intel(R) Atom(TM) Processor E3800 Series/Intel(R) Celeron(R) Processor N2920/J1900
03E8h-03EFh	Nuvoton Communications Port (COM2)
03F8h-03FFh	Nuvoton Communications Port (COM1)
04D0h-04D1h	Programmable interrupt controller
0D00h-FFFFh	PCI bus

APPENDIX

Address	Device Description
D000h-DFFFh	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series PCI Express - Root Port 1 - 0F48
E000h-E01Fh	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series Platform Control Unit - SMBus Port - 0F12
E020h-E03Fh	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series AHCI - 0F23
E040h-E043h	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series AHCI - 0F23
E050h-E057h	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series AHCI - 0F23
E060h-E063h	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series AHCI - 0F23
E070h-E077h	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series AHCI - 0F23
E080h-E087h	Intel(R) Atom(TM) Processor E3800 Series/Intel(R) Celeron(R) Processor N2920/J1900

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System timer
IRQ 3	Nuvoton Communications Port (COM2)
IRQ 4	Nuvoton Communications Port (COM1)
IRQ 8	High precision event timer
IRQ 11	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series Platform Control Unit - SMBus Port - 0F12
IRQ 16	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series PCI Express - Root Port 1 - 0F48
IRQ 17	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series PCI Express - Root Port 2 - 0F4A
IRQ 18	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series PCI Express - Root Port 3 - 0F4C
IRQ 19	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series PCI Express - Root Port 4 - 0F4E
IRQ 19	Intel(R) Pentium(R) processor N- and J-series / Intel(R) Celeron(R) processor N- and J-series AHCI - 0F23
IRQ 22	High Definition Audio Controller

C. Digital I/O Sample Code

File of the NCT5523D.H

```
//-----  
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY  
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE  
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR  
// PURPOSE.  
//-----  
#ifndef __NCT5523D_H  
#define __NCT5523D_H          1  
//-----  
#define NCT5523D_INDEX_PORT (NCT5523D_BASE)  
#define NCT5523D_DATA_PORT (NCT5523D_BASE+1)  
//-----  
#define NCT5523D_REG_LD      0x07  
//-----  
#define NCT5523D_UNLOCK     0x87  
#define NCT5523D_LOCK       0xAA  
//-----  
unsigned int Init_NCT5523D(void);  
void Set_NCT5523D_LD( unsigned char);  
void Set_NCT5523D_Reg( unsigned char, unsigned char);  
unsigned char Get_NCT5523D_Reg( unsigned char);  
//-----  
#endif// __NCT5523D_H
```

APPENDIX

File of the MAIN.CPP

```
//-----  
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY  
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE  
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR  
// PURPOSE.  
//-----  
#include <dos.h>  
#include <conio.h>  
#include <stdio.h>  
#include <stdlib.h>  
#include "NCT5523D.H"  
//-----  
int main (void);  
  
void Dio5Initial(void);  
void Dio5SetOutput(unsigned char);  
unsigned char Dio5GetInput(void);  
void Dio5SetDirection(unsigned char);  
unsigned char Dio5GetDirection(void);  
//-----  
int main (void)  
{  
    char SIO;  
  
    SIO = Init_NCT5523D();  
    if (SIO == 0)  
    {  
        printf("Can not detect Nuvoton NCT5523D, program abort.\n");  
        return(1);  
    }  
  
    Dio5Initial();  
  
    //for GPIO20..27  
    Dio5SetDirection(0x0F); //GP20..23 = input, GP24..27=output  
    printf("Current DIO direction = 0x%X\n", Dio5GetDirection());  
  
    printf("Current DIO status = 0x%X\n", Dio5GetInput());  
  
    printf("Set DIO output to high\n");  
    Dio5SetOutput(0x0F);  
  
    printf("Set DIO output to low\n");  
    Dio5SetOutput(0x00);  
  
    return 0;  
}  
//-----
```

APPENDIX

```
void Dio5Initial(void)
{
    unsigned char ucBuf;

    ucBuf = Get_NCT5523D_Reg(0x1C);
    ucBuf &= ~0x02;
    Set_NCT5523D_Reg(0x1C, ucBuf);

    Set_NCT5523D_LD(0x07); //switch to logic device 7
    //enable the GP2 group
    ucBuf = Get_NCT5523D_Reg(0x30);
    ucBuf |= 0x04;
    Set_NCT5523D_Reg(0x30, ucBuf);
}
//-----
void Dio5SetOutput(unsigned char NewData)
{
    Set_NCT5523D_LD(0x07); //switch to logic device 7
    Set_NCT5523D_Reg(0xE1, NewData);
}
//-----
unsigned char Dio5GetInput(void)
{
    unsigned char result;

    Set_NCT5523D_LD(0x07); //switch to logic device 7
    result = Get_NCT5523D_Reg(0xE1);
    return (result);
}
//-----
void Dio5SetDirection(unsigned char NewData)
{
    //NewData : 1 for input, 0 for output
    Set_NCT5523D_LD(0x07); //switch to logic device 7
    Set_NCT5523D_Reg(0xE8, NewData);
}
//-----
unsigned char Dio5GetDirection(void)
{
    unsigned char result;

    Set_NCT5523D_LD(0x07); //switch to logic device 7
    result = Get_NCT5523D_Reg(0xE8);
    return (result);
}
//-----
```

APPENDIX

File of the NCT5523D.CPP

```
//-----  
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY  
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE  
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR  
// PURPOSE.  
//-----  
#include "NCT5523D.H"  
#include <dos.h>  
//-----  
unsigned int NCT5523D_BASE;  
void Unlock_NCT5523D (void);  
void Lock_NCT5523D (void);  
//-----  
unsigned int Init_NCT5523D(void)  
{  
    unsigned int result;  
    unsigned char ucDid;  
  
    NCT5523D_BASE = 0x4E;  
    result = NCT5523D_BASE;  
  
    ucDid = Get_NCT5523D_Reg(0x20);  
    if (ucDid == 0xC4) //NCT5523D??  
    { goto Init_Finish; }  
  
    NCT5523D_BASE = 0x2E;  
    result = NCT5523D_BASE;  
  
    ucDid = Get_NCT5523D_Reg(0x20);  
    if (ucDid == 0xC4) //NCT5523D??  
    { goto Init_Finish; }  
  
    NCT5523D_BASE = 0x00;  
    result = NCT5523D_BASE;  
  
Init_Finish:  
    return (result);  
}  
//-----  
void Unlock_NCT5523D (void)  
{  
    outportb(NCT5523D_INDEX_PORT, NCT5523D_UNLOCK);  
    outportb(NCT5523D_INDEX_PORT, NCT5523D_UNLOCK);  
}  
//-----  
void Lock_NCT5523D (void)  
{  
    outportb(NCT5523D_INDEX_PORT, NCT5523D_LOCK);  
}  
//-----
```

APPENDIX

```
void Set_NCT5523D_LD( unsigned char LD)
{
    Unlock_NCT5523D();
    outportb(NCT5523D_INDEX_PORT, NCT5523D_REG_LD);
    outportb(NCT5523D_DATA_PORT, LD);
    Lock_NCT5523D();
}
//-----
void Set_NCT5523D_Reg( unsigned char REG, unsigned char DATA)
{
    Unlock_NCT5523D();
    outportb(NCT5523D_INDEX_PORT, REG);
    outportb(NCT5523D_DATA_PORT, DATA);
    Lock_NCT5523D();
}
//-----
unsigned char Get_NCT5523D_Reg(unsigned char REG)
{
    unsigned char Result;
    Unlock_NCT5523D();
    outportb(NCT5523D_INDEX_PORT, REG);
    Result = inportb(NCT5523D_DATA_PORT);
    Lock_NCT5523D();
    return Result;
}
//-----
```

D. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
File of the NCT5523D.H
//-----
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----
#ifndef __NCT5523D_H
#define __NCT5523D_H          1
//-----
#define NCT5523D_INDEX_PORT (NCT5523D_BASE)
#define NCT5523D_DATA_PORT (NCT5523D_BASE+1)
//-----
#define NCT5523D_REG_LD      0x07
//-----
#define NCT5523D_UNLOCK      0x87
#define NCT5523D_LOCK        0xAA
//-----
unsigned int Init_NCT5523D(void);
void Set_NCT5523D_LD( unsigned char);
void Set_NCT5523D_Reg( unsigned char, unsigned char);
unsigned char Get_NCT5523D_Reg( unsigned char);
//-----
#endif// __NCT5523D_H
```

File of the MAIN.CPP.

```
//-----  
//  
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY  
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE  
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR  
// PURPOSE.  
//  
//-----  
#include <dos.h>  
#include <conio.h>  
#include <stdio.h>  
#include <stdlib.h>  
#include "NCT5523D.H"  
//-----  
int main (void);  
  
void WDTInitial(void);  
void WDTEnable(unsigned char);  
void WDTDisable(void);  
  
//-----  
int main (void)  
{  
    char SIO;  
  
    SIO = Init_NCT5523D();  
    if (SIO == 0)  
    {  
        printf("Can not detect Nuvoton NCT5523D, program abort.\n");  
        return(1);  
    }  
  
    WDTInitial();  
  
    WDTEnable(10);  
  
    WDTDisable();  
  
    return 0;  
}  
//-----  
void WDTInitial(void)  
{  
    unsigned char bBuf;  
    Set_NCT5523D_LD(0x08);  
    bBuf = Get_NCT5523D_Reg(0x30); //switch to logic device 8  
    bBuf &= (~0x01);  
    Set_NCT5523D_Reg(0x30, bBuf); //Enable WDTO  
}  
//-----
```

APPENDIX

```
void WDTEnable(unsigned char NewInterval)
{
    unsigned char bBuf;

    Set_NCT5523D_LD(0x08);                //switch to logic device 8
    Set_NCT5523D_Reg(0x30, 0x01);        //enable timer

    bBuf = Get_NCT5523D_Reg(0xF0);
    bBuf &= (~0x08);
    Set_NCT5523D_Reg(0xF0, bBuf);        //count mode is second

    Set_NCT5523D_Reg(0xF1, NewInterval); //set timer
}
//-----
void WDTDisable(void)
{
    Set_NCT5523D_LD(0x08);                //switch to logic device 8
    Set_NCT5523D_Reg(0xF1, 0x00);        //clear watchdog timer
    Set_NCT5523D_Reg(0x30, 0x00);        //watchdog disabled
}
//-----
```


APPENDIX

File of the NCT5523D.CPP

```
//-----  
//  
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY  
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE  
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR  
// PURPOSE.  
//  
//-----  
#include "NCT5523D.H"  
#include <dos.h>  
//-----  
unsigned int NCT5523D_BASE;  
void Unlock_NCT5523D (void);  
void Lock_NCT5523D (void);  
//-----  
unsigned int Init_NCT5523D(void)  
{  
    unsigned int result;  
    unsigned char ucDid;  
  
    NCT5523D_BASE = 0x4E;  
    result = NCT5523D_BASE;  
  
    ucDid = Get_NCT5523D_Reg(0x20);  
    if (ucDid == 0xC4) //NCT5523D??  
    { goto Init_Finish; }  
  
    NCT5523D_BASE = 0x2E;  
    result = NCT5523D_BASE;  
  
    ucDid = Get_NCT5523D_Reg(0x20);  
    if (ucDid == 0xC4) //NCT5523D??  
    { goto Init_Finish; }  
  
    NCT5523D_BASE = 0x00;  
    result = NCT5523D_BASE;  
  
Init_Finish:  
    return (result);  
}  
//-----  
void Unlock_NCT5523D (void)  
{  
    outportb(NCT5523D_INDEX_PORT, NCT5523D_UNLOCK);  
    outportb(NCT5523D_INDEX_PORT, NCT5523D_UNLOCK);  
}  
//-----  
void Lock_NCT5523D (void)  
{  
    outportb(NCT5523D_INDEX_PORT, NCT5523D_LOCK);  
}  
//-----
```

```
void Set_NCT5523D_LD( unsigned char LD)
{
    Unlock_NCT5523D();
    outportb(NCT5523D_INDEX_PORT, NCT5523D_REG_LD);
    outportb(NCT5523D_DATA_PORT, LD);
    Lock_NCT5523D();
}
//-----
void Set_NCT5523D_Reg( unsigned char REG, unsigned char DATA)
{
    Unlock_NCT5523D();
    outportb(NCT5523D_INDEX_PORT, REG);
    outportb(NCT5523D_DATA_PORT, DATA);
    Lock_NCT5523D();
}
//-----
unsigned char Get_NCT5523D_Reg(unsigned char REG)
{
    unsigned char Result;
    Unlock_NCT5523D();
    outportb(NCT5523D_INDEX_PORT, REG);
    Result = inportb(NCT5523D_DATA_PORT);
    Lock_NCT5523D();
    return Result;
}
//-----
```