

SPECIFICATIONS

MODEL NO.	S90401R-DT028QV
TYPE	LCD MODULE, 240(RGB) *320 PIXELS

Preliminary Specification

Final Specification

SUCCESS			CUSTOMER
PREPARED	CHECKED	APPROVED	APPROVED
XUETIANTIAN	LEIHUI	HUJINBO	

深圳市宇顺电子股份有限公司

SUCCESS ELECTRONICS LTD

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1. GENERAL SPECIFICATION

1.1 Description

The S90401R-DT028QV is a color active matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD) that uses amorphous silicon(a-Si) TFT as a switching device. This model is composed of a single 2.8 inches transmissive type main TFT-LCD panel. The resolution of the panel is 240 x 320 pixels and can display up to 262K color.

1.2 Feature

- TM type for main TFT-LCD panel
- Structure COG+FPC+BL
- Full, Normal (Still), Partial, Sleep, Standby mode are available

1.3 Application

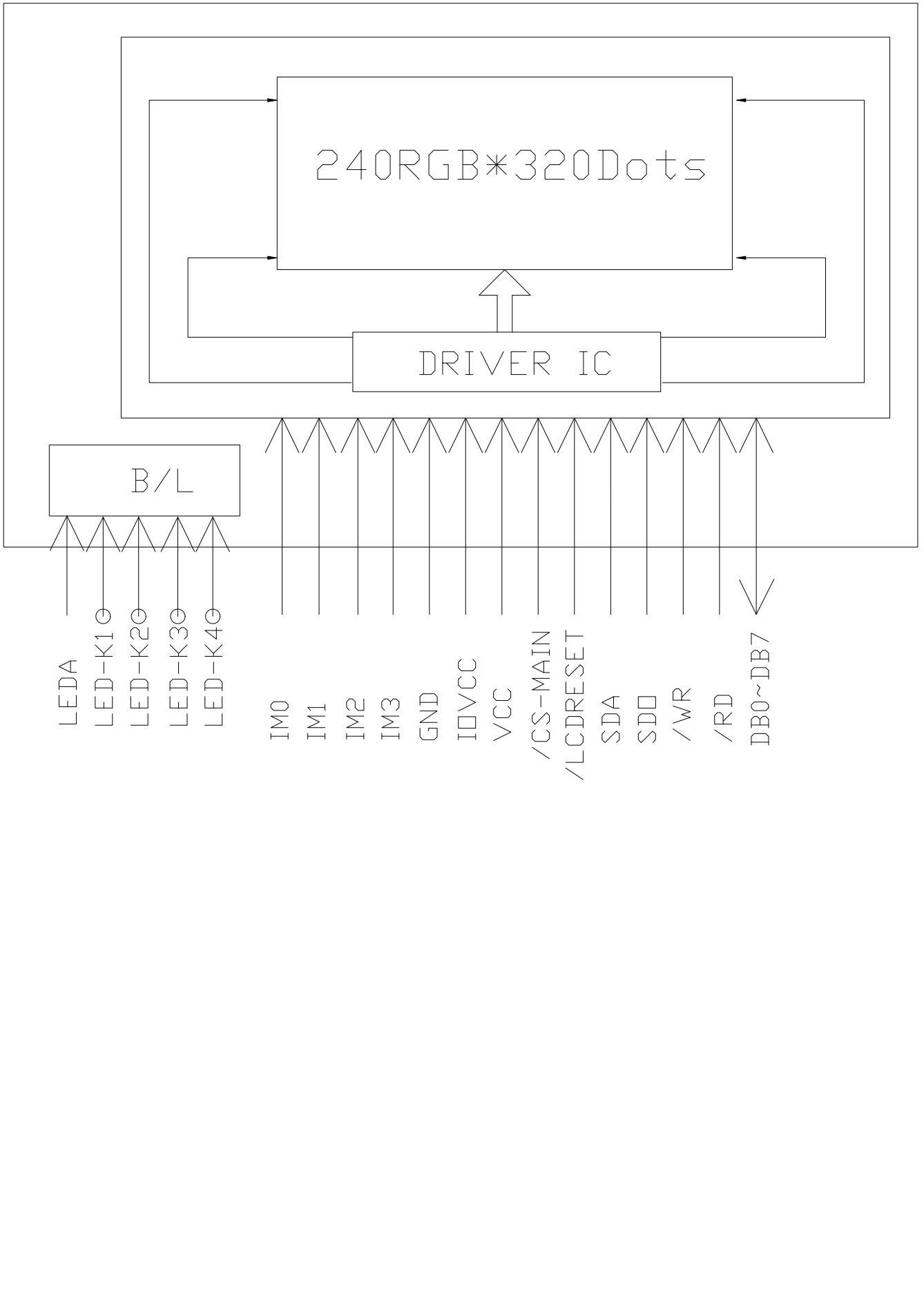
- Display terminals for POS machine or equivalent.

1.4 General Specification

No.	Item	Specification	Unit	Remark
1	LCD Size	2.8	inch	-
2	Panel Type	a-Si TFT active matrix	-	-
3	Resolution	240 x (RGB) x 320	pixel	-
4	Display Mode	Normally white, Transmissive	-	-
5	Display Number of Colors	262K	-	-
6	Viewing Direction	6 o'clock(Good View)	-	Note
7	Contrast Ratio	500(Typ)	-	-
8	Luminance	250(Typ)	cd/m ²	-
9	Module Size	50.0(W) x 69.2(L) x 2.25(T)	mm	Note
10	Active Area	43.2(W) x 57.6(L)	mm	Note
11	Pixel Pitch	0.18(W) x 0.18(L)	mm	-
12	Weight	TBD	g	-
13	Driver IC	ST7789V	-	-
14	Driver IC RAM Size	240x18x320	bit	-
15	Light Source	4 LEDs White	-	-
16	Interface	4-SPI	-	-
17	Operating Temperature	-20~70	°C	-
18	Storage Temperature	-30~80	°C	-

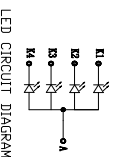
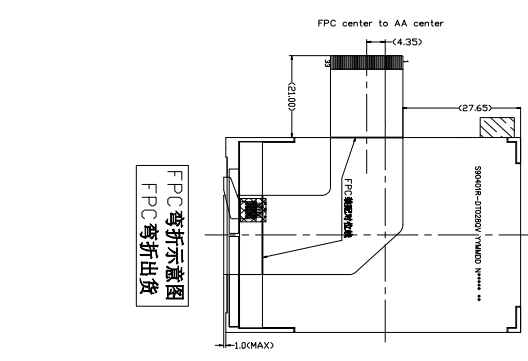
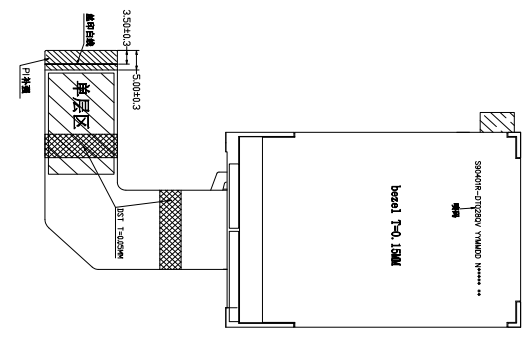
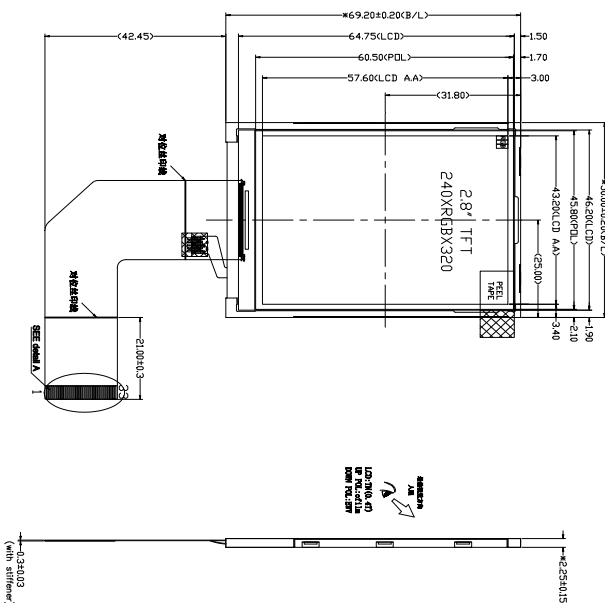
Note: Please refer to the mechanical drawing.

2. BLOCK DIAGRAM



3. MECHANICAL DRAWING

PIN NO.	DEFINITION
1	GND
2	GND
3	/CS-MAIN
4	DC
5	/VR
6	/RD
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	SDA
16	SDB
17	/LCDRESET
18	IM0
19	IM1
20	GND
21	GND
22	IM2
23	IM3
24	IM0(GND)
25	GND
26	VCC
27	IVCC
28	LED-K1
29	LED-K2
30	LED-K3
31	LED-K4
32	LED-A
33	LED-A



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DRAWING NO.			TITTLE		
STR-S90401R-DT028QV			MODULE SPEC.		
UNIT		mm	SCALE		FIT
3rd Angle			SHEET		1 OF 1
VER.	SYMBOL	AMENDMENT	SIGN	DATE	
01	新发行 (在S90401R基础上改为0.1mm+1mm, LCD使用0.4T)		lehui	2017.4.19	
DRAWN			CHECKED		
APPROVED			CUSTOMER'S APPROVAL		
SHENZHEN SUCCESS ELECTRONICS LTD					

Display Type	o-Si TFT-TRANSMISSIVE
Viewing Angle (Up/Down/Left/Right)	Best Image View: 6 O'clock 70/70/70/70(TYP)
Contrast Ratio	500(TYP)
Driver IC	517789V
Interface	4-SPI
Operating Voltage	VDD=2.8V IOVCC=1.8
Luminance	250(TYP)
Center CIE coordinate	X=0.29 Y=0.30
Backlight unit	WHITE(3.2V,60mA)
Connector type	
Operation Temp.	-20°C TO 70°C
Storage Temp.	-30°C TO 80°C

4.INTERFACE ASSIGNMENT

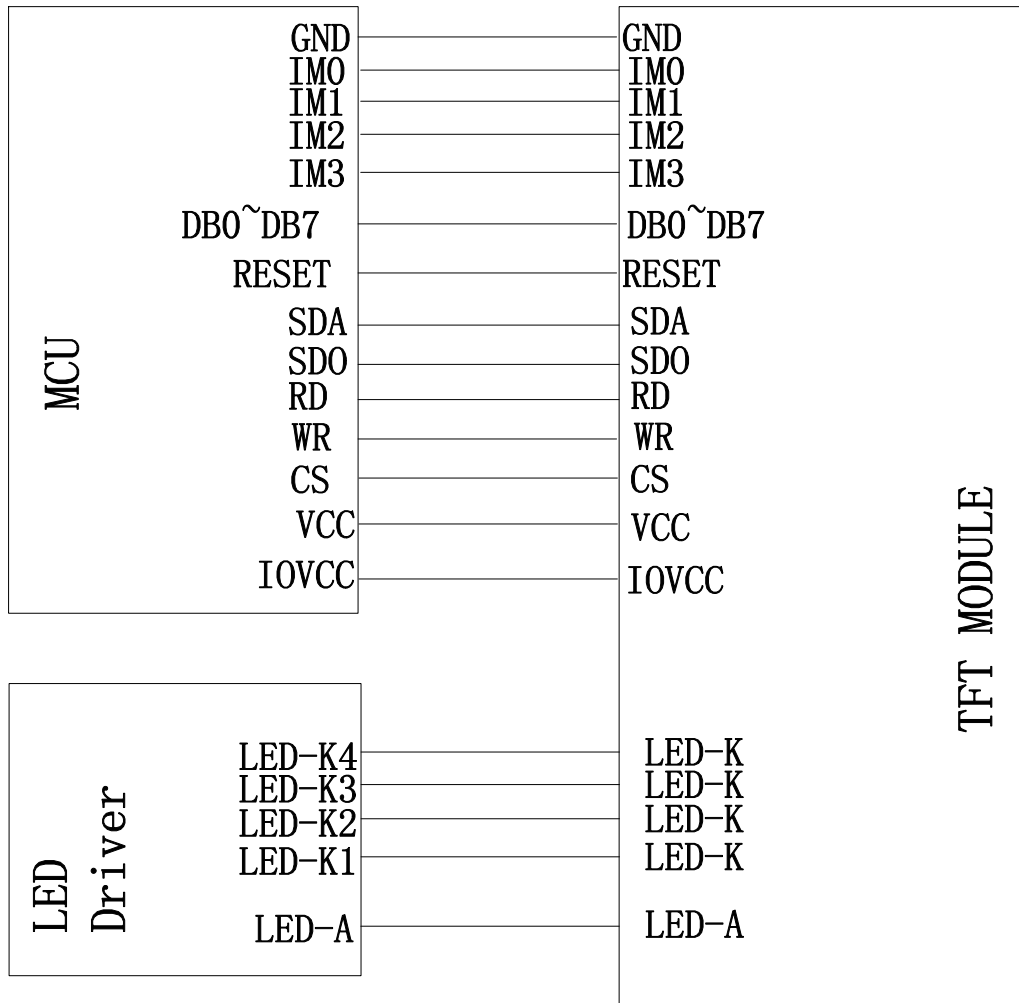
PIN NO.	SYMBOL	FUNCTION DESCRIPTIONS
1	GND	Ground.
2	GND	Ground.
3	CS	A chip selection signal. When CS is low,the chip can be accessed.
4	DC	Display data/command selection pin in parallel interface. This pin is used to be serial interface clock. When DC = 1, display data or parameter. When DC = 0, command data.
5	WR	Write enable in MCU parallel interface. Display data/command selection pin in 4-line serial interface.
6	RD	Read enable in 8080 MCU parallel interface.
7-14	D0-D7	Data bus.
15	SDA	SPI interface input/output pin.
16	SDO	SPI interface output pin.
17	RESET	This signal will reset the device and it must be applied to properly initialize the chip.
18	IM0	The MCU interface mode select.
19	IM1	The MCU interface mode select.
20	GND	Ground.
21	GND	Ground.
22	IM2	The MCU interface mode select.
23	IM3	The MCU interface mode select.
24	ID(GND)	LCD_identify pin.
25	GND	Ground.
26	VCC	Power Supply for Analog,
27	IOVCC	Power Supply for I/O System.
28	LED-K1	Power supply for backlight (cathode).
29	LED-K2	Power supply for backlight (cathode).
30	LED-K3	Power supply for backlight (cathode).
31	LED-K4	Power supply for backlight (cathode).
32	LED-A	Power supply for backlight (anode).

33	LED-A	Power supply for backlight (anode).
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Name	I/O	Description																																																																																
IM3, IM2, IM1, IM0	I	-The MCU interface mode select.																																																																																
		<table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>MPU Interface Mode</th> <th>Data pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>80-8bit parallel I/F</td> <td>DB[7:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>80-16bit parallel I/F</td> <td>DB[15:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>80-9bit parallel I/F</td> <td>DB[8:0]</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>80-18bit parallel I/F</td> <td>DB[17:0],</td> </tr> <tr> <td rowspan="2">0</td> <td rowspan="2">1</td> <td rowspan="2">0</td> <td rowspan="2">1</td> <td>3-line 9bit serial I/F</td> <td>SDA: in/out</td> </tr> <tr> <td>2 data lane serial I/F</td> <td>SDA: in/out WRX: in</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>4-line 8bit serial I/F</td> <td>SDA: in/out</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>80-16bit parallel I/F II</td> <td>DB[17:10], DB[8:1]</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>80-8bit parallel I/F II</td> <td>DB[17:10]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>80-18bit parallel I/F II</td> <td>DB[17:0],</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>80-9bit parallel I/F II</td> <td>DB[17:9]</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>3-line 9bit serial I/F II</td> <td>SDA: in/ SDO: out</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>4-line 8bit serial I/F II</td> <td>SDA:in/ SDO: out</td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0	MPU Interface Mode	Data pin	0	0	0	0	80-8bit parallel I/F	DB[7:0]	0	0	0	1	80-16bit parallel I/F	DB[15:0]	0	0	1	0	80-9bit parallel I/F	DB[8:0]	0	0	1	1	80-18bit parallel I/F	DB[17:0],	0	1	0	1	3-line 9bit serial I/F	SDA: in/out	2 data lane serial I/F	SDA: in/out WRX: in	0	1	1	0	4-line 8bit serial I/F	SDA: in/out	1	0	0	0	80-16bit parallel I/F II	DB[17:10], DB[8:1]	1	0	0	1	80-8bit parallel I/F II	DB[17:10]	1	0	1	0	80-18bit parallel I/F II	DB[17:0],	1	0	1	1	80-9bit parallel I/F II	DB[17:9]	1	1	0	1	3-line 9bit serial I/F II	SDA: in/ SDO: out	1	1	1	0	4-line 8bit serial I/F II	SDA:in/ SDO: out
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5. ELECTRICAL SPECIFICATION

5.1. APPLICATION CIRCUIT



5.2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	VDD	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	°C
Storage Temperature Range	TSTG	-40 ~ +125	°C

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded.

Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

5.3. TYPICAL OPERATION CONDITION**5.3.1 DC Characteristics**

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	VCC	Ta=25 °C	2.5	2.75	3.3	V
Power Supply for Digital IO	IOVCC	Ta=25 °C	1.65	1.8	3.3	V
Input Signal "H" Level	V _{IH}	-	0.7IOVCC	-	IOVCC	V
Input Signal "L" Level	V _{IL}	-	VSS	-	0.3IOVCC	V
Output Signal "H" Level	V _{OH}	I _{OH} =-0.1mA	0.8IOVCC	-	IOVCC	V
Output Signal "L" Level	V _{OL}	I _{OL} =0.1mA	VSS	-	0.2IOVCC	V

5.3.2 Current Consumption

Item	Symbol	Values		Unit	Remark
		type	Max.		
MCU Interface					
Normal(Still) Mode	I _{dd1}	6.0	15	mA	Note1
Standby Mode	I _{dd2}	-	100	uA	Note2

Note1: Test Condition

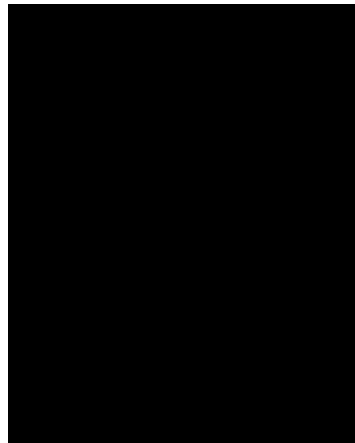
Typ: IOVCC=1.8V VCC=2.8V

Display Pattern: All Pixel Black

Frame Rate=60Hz at Line Inversion

Operating Temperature: 25°C

Max. current check pattern:

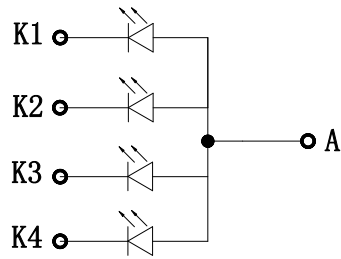


Black

Note2: In the standby mode, all the internal display operations are suspended including the internal R-C oscillator.

5.4. BACKLIGHT SPECIFICATION

5.4.1 BACKLIGHT CIRCUIT



LED CIRCUIT DIAGRAM

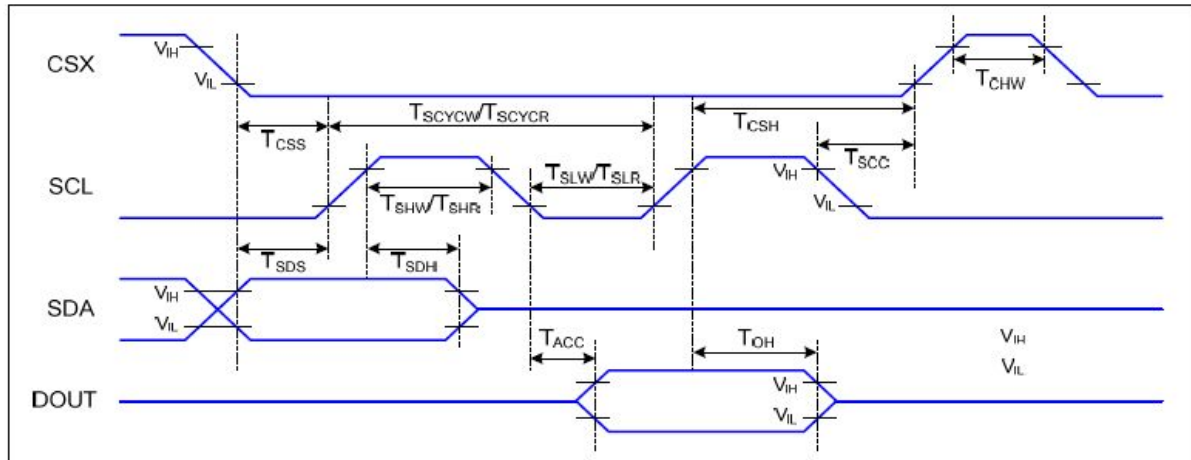
5.4.2 ELECTRICAL CHARACTERISTICS

(T=25°C)

PARAMETER	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
FORWARD VOLTAGE (Single Chip)	VF	IF=20mA	2.9	3.2	3.4	v

5.5. INTERFACE TIMING CHARACTERISTICS

Serial Interface Characteristics (3-line serial):

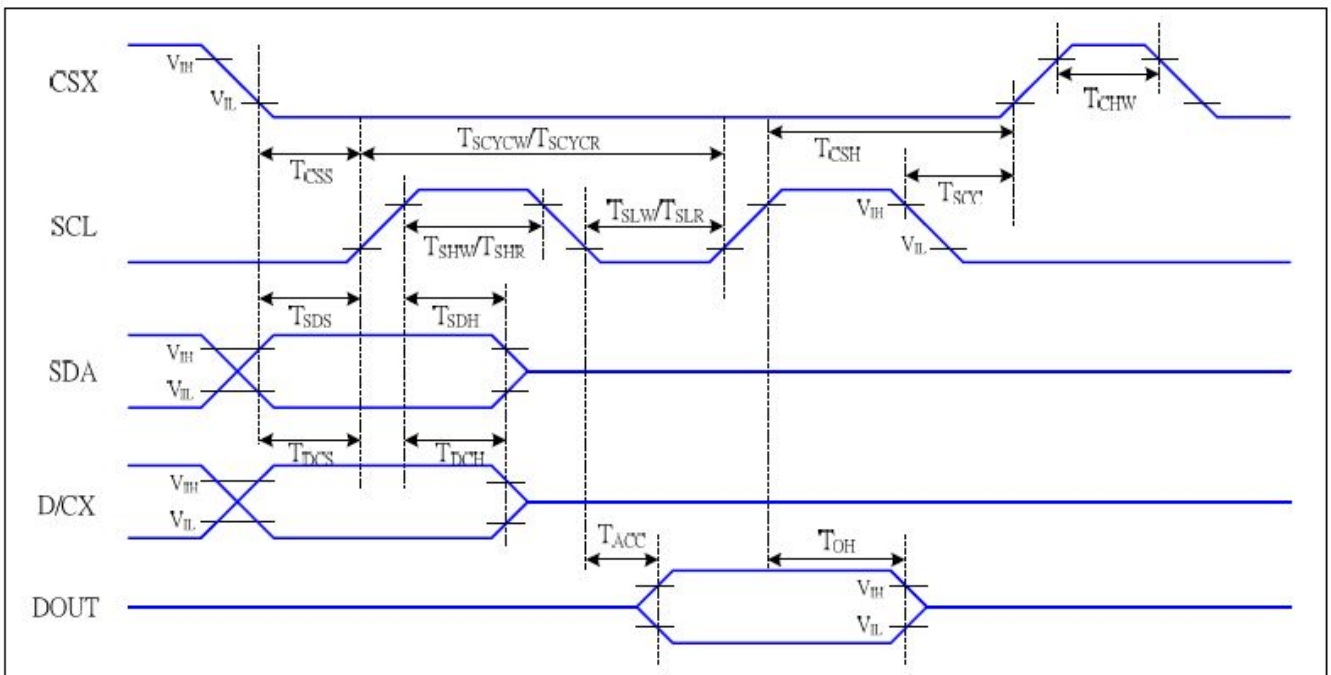


VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, T_a =-30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note : The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Serial Interface Characteristics (4-line serial):



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, $T_a=-30$ to 70 °C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note : The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

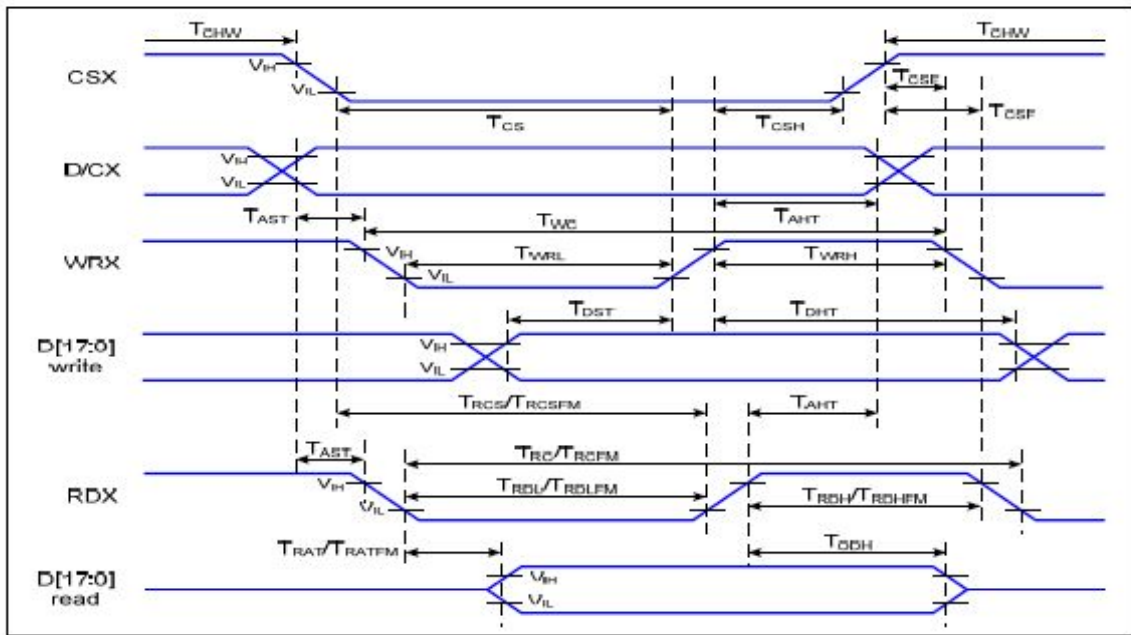


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 °C

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RCS}	Chip select setup time (Read ID)	45		ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	66		ns	
	T _{WRH}	Control pulse "H" duration	15		ns	
	T _{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T _{RC}	Read cycle (ID)	160		ns	When read ID data
	T _{RDH}	Control pulse "H" duration (ID)	90		ns	
	T _{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T _{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T _{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T _{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T _{DST}	Data setup time	10		ns	For CL=30pF

T_{DHT}	Data hold time	10		ns
T_{RAT}	Read access time (ID)		40	ns
T_{RATFM}	Read access time (FM)		340	ns
T_{ODH}	Output disable time	20	80	ns

Table 4 8080 Parallel Interface Characteristics

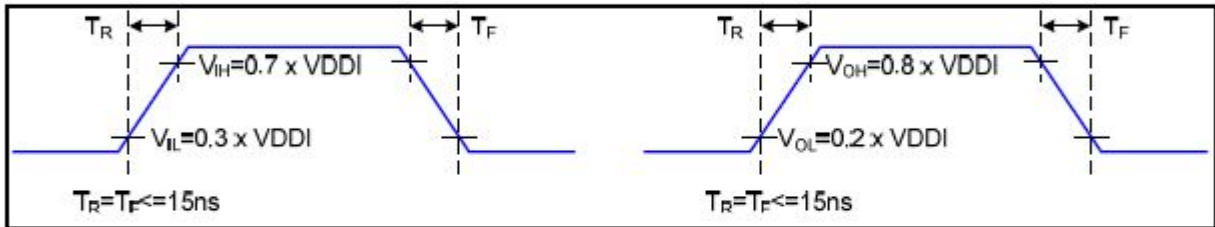


Figure 2 Rising and Falling Timing for I/O Signal

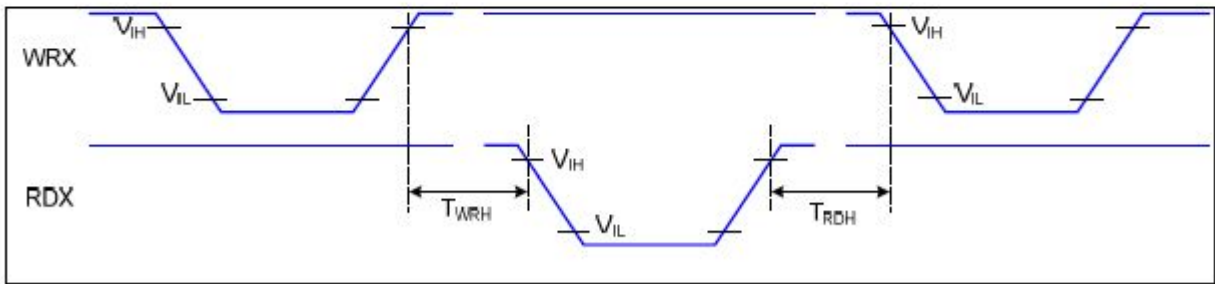


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_r , T_f) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.6. RESET TIMING CHARACTERISTICS

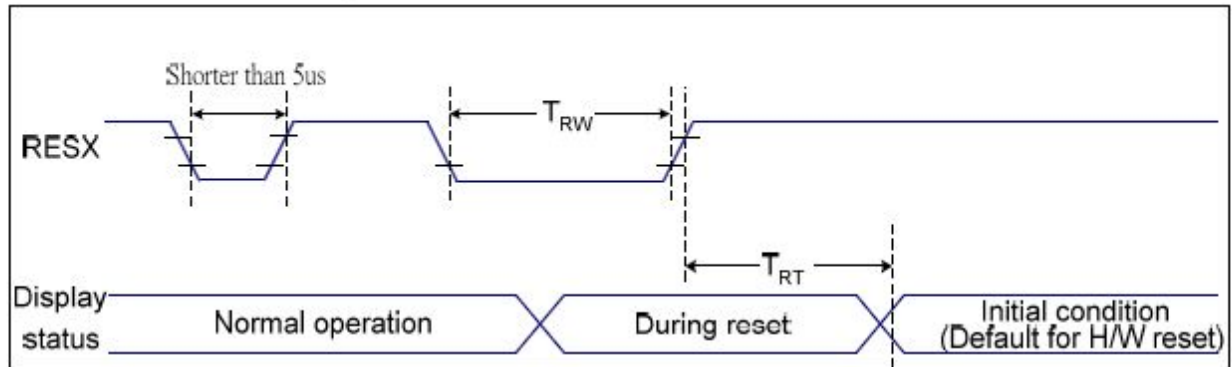


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, $T_a=-30 \sim 70 \text{ }^\circ\text{C}$

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

- During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

- Spike Rejection also applies during a valid reset pulse as shown below:

6. OPTICAL CHARACTERISTICS

(T_a=+25°C, VCC=IOVCC=+2.8V, I_B=60mA)

Item	Symbol	Condition	Values			Unit	Remark	
			Min.	Typ.	Max.			
Viewing Angle Range	Left	θ _L	CR ≥ 10	-	70	-	degree	Note 1,2
	Right	θ _R		-	70	-		
	Top	Φ _T		-	70	-		
	Botto	Φ _B		-	70	-		
Response Time	T _{on} + T _{off}	Normal θ=φ=0°	-	16	-	ms	Note 2,3	
Contrast Ratio	CR	Normal θ=φ=0°	-	500	-	-	Note 2,4	
Luminance	L	Normal θ=φ=0°	-	250	-	cd/m ²	Note 2,5	
Color Chromaticity (CIE1931)	White	W _x	Normal θ=φ=0°	-	0.307	-	-	Note 2,6
		W _y		-	0.329	-		
	Red	R _x		-	0.626	-		
		R _y		-	0.336	-		
	Green	G _x		-	0.276	-		
		G _y		-	0.550	-		
	Blue	B _x		-	0.144	-		
		B _y		-	0.13	-		
Color Gamut	NTSC	CIE1931	-	55.3	-	%	-	
Luminance Uniformity	U _L	Normal θ=φ=0°	75	80	-	%	Note 2,7	

Judgement criterion:

$$\Delta c'_{\text{白}} = \sqrt{(\Delta u')^2 + (\Delta v'/1.5)^2} = \sqrt{(u'_{\text{白}} - u'_{\text{白0}})^2 + [(v'_{\text{白}} - v'_{\text{白0}})/1.5]^2}$$

, the "u'_{白0}" and "u'_{白0}" is the type value in the Figure 1.

the error of the Red 、 Green and Blue must be controlled as follow

$$\Delta c'_{\text{白}} \leq 0.0115, \Delta c'_{\text{红}} \leq 0.0230, \Delta c'_{\text{绿}} \leq 0.0230, \Delta c'_{\text{蓝}} \leq 0.0230。$$

Note 1: Definition of viewing angle range

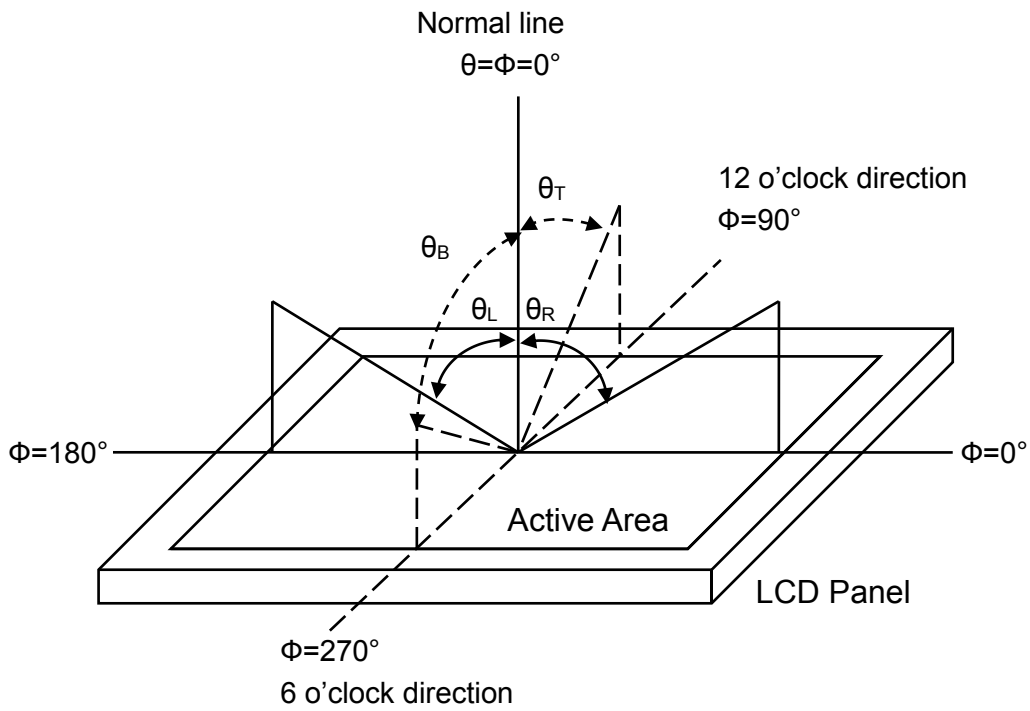


Fig. 1 Definition of viewing angle

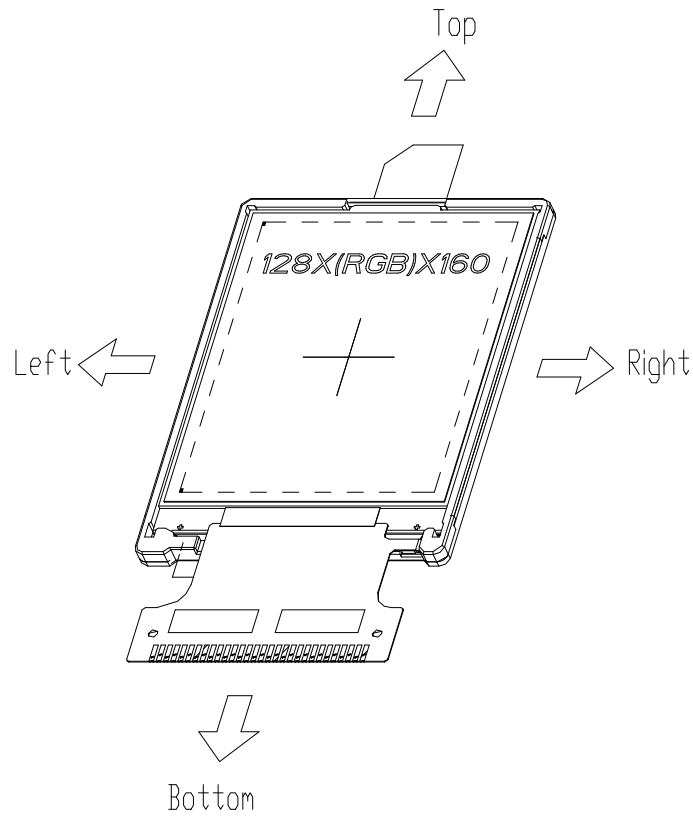


Fig. 2 Definition of viewing angle for display

Note 2: Definition of optical measurement system

The optical characteristics should be measured in a dark room with ambient temperature $T_a=+25^{\circ}\text{C}$. The optical properties are measured at the center point of the LCD screen after 5 minutes operation. (Equipment: Photo detector TOPCON BM-5AS Field of view: 1° /Height: 500mm.)

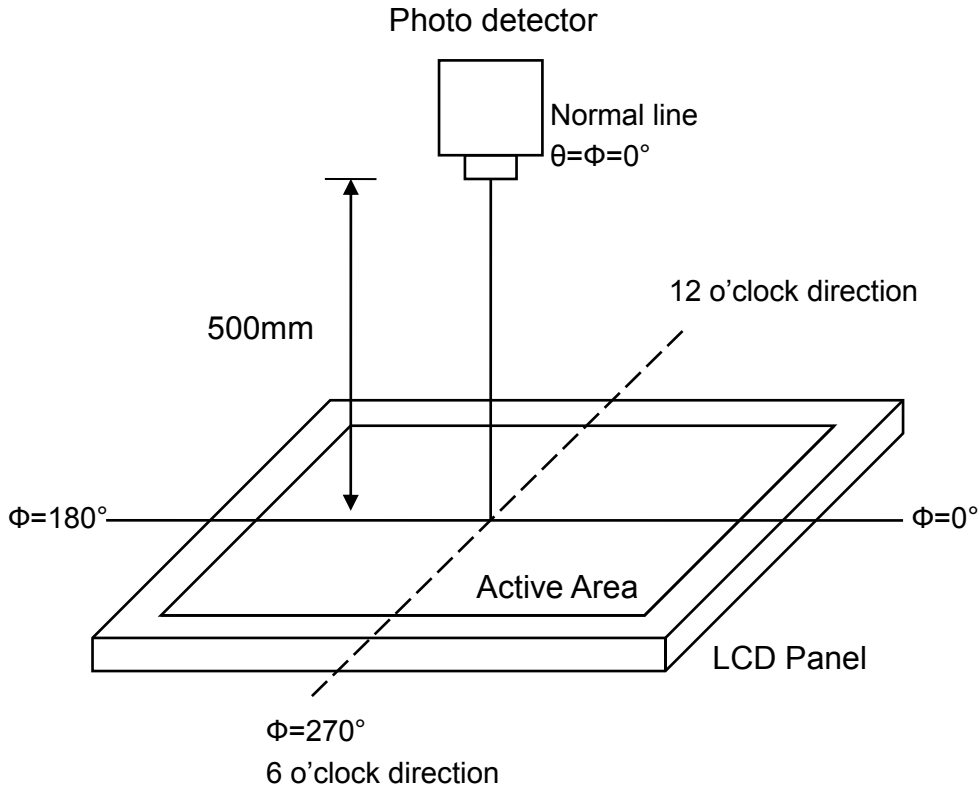


Fig. 3 Optical measurement system setup

Note 3: Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{on}) is the time between photo detector output intensity changed from 90% to 10%, and fall time (T_{off}) is the time between photo detector output intensity changed from 10% to 90%.

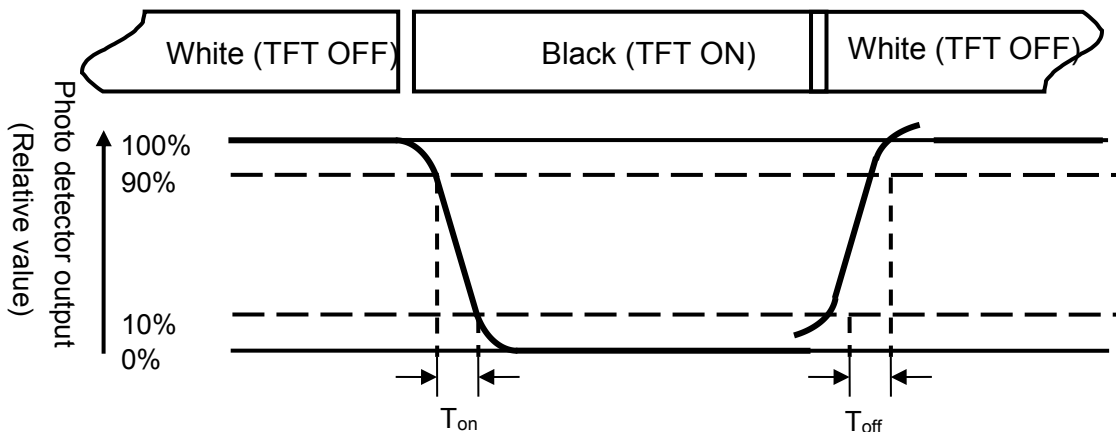


Fig. 4 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of luminance

Measured at the center area of the panel when LCD panel is driven at “white” state.

Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD when panel is driven at “White”, “Red”, “Green” and “Blue” state respectively.

Note 7: Definition of luminance uniformity

To test for uniformity, the tested area is divided into 3 rows and 3 columns. The measurement spot is placed at the center of each circle as below.

$$\text{Luminance Uniformity (U}_L\text{)} = \frac{L_{\min}}{L_{\max}}$$

L-----Active area length W----- Active area width

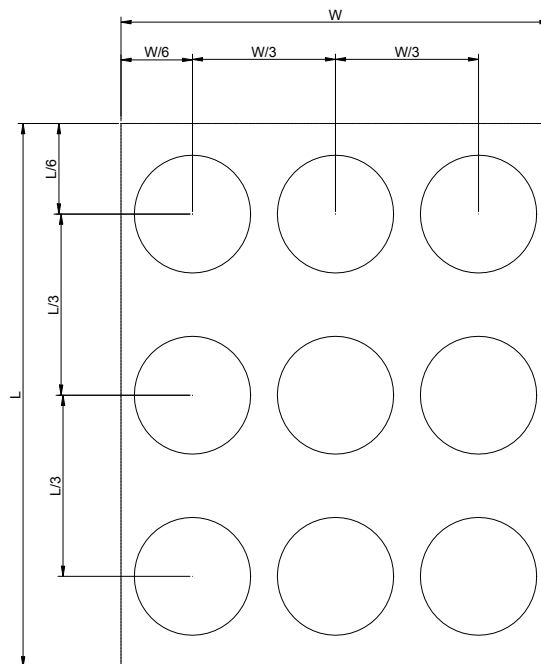


Fig. 5 Definition of luminance uniformity

L_{\min} : The measured minimum luminance of all measurement position.

L_{\max} : The measured maximum luminance of all measurement position.

7. RELIABILITY TESTS

ITEM	CONDITION	CRITERION
Operating Temperature Test	High Temperature: +70 °C, 120 hrs	No defects in display and operational functions
	Low Temperature: -20 °C, 120 hrs	
Storage Temperature Test	High Temperature: +80 °C, 120 hrs	No defects in display and operational functions
	Low Temperature: -30 °C, 120 hrs	
Humidity Endurance Test	55 °C, 95%RH, 48 hrs	No defects in display and operational functions
Thermal Shock Test	-30 °C (30mins)~ +80 °C (30mins) 10 cycles	No defects in display and operational functions
Vibration Resistance Test	Operating Time: thirty minutes exposure for each direction (X,Y,Z) Sweep Frequency:10~55Hz (1 min) Amplitude: 1.5mm	No defects in display and operational functions
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	No defects in display and operational functions
Package Vibration Test	Random Vibration : 0.015G ² /Hz from 5-200Hz, -6dB/Octave from 200-500Hz 1 hour for each direction of X. Y. Z. (3 hours for total)	No defects in display and operational functions
Package Drop Test	Height :72cm(Weight ≦ 10kg); 60cm(Weight ≧ 10kg) 1 corner, 3 edges, 6 surfaces	No defects in display and operational functions
Electro Static Discharge	± 2KV, Human Body Mode, 100pF/1500Ω ± 8KV,Air Mode,150pF/330Ω	No defects in display and operational functions
Life Time	20,000H	Functions,performance,appearance,etc,shall be free from remarkable deterioration under ordinary operating and storage conditions at room temperature(25+/-10°C), normal humidity(45+/-20%RH),and in area not exposed to direct sunlight

NOTE:

- 1) The samples must be free from defect before test, must be restored at room condition at least for 2 hours after reliability test before any inspection.
- 2) Before test the function of TP, the sample must be placed in room temperature for 24hrs after RA test.

8. PRECAUTIONS

8.1. HANDLING

- 8.1.1. Polarizer Cleaning, Petroleum ether (or N-hexane) is recommended for cleaning the front/rear polarizers and reflectors, acetone, toluene and ethanol are not allowed to avoid damaging the surface.
- 8.1.2. Body grounding, must wear Anti-ESD wrist strap while pick up LCDs.
- 8.1.3. FPC Soldering, less than 300°C/3S, solder must be grounding on grounding bench.
- 8.1.4. If use electric Screwdriver to do assembly, screwdriver must be grounding.

8.2. STORAGE

- 8.2.1. Keep in a sealed polyethylene bag.
- 8.2.2. Keep in a dark place.
- 8.2.3. Keep in temperature between 0°C and 35°C.
NOT allowed at 70°C for more than 160 Hours, or at -20°C for more than 48 Hrs.

8.3. SAFETY

If liquid crystal leak out of a damaged glass cell, **DO NOT** put it in your mouth or touch eyes, if the liquid crystal touch your skin or clothes, please wash it off immediately using soap and water.

9. LIMITED WARRANTY

Unless otherwise agreed between SUCCESS and customer, SUCCESS will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with SUCCESS LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects over specs must be returned to SUCCESS within 30 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of SUCCESS limited to repair and/or replacement on the terms set forth above. SUCCESS shall not be responsible for any subsequent or consequential events.

9.1. RETURNING LCM UNDER WARRANTY – TERMS AND CONDITIONS

- 9.1.1. No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :
 - Broken LCD glass.
 - Circuit modified in any way, including addition of components.
- 9.1.2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB's eyelet, conductors and terminals.