DATA IMAGE CORPORATION

TFT Module Specification

Preliminary

ITEM NO.: FG0403C1DSSWMG01

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Customer Companies	R&D Dept.	Q.C. Dept.	Eng. Dept.	Prod. Dept.
	JACK	JOE	GARY	KEN
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2. RECORD OF REVISION

Rev	Date	Item	Page	Comment
1	10/NOV/11’			Initial Preliminary

3. INTRODUCTION

The FG0403C1 is a kind of Transmissive TFT, active matrix color liquid crystal display (LCD) comprising an amorphous silicon TFT attached to each signal electrode. This module is consisting of TFT-LCD module, a driver circuit, a back-light unit. The resolution of a 4.3'' contains 480x(RGB)x800 pixels.

4. GENERAL SPECIFICATIONS

Parameter	Specifications	Unit
Screen Size	4.3 (diagonal)	inch
Display Format	480(H) x (R,G,B) x 800(V)	dot
Active Area	56.16(W) ×93.6 (H) mm	mm
Pixel Pitch	0.117(W) × 0.117(H) mm	mm
Pixel Configuration	Stripe	
Outline Dimension	61.6(W) x107 (H) x2.6 (D)	Mm
Back-light	LED	
TFT-LCD Display mode	Normally black	
Weight	T.B.D(typ)	g
View Angle direction(TFT)	All	

5. ABSOLUTE MAXIMUM RATINGS

GND=0V

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Power supply voltage	VCC	-0.3	4.6	V	
	IOVCC	-0.3	4.6	V	
	VCI	-0.3	4.6	V	
Operating temperature	Top	-20	70	℃	
Storage temperature	Tst	-30	80	℃	

6. ELECTRICAL CHARACTERISTICS

6.1 Operating Conditions

GND=0V,Ta=25°C

Parameter	Symbol	MIN.	Typ.	MAX.	Unit	Remark
Power Supply voltage	VCC	2.5	-	3.3	V	
	IOVCC	2.5	-	3.3	V	
	VCI	2.5	-	3.3	V	
"H" level logical input voltage	V_{IH}	0.7*IOVCC	-	IOVCC	V	
"L" level logical input voltage	V_{IL}	0	-	0.3*IOVCC	V	

6.2 Current Consumption

Ta= 25℃

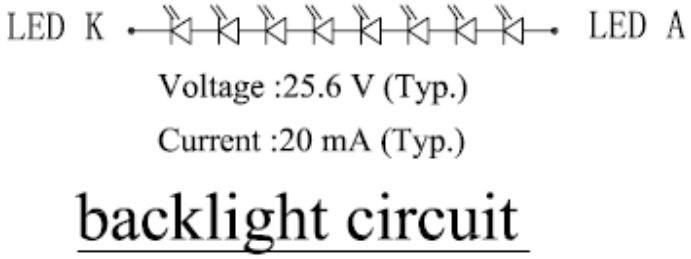
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Current for Power Supply Voltage	IVCC	-	TBD	TBD	mA	
	IIOVCC	-	TBD	TBD	mA	
	IVCI	-	TBD	TBD	mA	

6.3 Backlight Driving Consumption

Ta= 25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V_L		25.6		V	Note1
LED current	I_L	-	20	-	mA	Note1
LED dice Life Time		TBD			hr	Note2

Note 1:

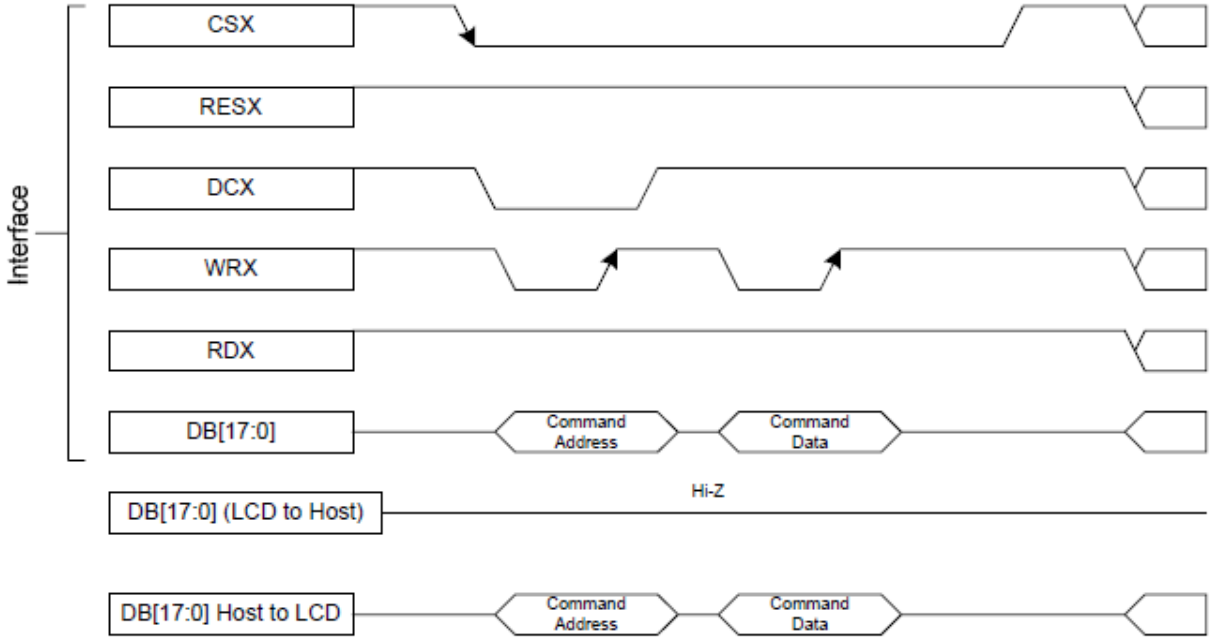


Note 2:
The “LED dice life time” is defined as the brightness decrease to 50% original brightness that the ambient temperature is 25℃ and LED dice current=20mA.

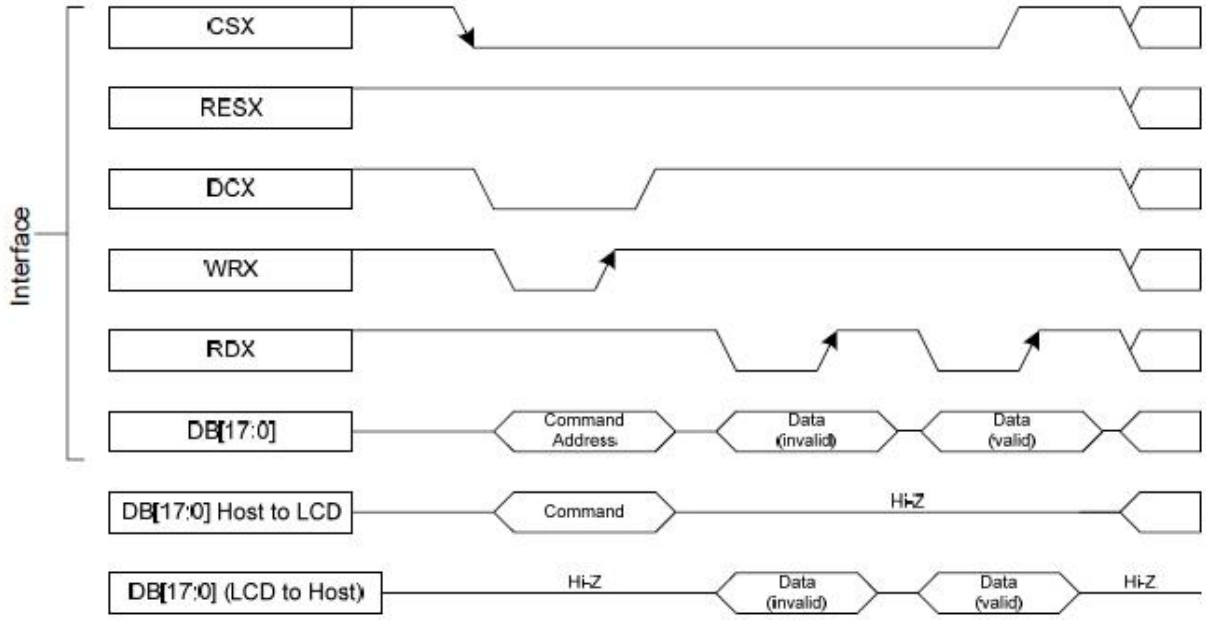
7. INPUT SIGNAL TIMING

7.1 MCU Interface

7.1.1 Write Cycle Sequence



7.1.2 Read Cycle Sequence



7.1.3 MCU Interface Set Table

8080 18-bit MPU interface, IM[2:0]=000

	DBI[2]	DBI[1]	DBI[0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Command/Parameter Write	X	X	X											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	X	X	X											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	DBI[2]	DBI[1]	DBI[0]	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	1	1	0	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	1	1	0	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

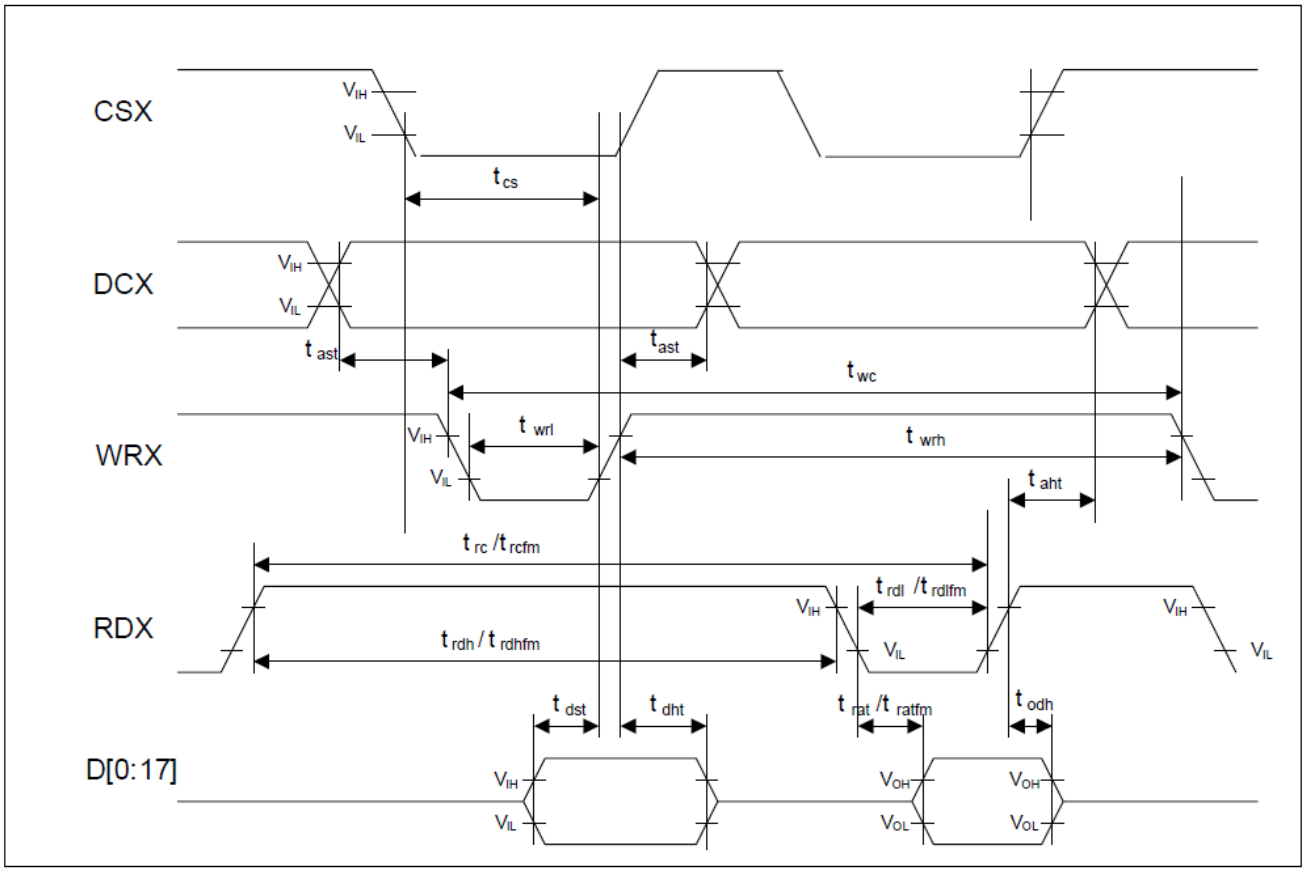
8080 16-bit MPU interface, IM[2:0]=010

	DBI[2]	DBI[1]	DBI[0]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Command/Parameter Write	X	X	X									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	X	X	X									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	DBI[2]	DBI[1]	DBI[0]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	1	0	1	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	1	0	1	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]

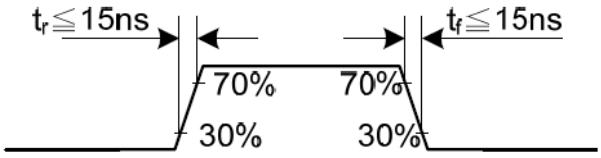
7.1.4 MCU Interface AC Characteristics

8080 16/18 bit Interface Timing Characteristics

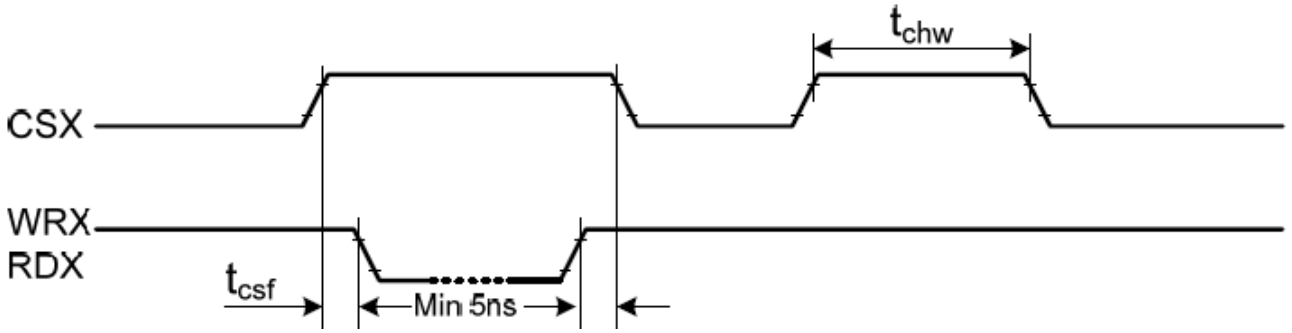


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	10	-	ns	-
WRX	twc	Write cycle	30	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB[17:0], DB[15:0],	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trodh	Read output disable time	20	80	ns	

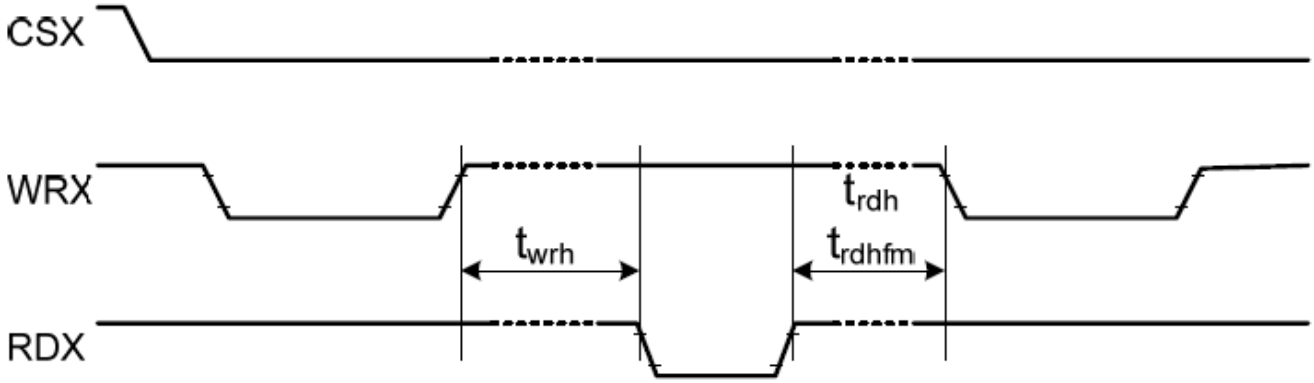
Note 1:



Note 2: Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.



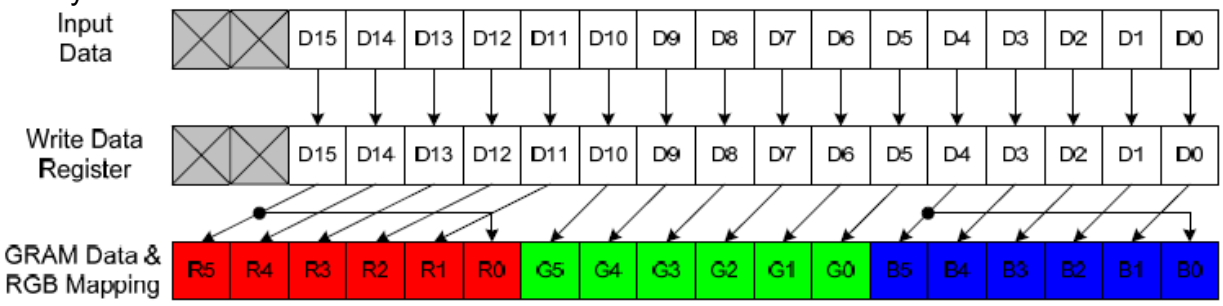
Note 3: Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.



7.2 SPI + Parallel RGB Interface (IM[2:0]=101)

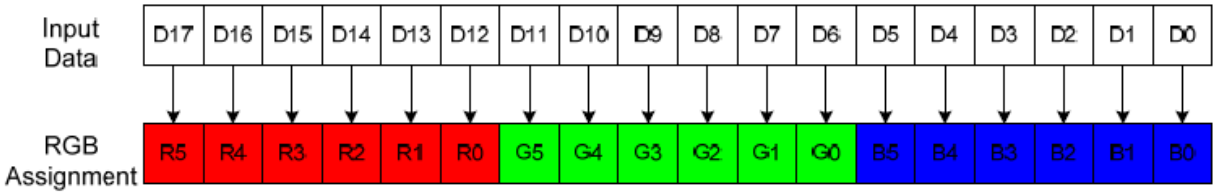
7.2.1 16-bit Parallel RGB Interface (DPI[2:0]=101)

The 16-bit RGB interface is selected by setting the DPI[2:0] bits to “101”. The display operation is synchronized with VSYNC, HSYNC and DCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D[15:0]) according to the data enable signal (ENABLE). Both D17 and D16 pins must be left to OPEN for ensure normally operation. Registers can be set by the system interface.



7.2.2 18-bit Parallel RGB Interface (DPI[2:0]=110)

The 18-bit RGB interface is selected by setting the DPI[2:0] bits to “110”. The display operation is synchronized with VSYNC, HSYNC, and DCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D[17:0]) according to the data enable signal (ENABLE). Registers can be set by the system interface.



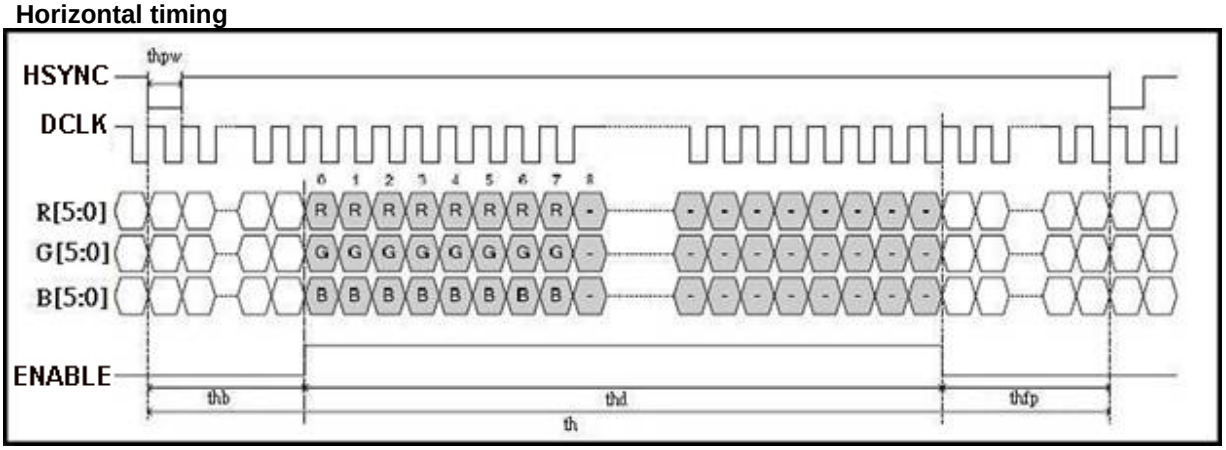
7.2.3 Parallel 16/18 bit RGB Interface Timing

7.2.3.1 Timing Data

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
DCLK frequency	F_{CPH}	25	28.8	35	MHz
DCLK period	T_{CPH}	28.5	34.7	40	ns
DCLK pulse duty	T_{CWH}	40	50	60	%
HSYNC period	th		534		T_{CPH}
HSYNC pulse width	thpw	3	26		T_{CPH}
HSYNC Back Porch	thb		12		T_{CPH}
Horizontal Display Area	thd	480	480	480	T_{CPH}
HSYNC Front Porch	thfp		16		T_{CPH}
VSYNC period	tv		900		T_H
VSYNC pulse width	tvpw	1	30	20	T_H
VSYNC Back Porch	tvb		30		T_H
Vertical Display Area	tvd	800	800	800	T_H
VSYNC Front Porch	tvfp		40		T_H

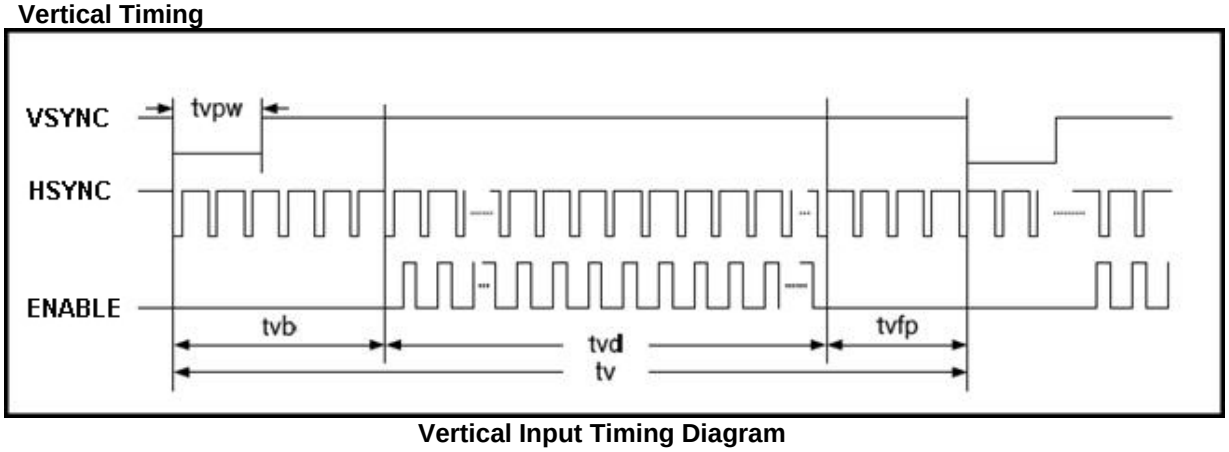
7.2.3.2 Timing Diagram

Horizontal timing



Horizontal Input Timing Diagram

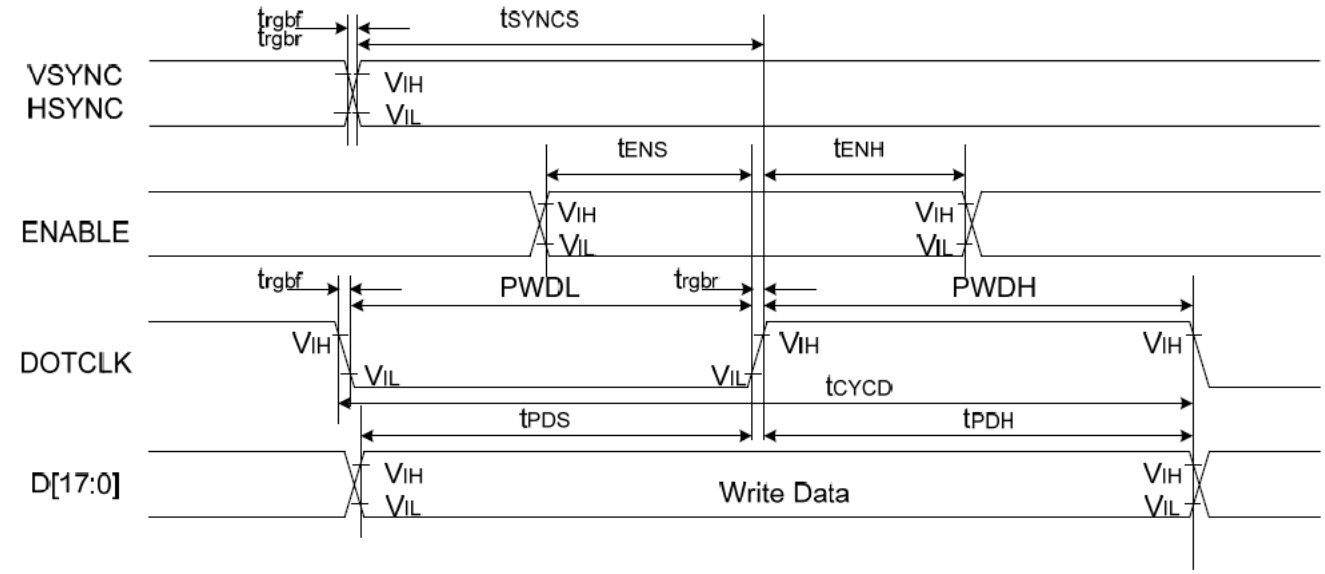
Vertical Timing

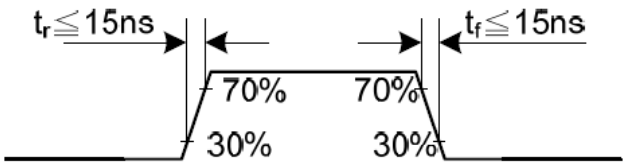


Vertical Input Timing Diagram

7.2.3.3 Parallel 16/18 bit RGB Interface AC Timing Characteristics

Signal	Symbol	Parameter	min	max	Unit
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns
	t_{ENH}	ENABLE hold time	15	-	ns
DB[17:0]	t_{POS}	Data setup time	15	-	ns
	t_{PDH}	Data hold time	15	-	ns
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns
	PWDL	DOTCLK low-level period	15	-	ns
	t_{CYCD}	DOTCLK cycle time	30	-	ns
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	_	15	ns

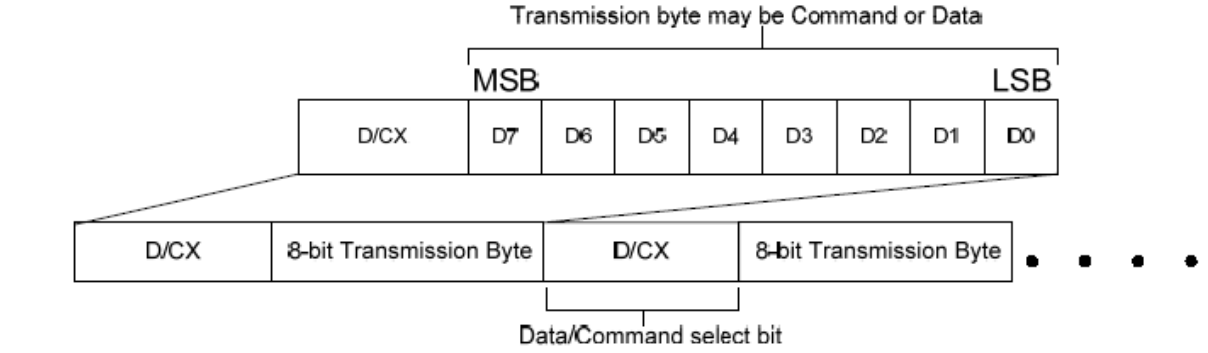




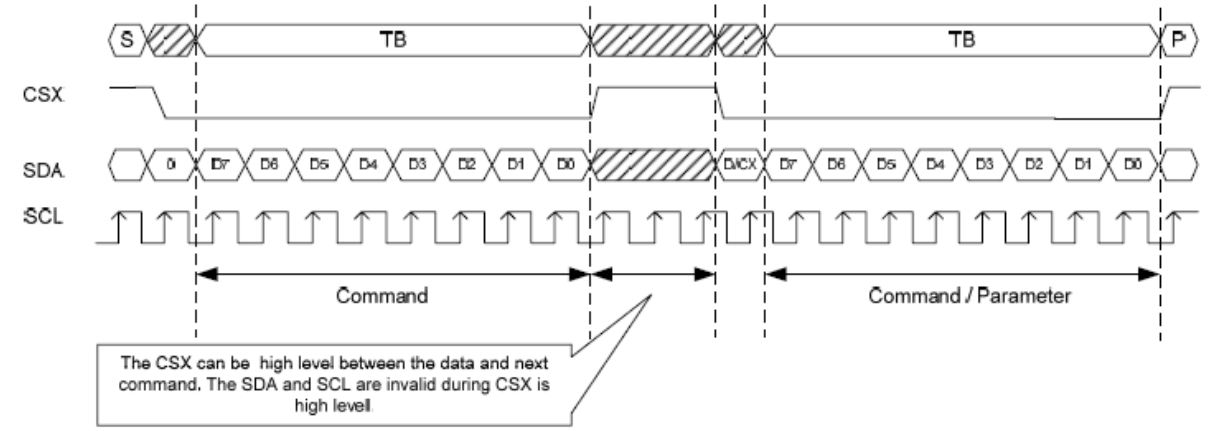
7.2.4 Display Serial Interface Timing Characteristics (3-line SPI system)

7.2.4.1 SPI Interface Data Format

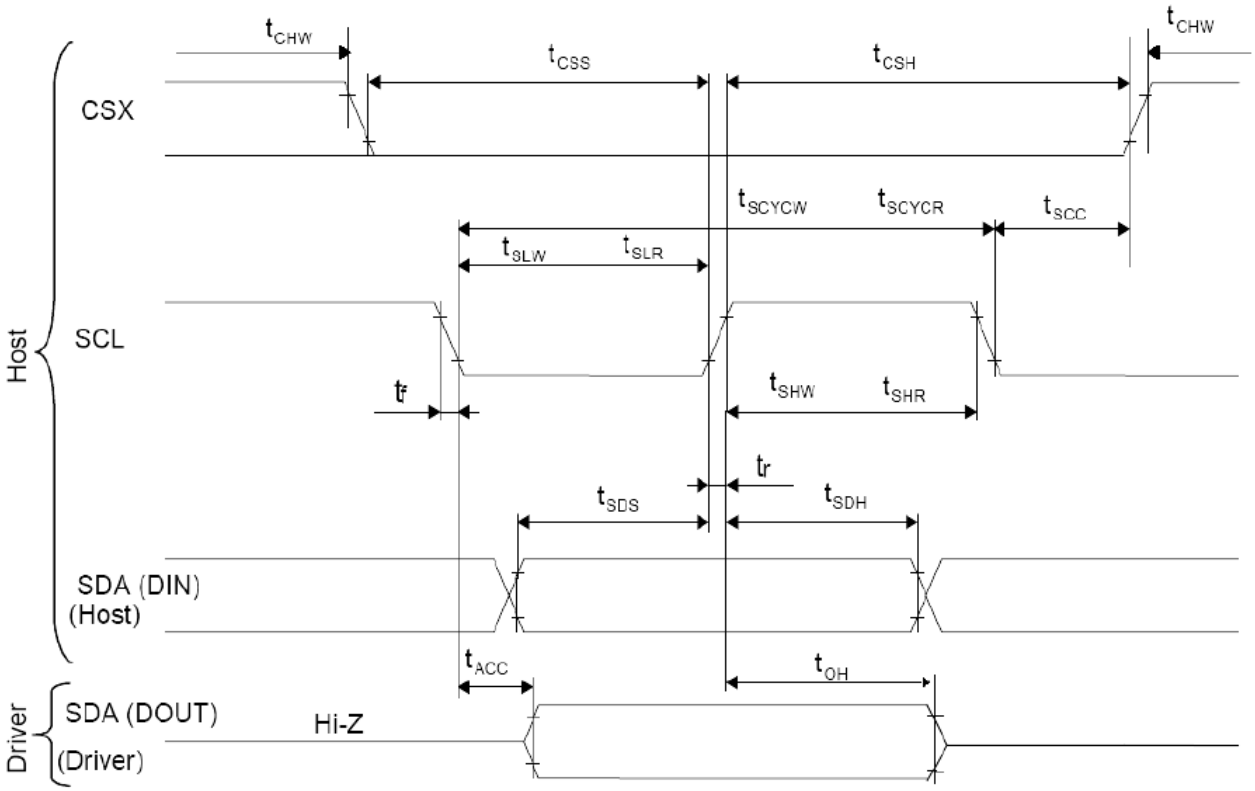
Data Format for 3-line Serial Interface



3-line Serial Interface Protocol

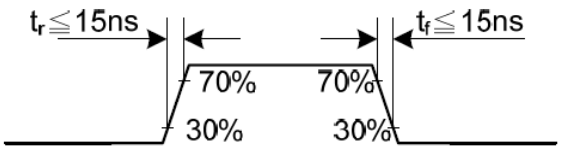


7.2.4.2 SPI Interface AC Timing Characteristics

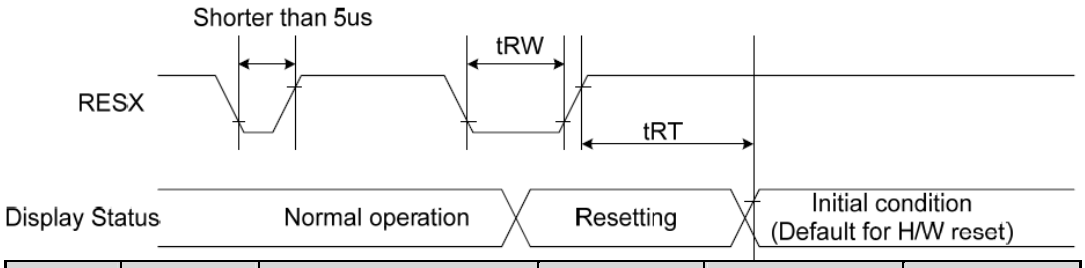


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	40	-	ns	
	tshw	SCL “H” Pulse Width (Write)	15	-	ns	
	tslw	SCL “L” Pulse Width (Write)	15	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	60	-	ns	
	tslr	SCL “L” Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	10	-	ns	
	tsdh	Data hold time (Write)	10	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	60	ns	
	toh	Output disable time (Read)	15	-	ns	
CSX	tscc	SCL-CSX	30	-	ns	
	tchw	CSX “H” Pulse Width	60	-	ns	
	tcss	CSX-SCL Time	15	-	ns	
	tcsh		15	-	ns	

Note :



7.3 Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
Resx	tRW	Rest pulse duration	10		uS
	tRT	Reset cancel		5 (note1.5)	ms
				120 (note1.6.7)	ms

Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

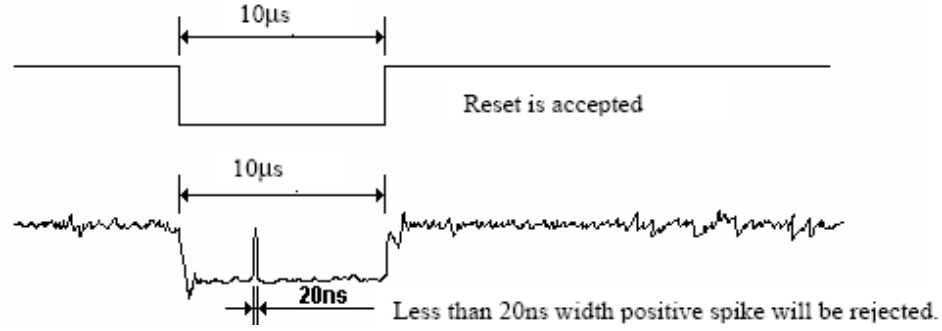
Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence,

which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

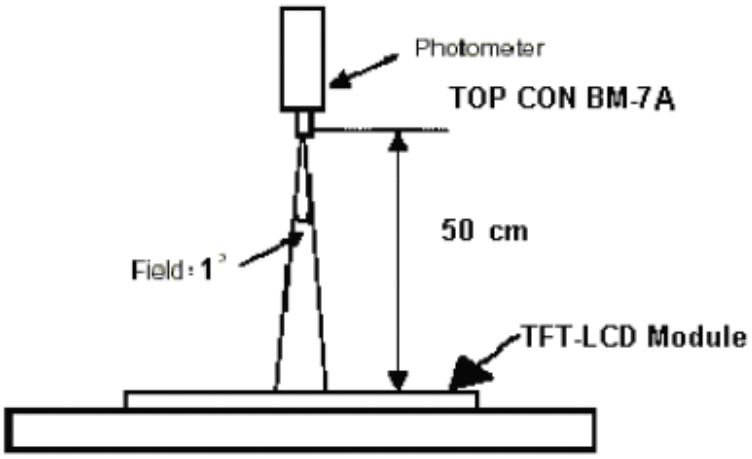
Note7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. OPTICAL CHARACTERISTIC

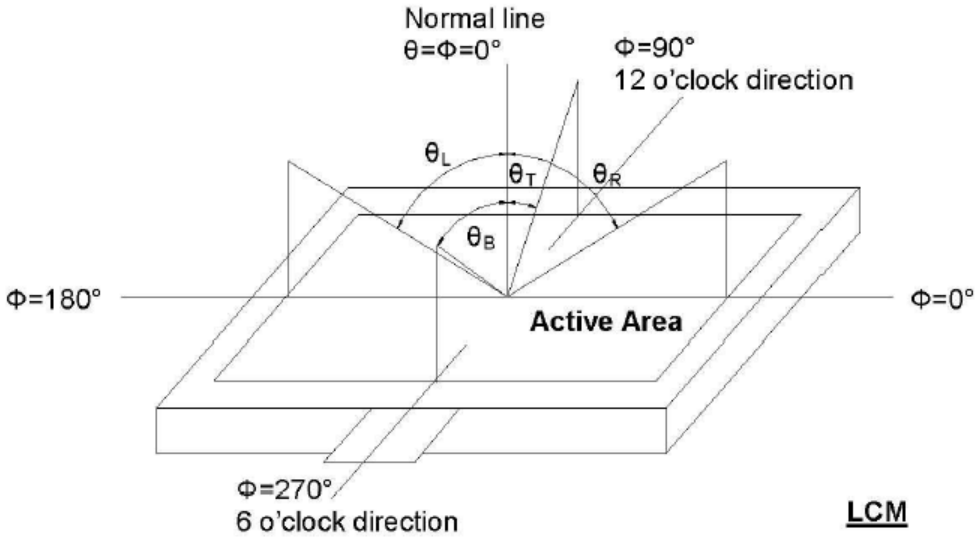
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle		θL	Center CR≥10	70	80	-	deg	Note 1,2
		θR		70	80	-		
		θT		70	80	-		
		θB		70	80	-		
Contrast Ratio		CR	at optimized viewing angle	-	800	-		Note 1,4
Response time		Tr+Tf	Center θx=θy =0°	-	25	-	ms	Note 1,6
Uniformity		B-uni	θx=θy =0°	70		-	%	Note 1,5
Brightness		L	θx=θy =0°	-	350	-	cd/㎡	Note 1,3
Chromaticity	W	x_W	Center θx=θy =0°	TYP-0.05	0.285	TYP+0.05		Note 1,7
		y_W			0.333			
	R	x_R	Center θx=θy =0°		TBD			
		y_R			TBD			
	G	x_G	Center θx=θy =0°		TBD			
		y_G			TBD			
	B	x_B	Center θx=θy =0°		TBD			
		y_B			TBD			

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance ≤1 lux, and at room temperature). The operation temperature is 25°C±2°C and LED Backlight Current IL=20mA. The measurement method is shown in Note1.

Note 1: The method of optical measurement:



Note 2: Definition of viewing angle range

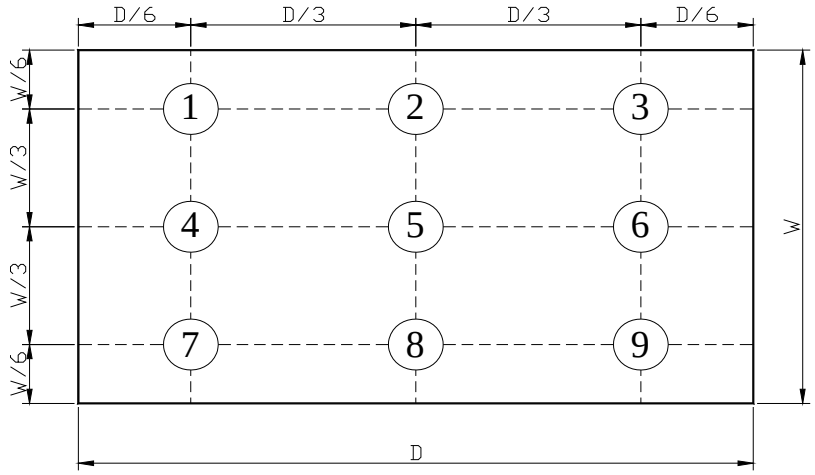


Note 3: Measured at the center area of the panel and at the viewing angle of the θx=θy =0°

Note 4: Definition of Contrast Ratio (CR):

$$CR = \frac{\text{Luminance with all pixels in white state}}{\text{Luminance with all pixels in Black state}}$$

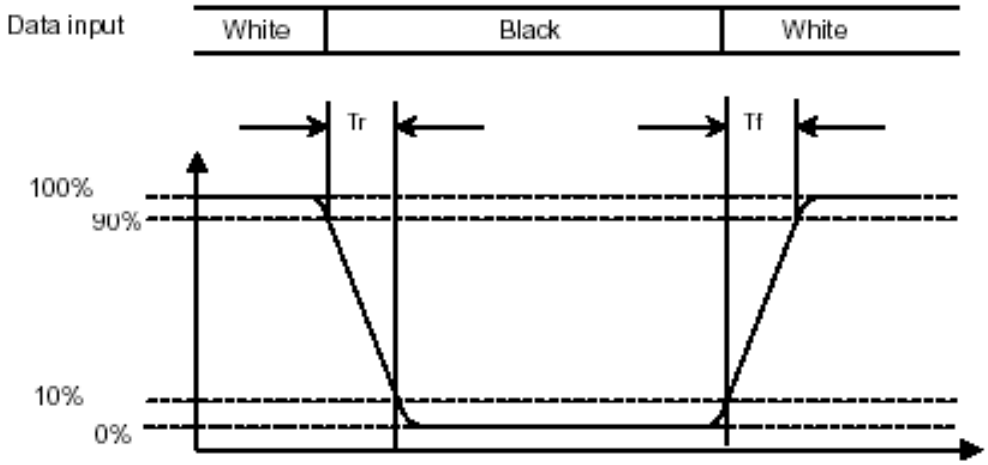
Note 5: Definition of Brightness Uniformity (B-uni):



$$\text{B-uni} = \frac{\text{Minimum luminance of 9 points}}{\text{Maximum luminance of 9points}} \quad \text{(Note 5).}$$

Note 6: Definition of Response Time:

The Response Time is set initially by defining the “Rising Time (Tr)” and the “Falling Time (Tf)” respectively. Tr and Tf are defined as following figure.



Note 7: The color coordinates (x_w,y_w),(x_R,y_R),(x_G,y_G),and (x_B,y_B) are obtained with all pixels in the viewing field at white, red, green, and blue states, respectively.

9. PIN CONNECTIONS

9.1 TFT-LCD PIN CONNECTIONS

<table>
<tr><th>Pin No</th><th>Symbol</th><th>Description</th><th>Remark</th></tr>
<tr><td>1</td><td>VCI</td><td>A supply voltage to the analog circuit. Connect to an external power.</td><td></td></tr>
<tr><td>2</td><td>VCI</td><td>A supply voltage to the analog circuit. Connect to an external power.</td><td></td></tr>
<tr><td>3</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>4</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>5</td><td>IOVCC</td><td>A supply voltage to the digital circuit. Connect to an external power.</td><td></td></tr>
<tr><td>6</td><td>IOVCC</td><td>A supply voltage to the digital circuit. Connect to an external power.</td><td></td></tr>
<tr><td>7</td><td>IM2</td><td>Select the interface mode</td><td>Note1</td></tr>
<tr><td>8</td><td>IM1</td><td>Select the interface mode</td><td>Note1</td></tr>
<tr><td>9</td><td>IM0</td><td>Select the interface mode</td><td>Note1</td></tr>
<tr><td>10</td><td>RESX</td><td>The external reset input.
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td><td></td></tr>
<tr><td>11</td><td>DB17(D17)</td><td rowspan="18">A 18-bit parallel bi-directional data bus for MCU system
<table><tr><td>Interface Mode</td><td>Data Pin in Use</td></tr><tr><td>8080 16-bit MCU interface Mode</td><td>DB[15:0]</td></tr><tr><td>8080 18-bit MCU interface Mode</td><td>DB[17:0]</td></tr><tr><td>16-bit RGB Interface Mode</td><td>DB[15:0]</td></tr><tr><td>18-bit RGB Interface Mode</td><td>DB[17:0]</td></tr></table>Fix to GND level when not in use.</td><td></td></tr>
<tr><td>12</td><td>DB16(D16)</td><td></td></tr>
<tr><td>13</td><td>DB15(D15)</td><td></td></tr>
<tr><td>14</td><td>DB14(D14)</td><td></td></tr>
<tr><td>15</td><td>DB13(D13)</td><td></td></tr>
<tr><td>16</td><td>DB12(D12)</td><td></td></tr>
<tr><td>17</td><td>DB11(D11)</td><td></td></tr>
<tr><td>18</td><td>DB10(D10)</td><td></td></tr>
<tr><td>19</td><td>DB09(D9)</td><td></td></tr>
<tr><td>20</td><td>DB08(D8)</td><td></td></tr>
<tr><td>21</td><td>DB07(D7)</td><td></td></tr>
<tr><td>22</td><td>DB06(D6)</td><td></td></tr>
<tr><td>23</td><td>DB05(D5)</td><td></td></tr>
<tr><td>24</td><td>DB04(D4)</td><td></td></tr>
<tr><td>25</td><td>DB03(D3)</td><td></td></tr>
<tr><td>26</td><td>DB02(D2)</td><td></td></tr>
<tr><td>27</td><td>DB01(D1)</td><td></td></tr>
<tr><td>28</td><td>DB00(D0)</td><td></td></tr>
<tr><td>29</td><td>VSYNC</td><td>Frame synchronizing signal for RGB interface operation.
Fix to GND level when not in use.</td><td></td></tr>
<tr><td>30</td><td>HSYNC</td><td>Line synchronizing signal for RGB interface operation.
Fix to GND level when not in use.</td><td></td></tr>
<tr><td>31</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>32</td><td>DCLK</td><td>Dot clock signal for RGB interface operation.
Fix to IOVCC level when not in use.</td><td></td></tr>
<tr><td>33</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>34</td><td>ENABLE</td><td>Data enable signal for RGB interface operation.
Low : access enabled. High : access inhibited.
Fix to GND level when not in use.</td><td></td></tr>
</table>

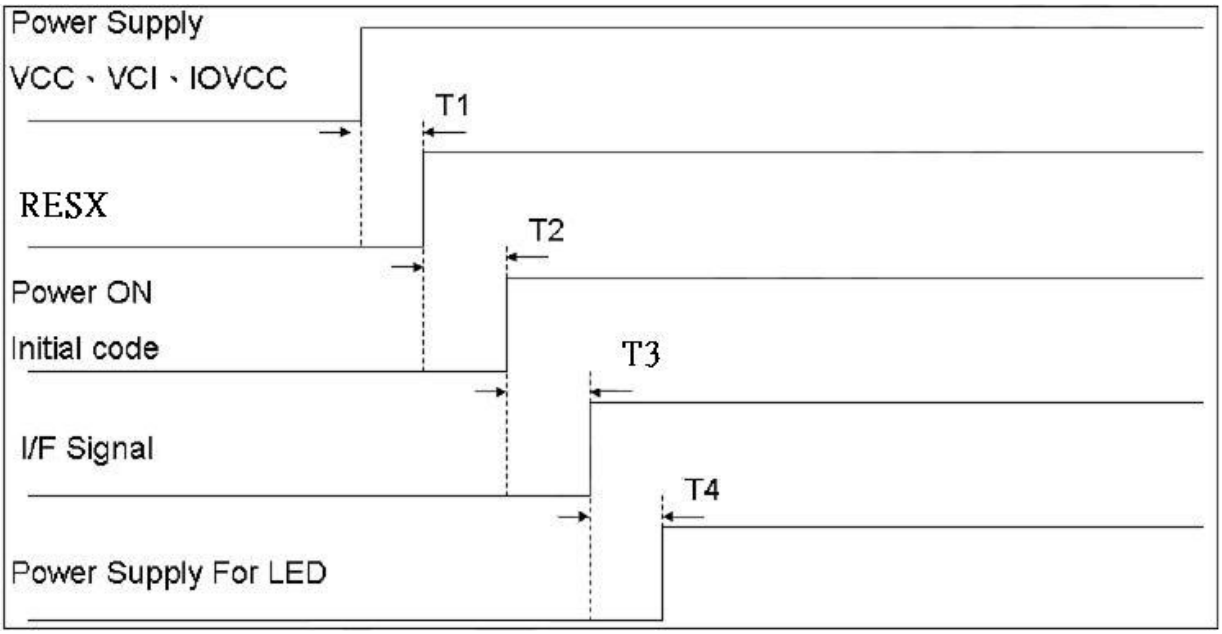
35	SDA	Serial data input / output. **Fix to IOVCC or GND level when not in use.**	
36	RDX	8080 system (RDX): Serves as a read signal and read data at the rising edge. **Fix to IOVCC or GND level when not in use.**	
37	CSX	A chip select signal. Low: the chip is selected and accessible High: the chip is not selected and not accessible **Fix to IOVCC or GND level when not in use.**	
38	DCX_SCL	8080 system (DCX): The signal for command or parameter select. Low: Command. High: Parameter. Serial interface (SCL): Serial clock input. **Fix to IOVCC or GND level when not in use.**	
39	WRX_DCX	8080 system (WRX): Serves as a write signal and writes data at the rising edge. **Fix to IOVCC or GND level when not in use.**	
40	VCC	A supply voltage to the digital circuit. Connect to an external power.	
41	VCC	A supply voltage to the digital circuit. Connect to an external power.	
42	GND	Ground	
43	GND	Ground	
44	LEDK	POWER SUPPLY FOR LED-	
45	LEDA	POWER SUPPLY FOR LED+	

Note1

IM2	IM1	IM0	Interface	Data Pin in Use
0	0	0	8080 18-bit MCU interface	DB[17:0]
0	1	0	8080 16-bit MCU interface	DB[15:0]
1	0	1	3-line SPI + parallel RGB interface	SDA + DB[17:0]

9.2 power ON/OFF sequence:

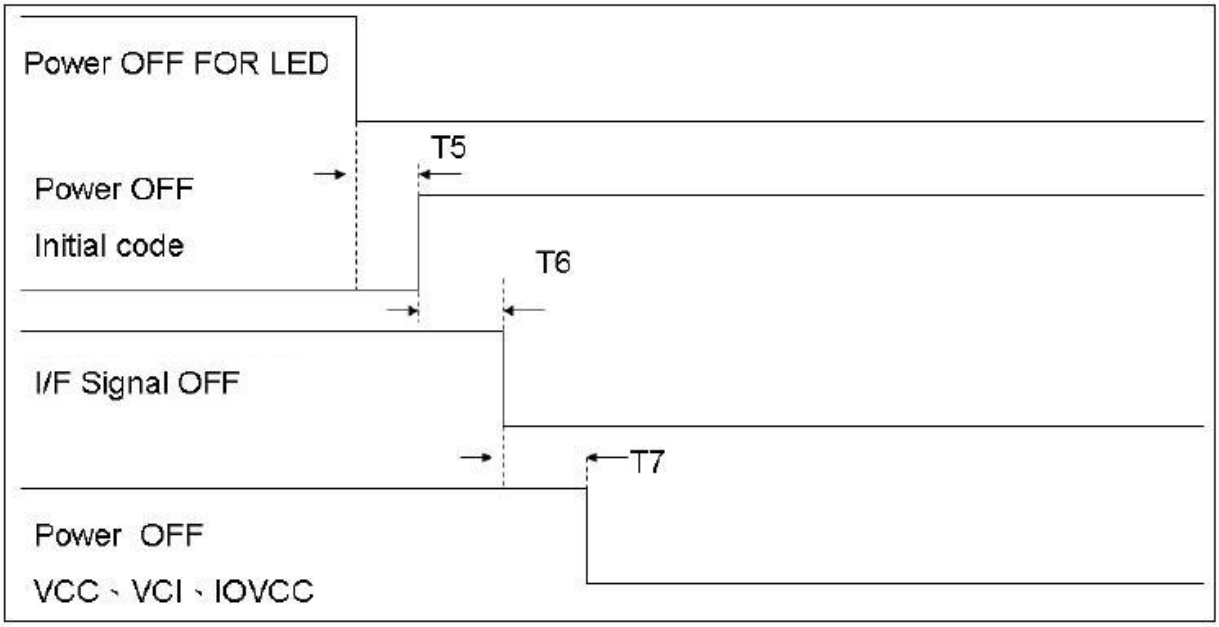
Power on:



10ms≦T1≦20ms ; 50ms≦T2≦100ms

100ms≦T3≦200ms ; 100ms≦T4≦200ms

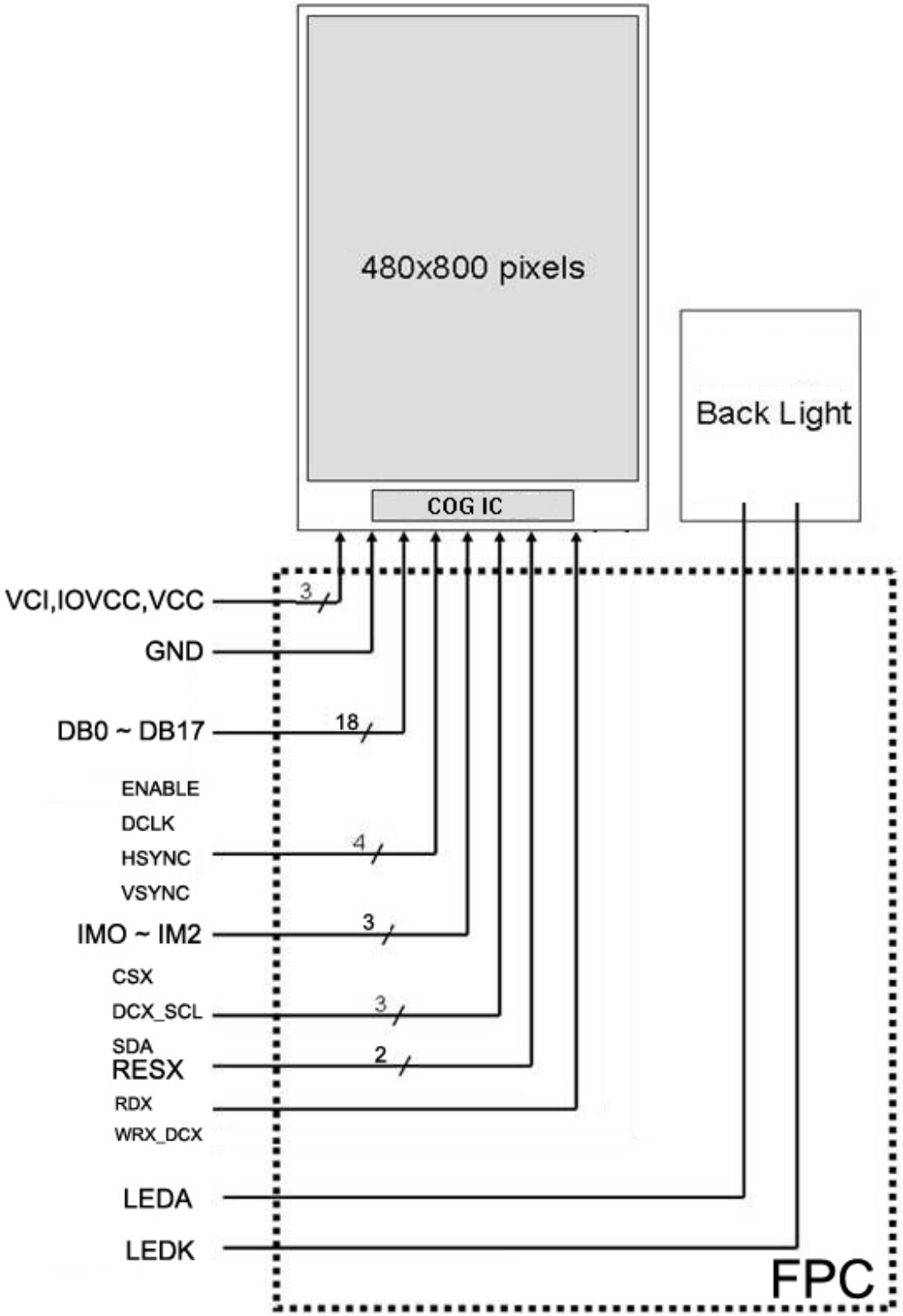
Power off:



50ms≦T5≦100ms ; 50ms≦T6≦100ms

100ms≦T7≦200ms

10. BLOCK DIAGRAM



11. QUALITY ASSURANCE

11.1 Test Condition

11.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 25 ± 5°C
Humidity : 65 ± 5%

11.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

11.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

11.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

11.1.5 Test Method

Reliability Test Item & Level		Test Level
No.	Test Item	
1	High Temperature Storage Test	T=80,240hrs
2	Low Temperature Storage Test	T=-30,240hrs
3	High Temperature Operation Test	T=70,240hrs
4	Low Temperature Operation Test	T=-20,240hrs
5	High Temperature and High Humidity (No operation)	T=60℃,90%RH,240hrs
6	Thermal Cycling Test (No operation)	-30℃ → +25℃ → +80℃, 100 Cycles 30 min 5 min 30 min
7	Vibration Test (No operation)	Frequency :10 ~ 55 H_Z Amplitude :1.5 mm Sweep time : 11 mins Test Period: 6 Cycles for each direction of X, Y, Z

11.2 Judgment standard

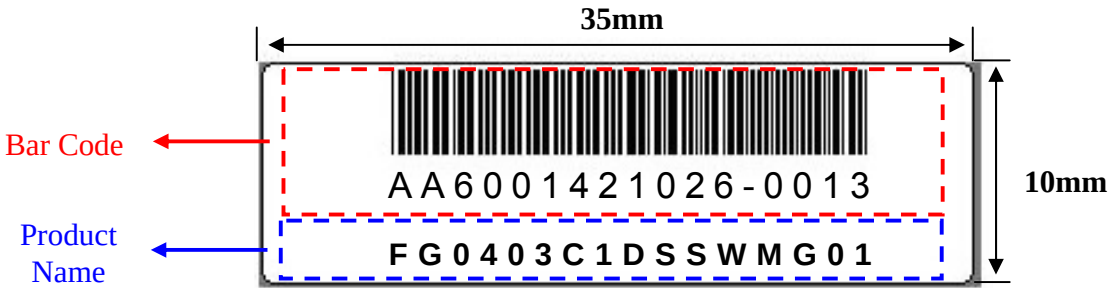
The Judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect. Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defect.

12. LCM PRODUCT LABEL DEFINE

Product Label style:

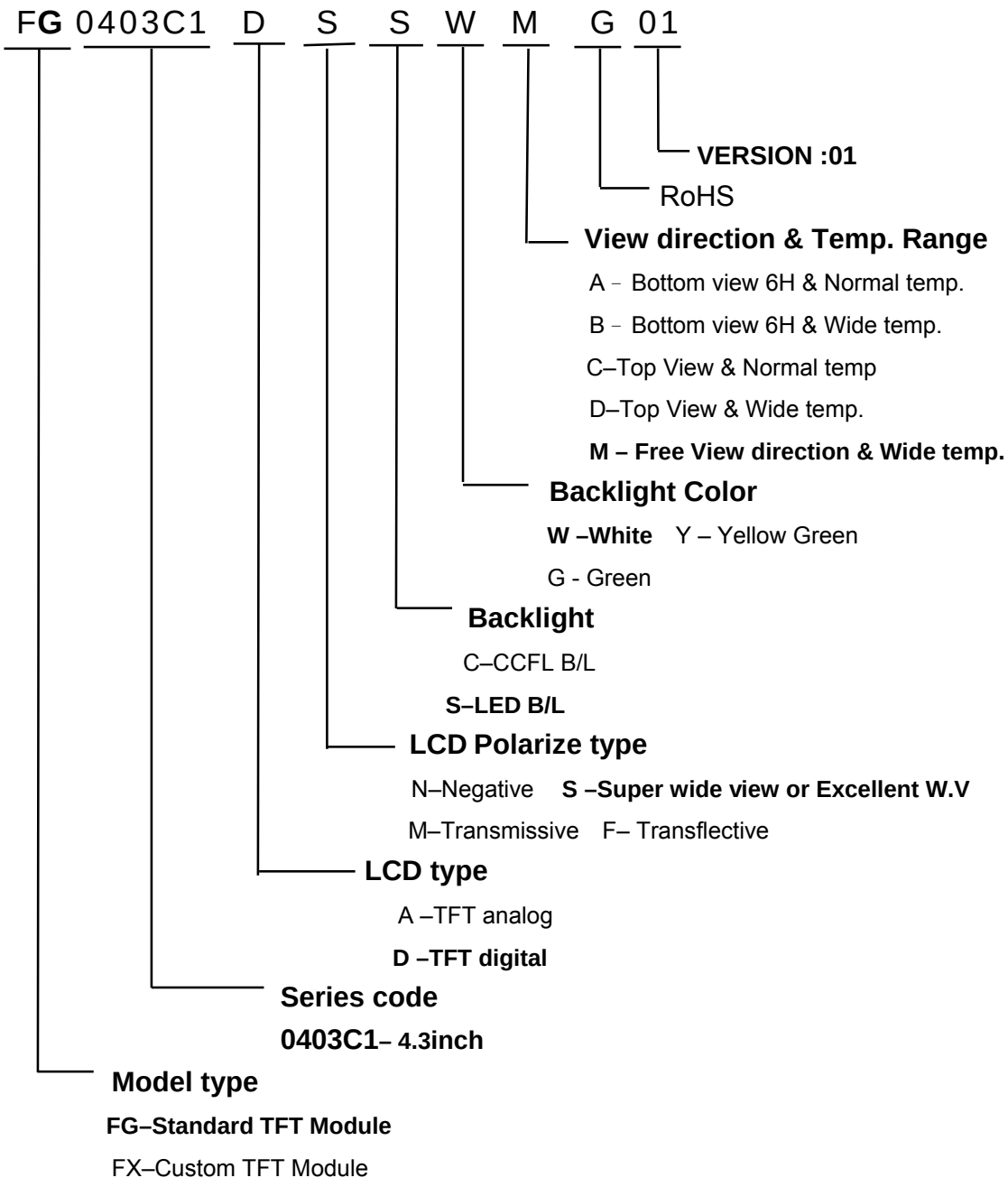


BarCode Define:

A A 6 0014 2 10 26-0013

- Serial number of the products
  Serial number starts from 0000
  Every work order is 10K at most
- Week of production
- Year of production
- Storage area
- Serial number of work order
  Serial number starts from 0000 each month
- Month of work order
- Year of work order
- The first 3 numbers of work order

Product Name Define:

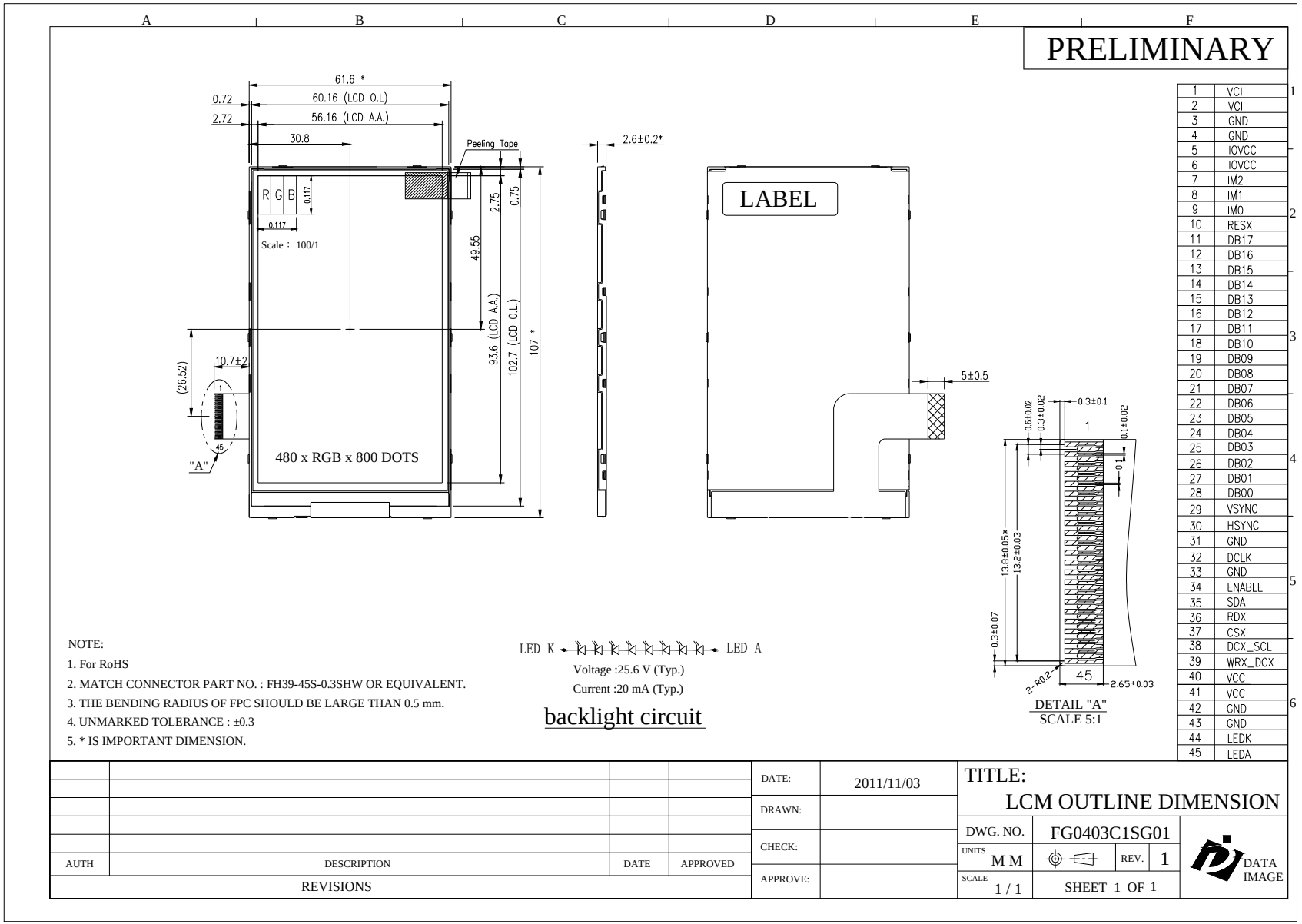


13. PRECAUTIONS IN USE LCM

1. ASSEMBLY PRECAUTIONS
   (1) You must mount a module using holes arranged in four corners or four sides.
   (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
   (3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
   (4) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
   (5) Do not open the case because inside circuits do not have sufficient strength.
   (6) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
   (7) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
   (8) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.
2. OPERATING PRECAUTIONS
   (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
   (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification
   (3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
   (4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
   (5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
   (6) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
3. ELECTROSTATIC DISCHARGE CONTROL
   (1) The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such the copper leads on the PCB and the interface terminals with any parts of the human body.
   (2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
   (3) Only properly grounded soldering irons should be used.
   (4) If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.
   (5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended
   (6) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.
4. STORAGE PRECAUTIONS
   (1) When you store LCDs for a long time, it is recommended to keep the temperature between 0°C-40°C without the exposure of sunlight and to keep the humidity less than 90%RH.
   (2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C 90%RH
   (3) Please do not leave the LCDs in the environment of low temperature; below -20°C.
5. OTHERS
   (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays
   (2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
   (3) For the packaging box, please pay attention to the followings:
      a. Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
      b. Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
      c. Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)
6. LIMITED WARRANTY

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events.

14. OUTLINE DRAWING



15. PACKAGE INFORMATION

TBD