DATA IMAGE CORPORATION

TFT Module Specification

Preliminary

ITEM NO.: FG0204K0DNSWBG01

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Customer Companies	R&D Dept.	Q.C. Dept.	Eng. Dept.	Prod. Dept.
	ALEX	JOE	GARY	KEN
Approved by	Version:	Issued Date:	Sheet Code:	Total Pages:
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2. RECORD OF REVISION

Rev	Date	Item	Page	Comment
1	31/MAR/14’			Initial preliminary

3. GENERAL SPECIFICATIONS

Parameter		Specifications	Unit
Screen Size		2.4 (diagonal)	inch
Surface Treatment		Anti-Glare	
Display Format		480 x 234	dots
Active Area		48 (W) x 35.685 (H)	mm
Dot Pitch		0.1(W) x 0.1525 (H)	mm
Pixel Configuration		R.G.B Delta	
Outline Dimension		55.2 (W) x 47.55 (H) x 2.81(T)	mm
Weight		12	g
View Angle direction (Gray inversion)		6 o'clock	
Temperature Range	Operation	-20~70	℃
	Storage	-30~80	℃

4. ABSOLUTE MAXIMUM RATINGS

(GND=PGND=0V)

Parameter	Symbol	MIN.	MAX.	Unit
Power supply voltage (1)	VCC	-0.3	+7.0	V
Power supply voltage (2)	AVDD	-0.3	+7.0	V
Power supply voltage (3)	PVDD	-0.3	+7.0	V
Input voltage	Vin	-0.3	VCC+0.3	V

Note:
All of the voltages listed above are with respective to VSS=0V.
Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

5. ELECTRICAL CHARACTERISTICS

a. Typical operating conditions

(GND=PGND=0V) Ta=25℃

Parameter		Symbol	MIN.	TYP	MAX.	Unit	Remark
Power voltage		VCC	2.7	3.3	3.6	V	
		PVDD,AVDD	3.0	3.3	3.6	V	
		VCOM AC	5.25	5.75	6.25	V	
		VCOM DC	0.7	0.9	1.1		
Input Signal voltage	H Level	VIH	0.7*VCC		VCC	V	
	L Level	VIL	GND		0.3*VCC	V	
Analog stand by current		Ist	-	--	10	μA	PVDD;STB="O" all factions are shut down

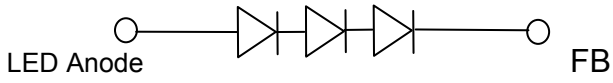
b. Current consumption

(GND=PGND=0V) Ta=25℃

Parameter	Symbol	Condition	MIN.	TYP	MAX.	Unit
	I_{VCC}	Vcc=3.3V		1.5	2.0	mA
	I_{PVDD}	PVDD=3.3V		13.5	16	mA
	I_{AVDD}	AVDD=3.3V		1.2	2.0	mA

C. Backlight Driving for Power Consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V_L	--	9.45	11.7	V	I_L=20 mA, Ta= 25 °C
LED current	I_L	--	20	--	mA	Ta= 25 °C



5.1 AC Characteristics

a. Timing conditions

Parameter	Symbol	MIN.	TYP	MAX.	Unit
Delay between Hsync and DCLK	Thc			1	DCLK
Hysnc width	Twh	1	32		DCLK
Hysnc period	Th	60	63.5	67	μs
Vsync setup time	Tvst	12			ns
Vsync hold time	Tvhd	12			ns
Hsync setup time	Thst	12			ns
Hsync hold time	Thhd	12			ns
Data set-up time	Tdsu	12			ns
Data hold time	Tdhd	12	-		ns
DE set-up time	Tesu	12	-		ns
Vsync width	Twv	2	4	6	Th
Vsync period NTSC	Tv		262.5		Th
Vsync period PAL	Tv	-	312.5	--	Th
Hsync to Vsync time for ODD field	THV O	-4		+4	DCLK
Hsync to Vsync time for EVEN field	THV E	-	0.5		Th
S/D output stable time	Tst			30	μs
G/D output stable time	Tgst		1		μs

b. Operating mode dependent AC characteristic

Serial RGB Mode, SEL [2…0]=[000, 001]

Parameter	Symbol	MIN.	TYP	MAX.	Unit
DCLK frequency	Fclk		9.7		Mhz
DCLK period	Tcph		103		ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso		56		DCLK
Delay from Hsync to Gate output	Thgo		45		DCLK
Delay from Hsync to Gate output off	Thgz		19		DCLK
Delay from Hsync to FRP	Thf		56		DCLK
Delay from Hsync to 1st data input **(for SYNC mode)**	Ths	83	99	114	DCLK

c. Operating mode dependent AC characteristic

YUV Mode, SEL [2…0]=[011~110]

Parameter	Symbol	MIN.	TYP	MAX.	Unit
DCLK frequency	Fclk		24.54/27		Mhz
DCLK period	Tcph		40.7/37		ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso		143		DCLK
Delay from Hsync to Gate output	Thgo		113		DCLK
Delay from Hsync to Gate output off	Thgz		48		DCLK
Delay from Hsync to FRP	Thf		143		DCLK
Delay from Hsync to 1,st data input (for TS601=0)	Ths	233	249	264	DCLK

d. Operating mode dependent AC characteristic

CCIR656 Mode (720 x 480 pixel), SEL [2…0]=[111]

Parameter	Symbol	MIN.	TYP	MAX.	Unit
DCLK frequency	Fclk	-	27	-	Mhz
DCLK period	Tcph		37		ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from CCIR_H to Source output	Thso		171		DCLK
Delay from CCIR_H to Gate output	Thgo		141		DCLK
Delay from CCIR_H to Gate output off	Thgz		76		DCLK
Delay from CCIR_H to FRP	Thf		171		DCLK

e. Operating mode dependent AC characteristic

CCIR656 Mode (640 x 480 pixel), SEL [2…0]=[010]

Parameter	Symbol	MIN.	TYP	MAX.	Unit
DCLK frequency	Fclk	-	24.54	-	Mhz
DCLK period	Tcph		40.7		ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from CCIR_H to Source output	Thso		171		DCLK
Delay from CCIR_H to Gate output	Thgo		141		DCLK
Delay from CCIR_H to Gate output off	Thgz		76		DCLK
Delay from CCIR_H to FRP	Thf		171		DCLK

5.2 Waveform:

5.2.1 Timing format: Serial communication timing:

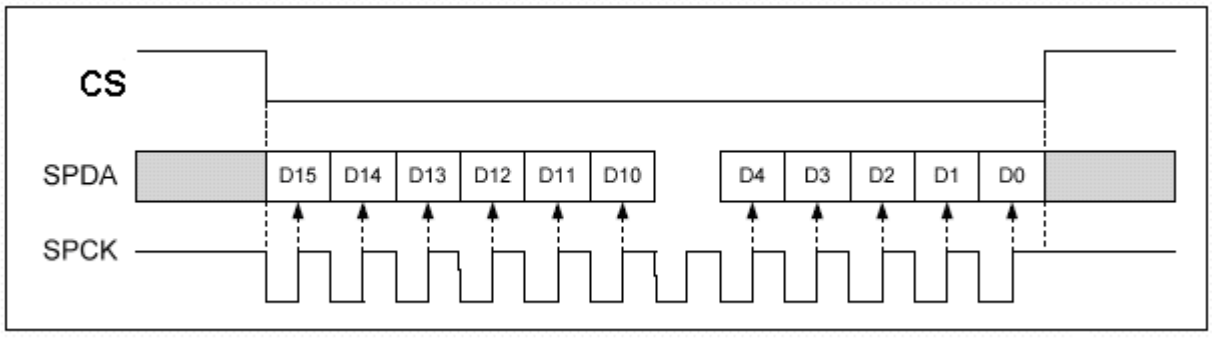
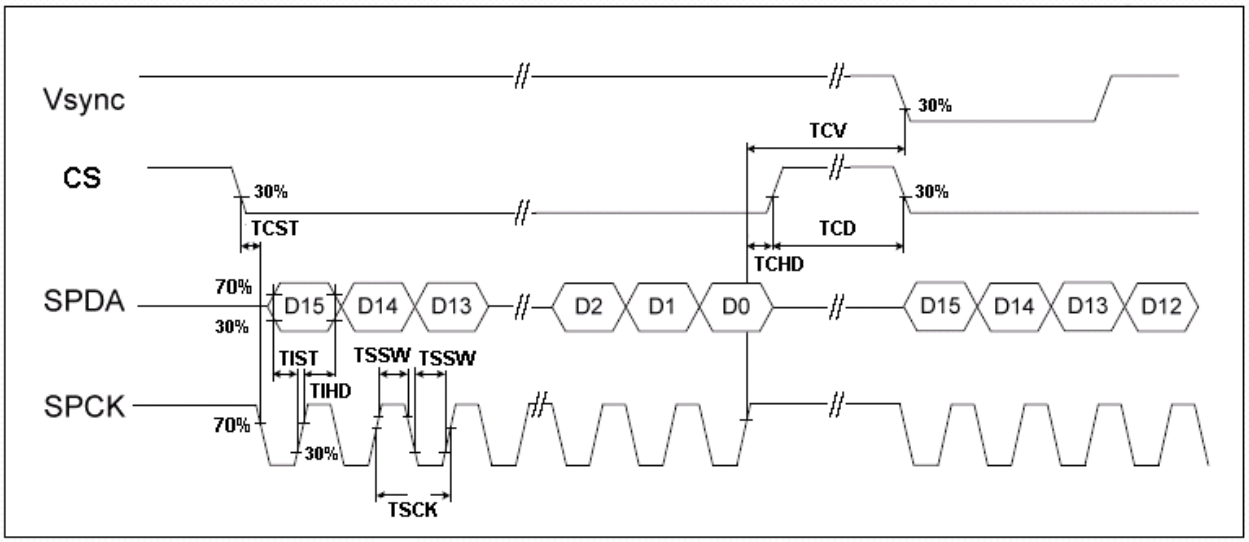


Figure 5.2 SPI Timing Diagram



Note: All the SPI register settings will active at the falling edge of the VSYNC except GRB_STB and SEL[2:0] bits

Figure6. 2.1 SPI Timing Diagram V.S. Vsync

5.2.2 Serial communication

Parameter	Symbol	MIN.	TYP	MAX.	Unit
Serial clock period	Tsck	320	-	-	ns
Serial clock duty cycle	Tscw	40	50	60	%
Serial clock width	Tssw	120	-	-	ns
Serial data setup time	Tist	120	-	-	ns
Serial data hold time	Tihd	120	-	-	ns
SPENB setup time	Tcst	120	-	-	ns
SPENB data hold time	Tchd	120	-	-	ns
Chip select distinguish	Tcd	1	-	-	µs
Delay between SPCK and Vsync	Tcv	1	-	-	µs

Note: The first valid data line on panel is G1=Tstv+1=14(Active area is 240 channels).

5.3 Clock and Data Input Timing Diagram

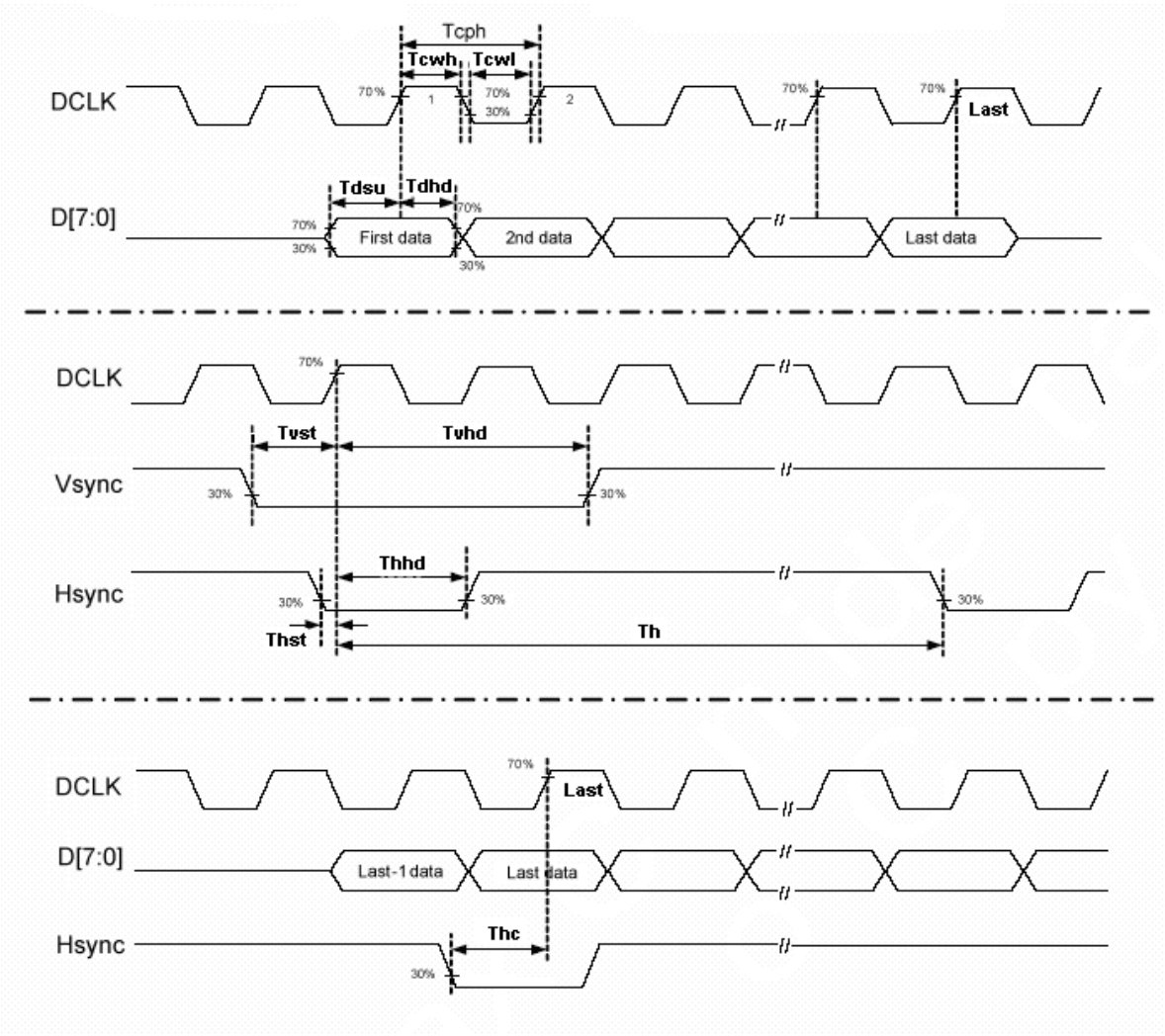


Figure6.3 Clock and Data Input Timing Diagram

5.4 Source Driver Output Timing Chart (IC internal timing, for user reference)

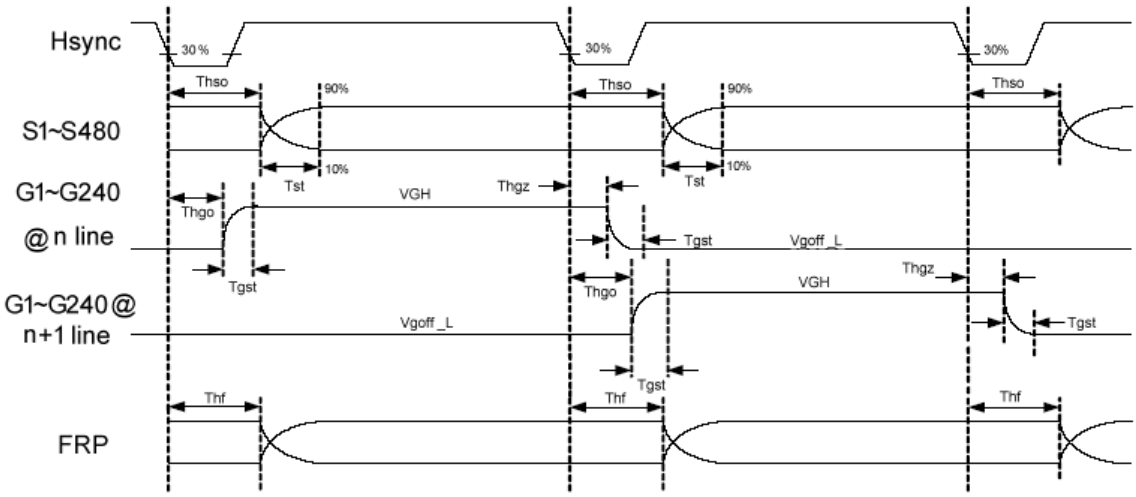


Figure 6.4 Source Driver and VCOM (FRP) Output Timing Chart

5.5 Input Data Format Timing

5.5.1 Serial RGB Data Format

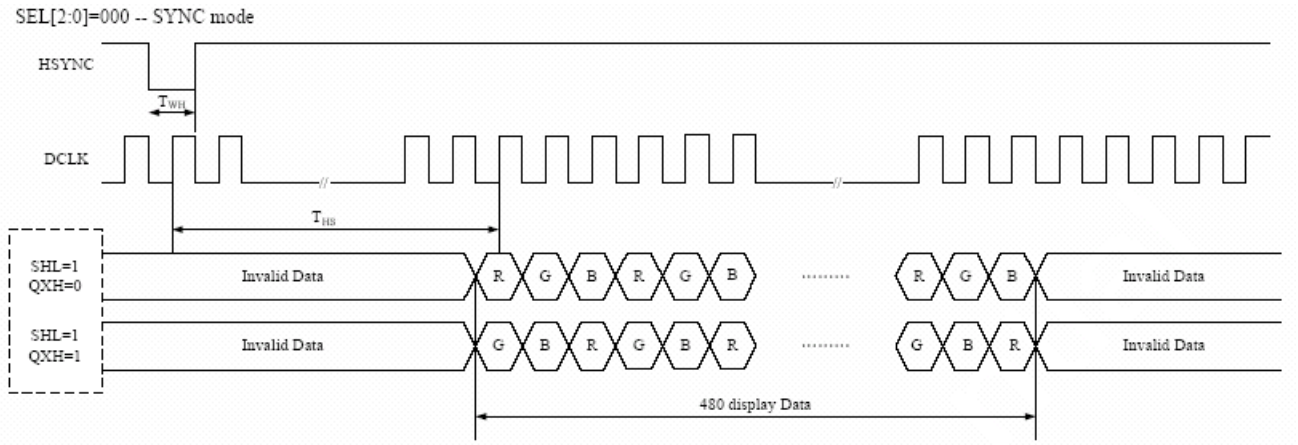


Figure 6.5.1 Serial RGB Data Format

5.5.2 YUV mode Data Format

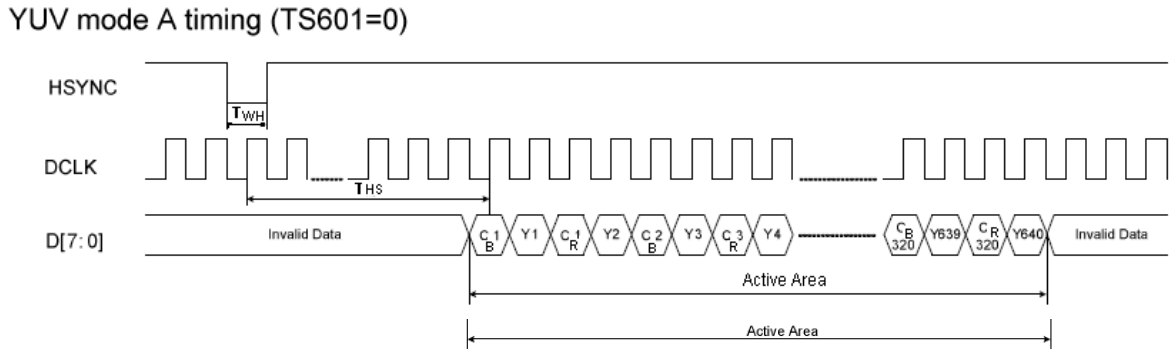


Figure 6.5.2 YUV Mode Data Format

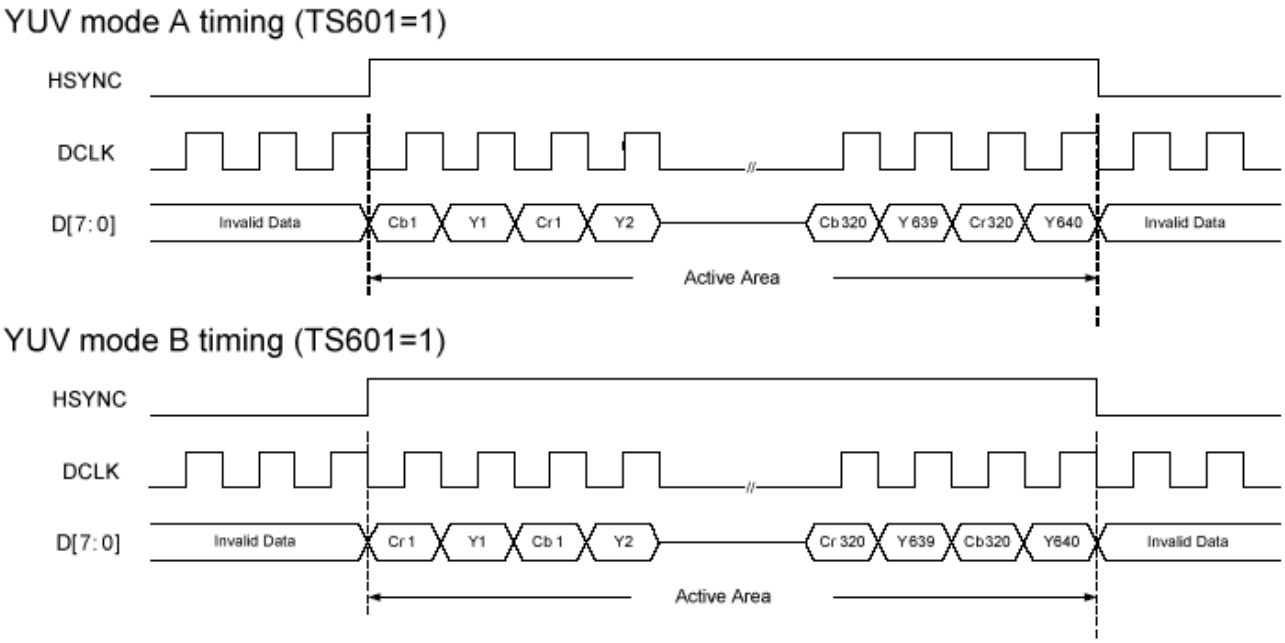


Figure 5.5.2.1 YUV Mode Data Format, TS601=1, HSDPOL=0

Input format	DCLK Freq (MHz)	Display Data	Active Area (DCLK)
YUV mode	24.54	640	1280
	27	720	1440

5.5.3 CCIR656 Data Format

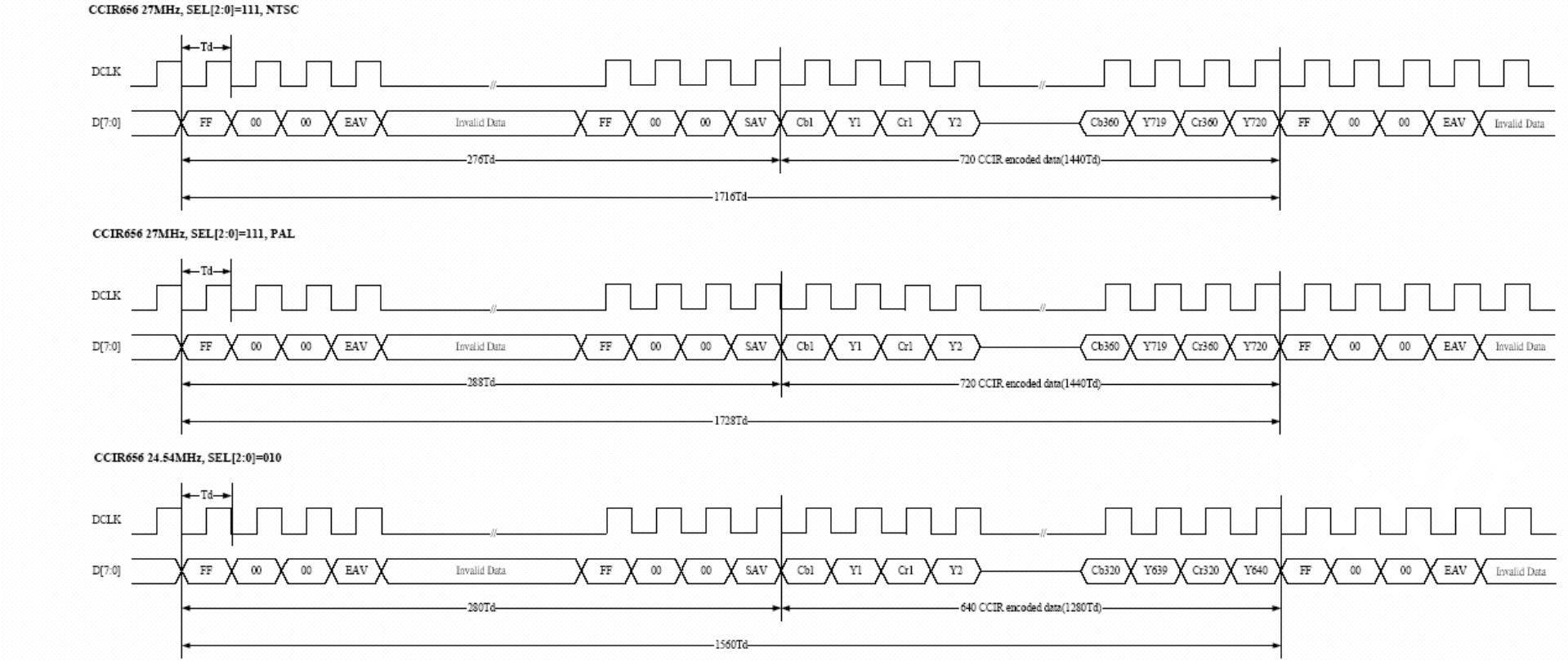


Figure 5.5.3 CCIR656 Data Format

5.6 Power ON/OFF sequence

Specially take care that the large current may cause a permanent damage to the IC when voltage is applied to the charge pump power supply in the condition that the logic power supply is floating.
Please refer to the following timing and command setting, concerning the power supply ON and the power supply OFF.

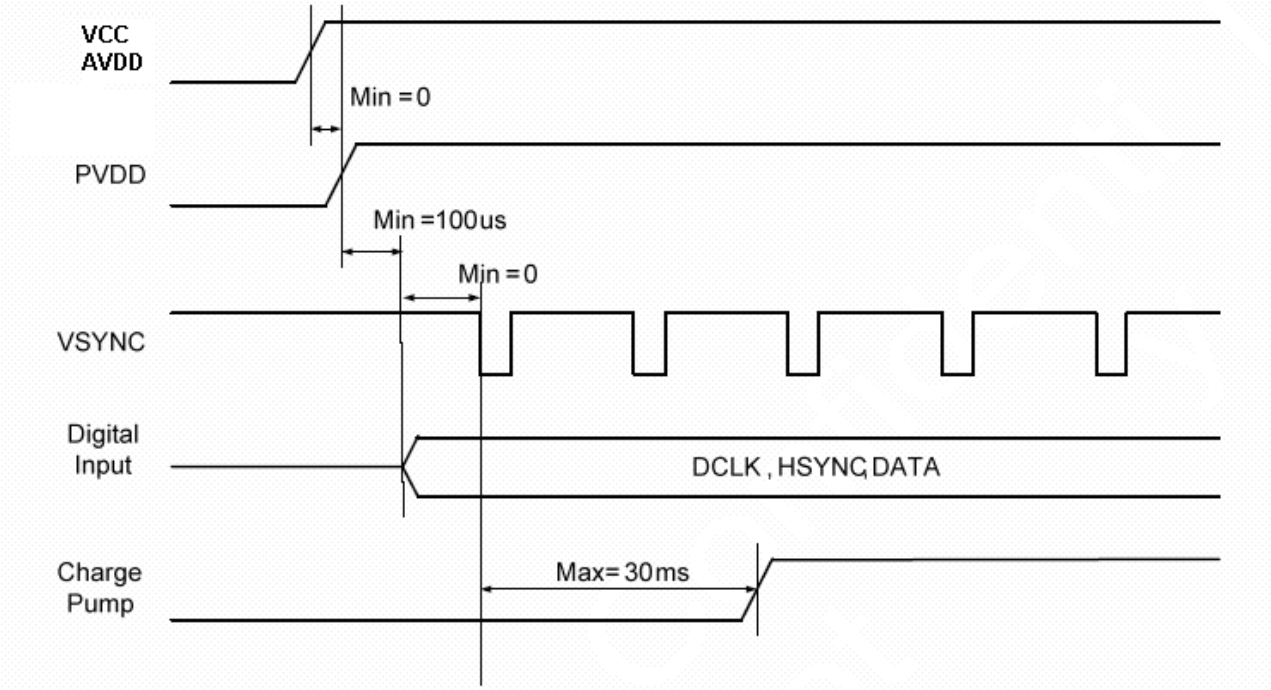


Figure 6.6 Power on sequence timing diagram

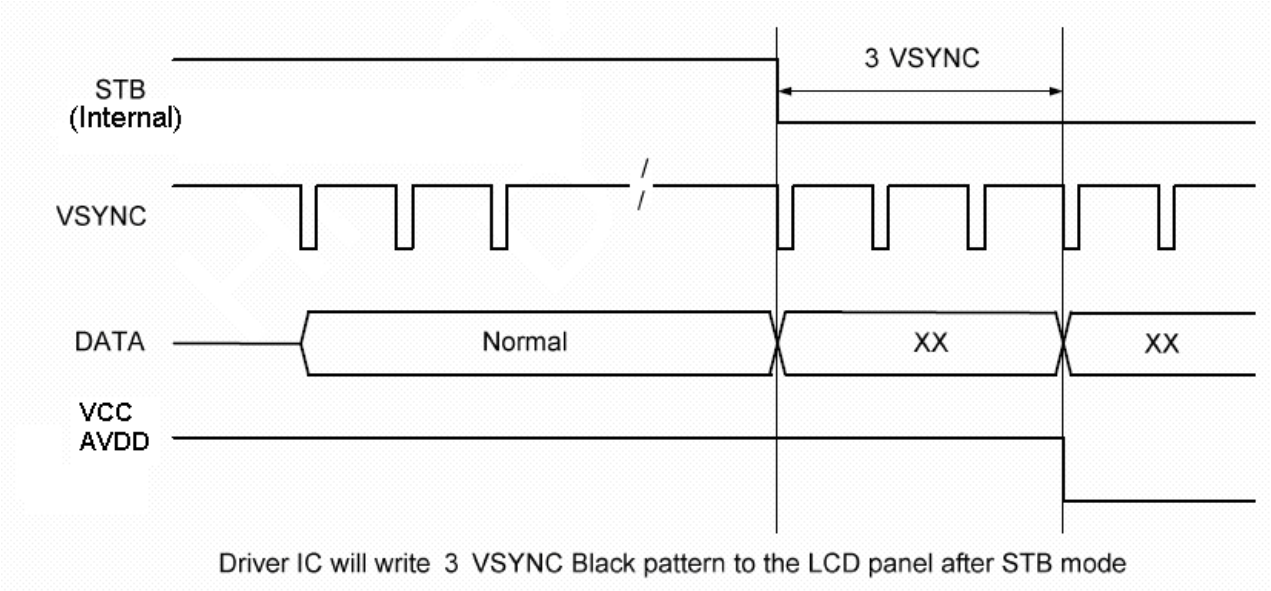
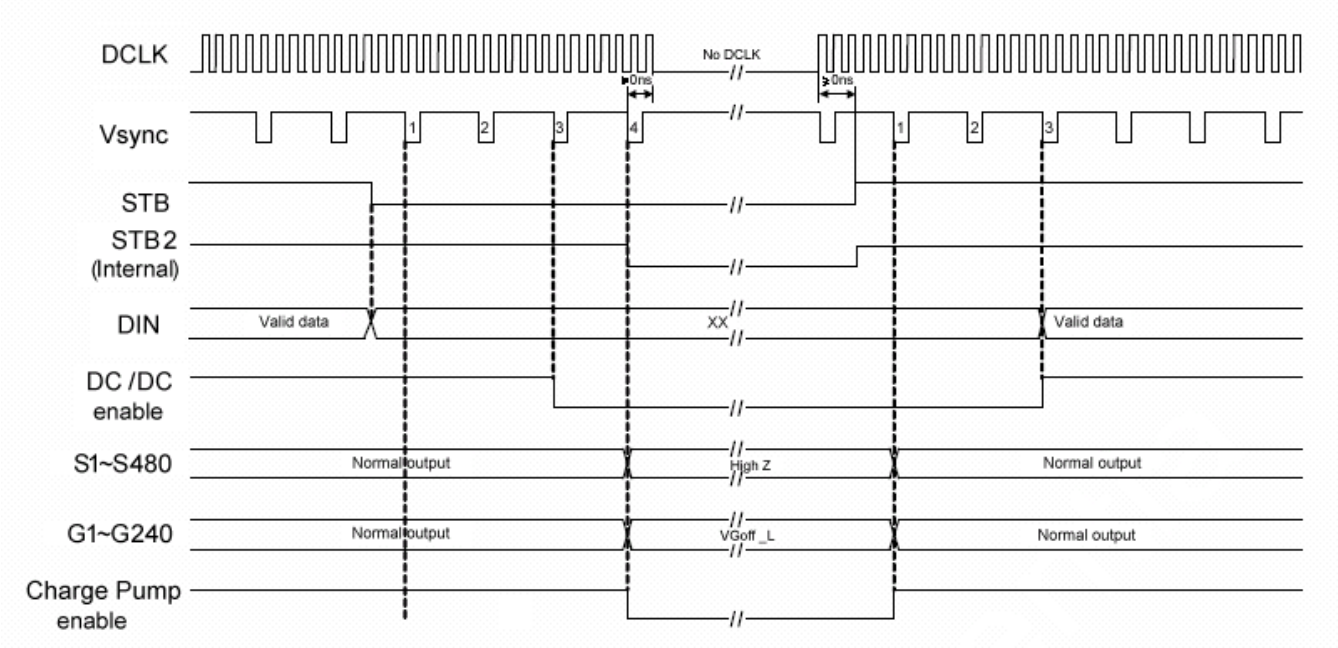


Figure 6.6.1 Power off sequence timing diagram



During No CLK, Hsync and Vsync can be stopped. But in all other cases Hsync and Vsync must be active

Figure 5.6.2 Enter and exit stand-by mode timing diagram

6. REGISTER DESCRIPTION

Register	Function Description
R00	System Setting Register
R01	Timing Control Setting Register
R02	Driver Setting Register
R03	Data format Setting Register
R04	Source Delay Setting Register
R05	Vertical Delay Setting Register
R06	Voltage Level Setting Register
R07	Internal Setting Register

Table 6.1 Function Description

6.1 Function Control Register

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R00	0	0	0	0									GRB	STB	SHDB	SHCB
R01	0	0	1	0							SWD2	SWD1	SWD0	DITB		D/S
R02	0	1	0	0									FPOL		UD	SHL
R03	0	1	1	0								PALM	PAL	SEL2	SEL1	SEL0
R04	1	0	0	0								DDL4	DDL3	DDL 2	DDL1	DDL0
R05	1	0	1	0									HDL3	HDL2	HDL1	HDL0
R06	1	1	0	0					VDV1	VDV0	LPC1	LPC0		VSCL2	VSCL1	VSCL0
R07	1	1	1	0									DCKS1	DCKS0		

Note 1：D12 must be low。

Note 2：All the SPI register settings will active at the falling edge of the VSYNC except GRB、STB and SEL[2:0] bits。

6.2 System Setting Register (R00h), default = 0Eh

	D15	D14	D13	D12	D11	D10	D9	D8	*D7*	*D6*	*D5*	*D4*	**D3**	**D2**	**D1**	**D0**
R00	0	0	0	0									**GRB**	**STB**	**SHDB**	**SHCB**
	0	0	0	0									**1**	**1**	**0**	**1**

GRB	**Global Reset**
L	The Controller is resets, the Charge Pump and DC/DC is off.
H	Normal operation; Default setting.

STB	**Stand By Mode**
L	TCON, SD, Charge Pump and DC-DC are off. All outputs are High-Z.
H	Normal operation; Default setting.

SHDB	**DC-DC converter shutdown signal**
L	The DC-DC is off. Default Setting. (DRV output pin is “LOW”
H	The DC-DC is on. (DRV output pin is working)

Note: The function disable, the DRV output be VSS.

SHCB	**Charge Pump shutdown signal**
L	The Charge Pump for VGH VGL VCAC are off
H	The Charge Pump is on; Default setting.

6.3 Color dot arrangement Setting Register (R01h), default = 01h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R01	0	0	1	0							SWD2	SWD1	SWD0	DITB		D/S
	0	0	1	0							0	0	0	0		1

SWD[2:0] Control and switch the relationship between the R, G, B and outputs. (Default = 000 for this color dot fixed panel, don't need to change it)

DITB	Dithering setting
L	Dithering on 8-bit resolution. Default Setting.
H	Dithering off. 6-bit resolution (the last 2-bits truncated).

D/S	Data/Stripe mode setting
L	Stripe mode
H	Delta Mode. Default setting

6.4 Driver Setting Register (R02h), default = 03h

	D15	D14	D13	D12	D11	D10	D9	D8	*D7*	*D6*	*D5*	*D4*	**D3**	**D2**	**D1**	**D0**
R02	0	1	0	0									**FPOL**		**UD**	**SHL**
	0	1	0	0									**0**		**1**	**1**

FPOL	Control the inversion of FRP depending on the polarity of the Gamma Correction
L	FRP in phase with the polarity of the gamma correction.
H	FRP inverted with respect to the polarity of the gamma correction. Default setting.

UD	UP/DOWN Scan Control of Gate Driver
L	Scan up. G240->G239->…..->G2->G1.
H	Scan down. G1->G2->…..->G239->G240. Default Setting.

SHL	Left/Right Selection
L	Shift left. S480->S479->……->S2->S1.
H	Shift right. S1->S2->……->S479->S480. Default Setting.

6.5 Data format Setting Register (R03h), default = 00h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R03	0	1	1	0								**PALM**	**PAL**	**SEL2**	**SEL1**	**SEL0**
	0	1	1	0								**0**	**0**	**0**	**0**	**0**

PALM	**PAL Selection Signal (only available when PAL=H)**
L	Input data format is PAL 1/6,8(280 active line). Default Setting.
H	Input data format is PAL 1/6(288 active line).

PAL	**NTSC/PAL Selection Signal**
L	Input data format is NTSC. Default Setting.
H	Input data format is PAL.

Select Input Data Format, Default Setting=000.

SEL2	**SEL1**	**SEL0**	**Format**	**Operating Frequency**
0	**0**	**0**	**Serial-RGB data format (HV mode)**	**9.7MHz**
0	0	1	Serial-RGB data format (DE mode)	9.7MHz
0	1	0	CCIR 656 data format(640RGB)	24.54MHz
0	1	1	YUV mode A data format	24.54MHz
1	0	0	YUV mode A data format	27MHz
1	0	1	YUV mode B data format	24.54MHz
1	1	0	YUV mode B data format	27MHz
1	1	1	CCIR 656 data format(720RGB)	27MHz

6.6 Source Delay Setting Register (R04h), default = 00h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R04	1	0	0	0								**DDL4**	**DDL3**	**DDL2**	**DDL 1**	**DDL 0**
	1	0	0	0								**0**	**0**	**0**	**0**	**0**

Select the data delay timing, Default Setting=00000.

DDL4	DDL3	DDL2	DDL1	DDL0	Delay	Unit
0	**0**	**0**	**0**	**0**	**0**	DCLK Period
0	0	0	0	1	1	
0	0	0	1	0	2	
0	0	0	1	1	3	
0	0	1	0	0	4	
0	0	1	0	1	5	
0	0	1	1	0	6	
0	0	1	1	1	7	
0	1	0	0	0	8	
0	1	0	0	1	9	
0	1	0	1	0	10	
0	1	0	1	1	11	
0	1	1	0	0	12	
0	1	1	0	1	13	
0	1	1	1	0	14	
0	1	1	1	1	15	
1	0	0	0	0	-1	
1	0	0	0	1	-2	
1	0	0	1	0	-3	
1	0	0	1	1	-4	
1	0	1	0	0	-5	
1	0	1	0	1	-6	
1	0	1	1	0	-7	
1	0	1	1	1	-8	
1	1	0	0	0	-9	
1	1	0	0	1	-10	
1	1	0	1	0	-11	
1	1	0	1	1	-12	
1	1	1	0	0	-13	
1	1	1	0	1	-14	
1	1	1	1	0	-15	
1	1	1	1	1	-16	

6.7 Vertical Delay Setting Register (R05h), default = 00h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R05	1	0	1	0									**HDL3**	**HDL2**	**HDL1**	**HDL0**
	1	0	1	0									**0**	**0**	**0**	**0**

Select the first active line delay timing, Default Setting=0000.

HDL3	HDL2	HDL1	HDL0	Delay	Unit
0	**0**	**0**	**0**	**0**	HSYNC. Period.
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	
1	0	0	1	-1	
1	0	1	0	-2	
1	0	1	1	-3	
1	1	0	0	-4	
1	1	0	1	-5	
1	1	1	0	-6	
1	1	1	1	-7	

6.8 Voltage Level Setting Register (R06h), default = 06h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R06	1	1	0	0					**VDV1**	**VDV0**	**LPC1**	**LPC0**		**VSCL2**	**VSCL1**	**VSCL0**
	1	1	0	0					**0**	**0**	**0**	**0**		**1**	**1**	**0**

Voltage level control, default setting=00

VD1	VD0	VDDA
0	0	5V
0	1	4.8V
1	0	4.6V
1	1	4.4V

Low power control, default setting=00

LPC1	LPC0	Output driving time	Unit
0	1	30	us
0	1	20	
1	0	63.5	
1	0	40	

VCOM amplitude control, default setting=110.

VSCL2	VSCL1	VSCL0	VCAC Level	Unit
0	1	0	4.75	V
0	1	1	5.0	
1	0	0	5.25	
1	0	1	5.5	

1	**1**	**0**	**5.75**
1	1	1	6.0
0	0	0	6.25
0	0	1	6.375

6.9 Internal Setting Register (R07h), default = 03h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R07	1	1	1	0									DCKS1	DCKS0		
	1	1	1	0									**0**	**0**		

DCKS1	DCKS0	CKC1	CKC2	Unit
0	1	150	37.5	KHz
0	1	50	12.5	
1	0	100	25	
1	1	200	50	

7. OPTICAL CHARACTERISTICS

Ta = 25°C

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	ϕ	CR≥10	±45	±50		deg	Note 2
	Vertical	θ (to 12 o'clock)		45	50		deg	
		θ (to 6 o'clock)		35	40		deg	
Contrast Ratio		CR		150	--			Note 1
Response time	Rise	Tr	θ=0° ϕ=0°		15	30	ms	Note 4
	Fall	Tf			35	50	ms	
Uniformity		U			70		%	Note 5
Brightness				200	250	--	cd/m^2	Note 2
Chromaticity	White	x	θ=0°	0.25	0.300	0.35		Note 2
		y		0.28	0.330	0.38		

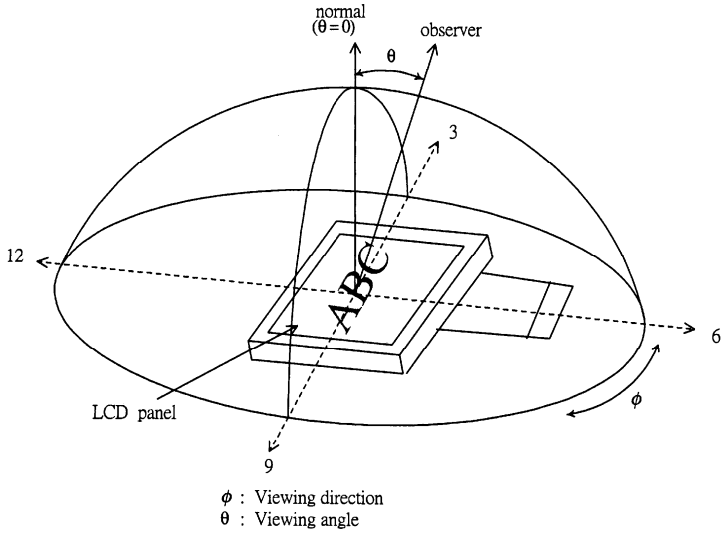
Note 1：CR = $\frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

Contrast Ratio is measured in optimum common electrode voltage.
The test configurations of contrast ratio see section9-2 .

Note 2 :1.Topcon BM-7(fast) luminance meter 1.0° field of view is used in the testing (after 2 minutes operation).

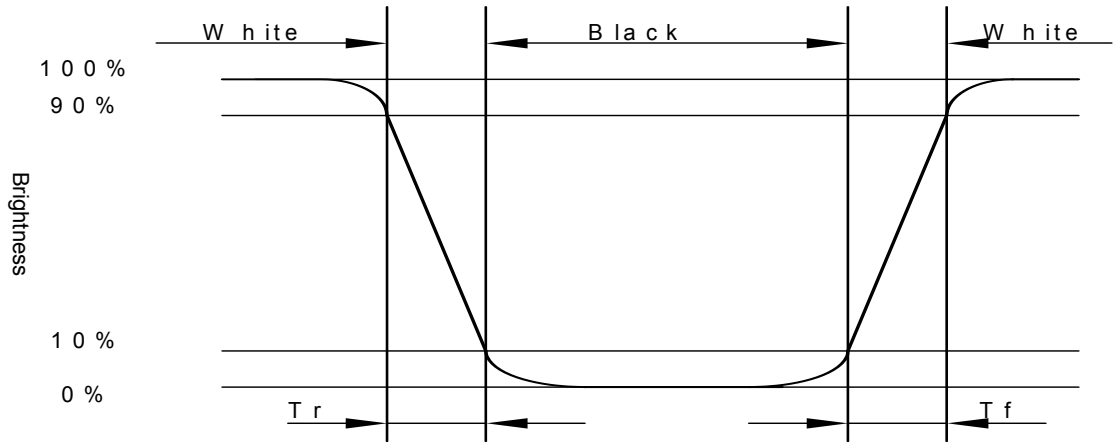
2. LED current =20mA.

Note 3 : The definitions of viewing angles diagrams:

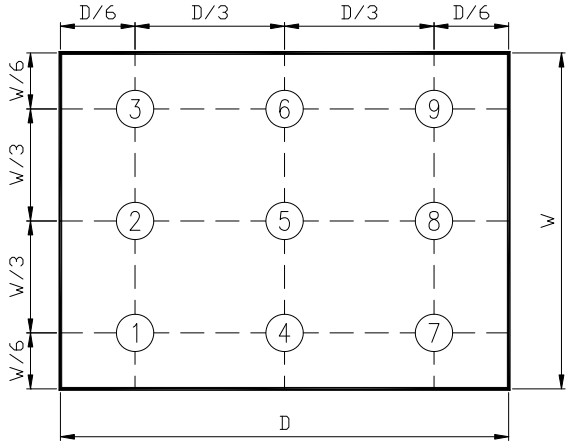


ϕ : Viewing direction
θ : Viewing angle

Note 4: The definition of response time:

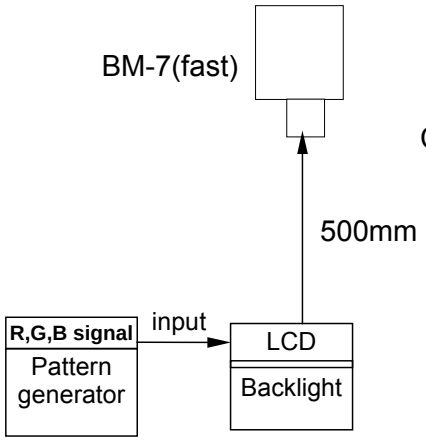


Note 5: Definition of Brightness Uniformity (Buni):



$$\text{Buni} = \frac{\text{Minimum luminance of 9 points}}{\text{Maximum luminance of 9points}}$$

Testing configuration

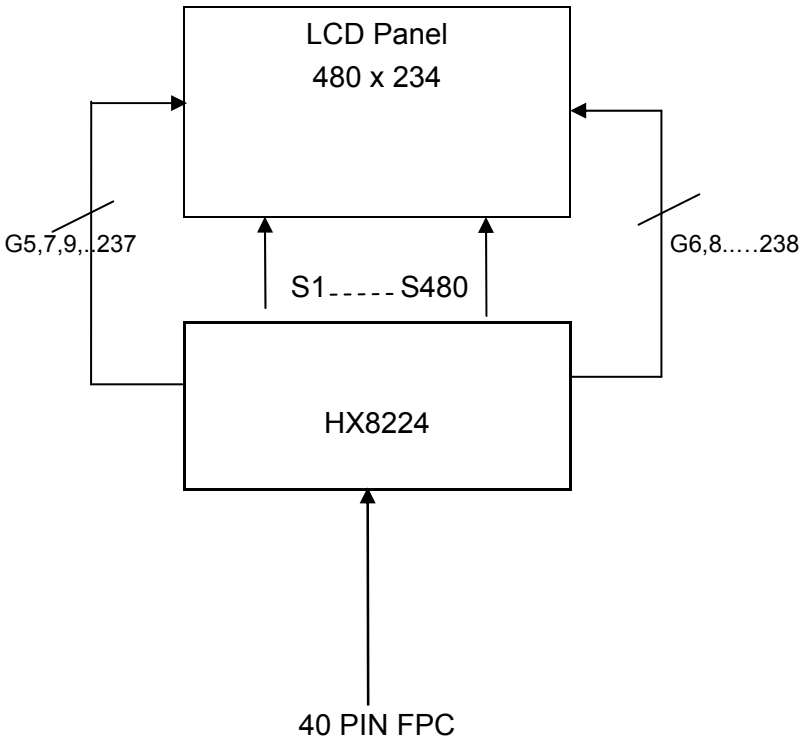


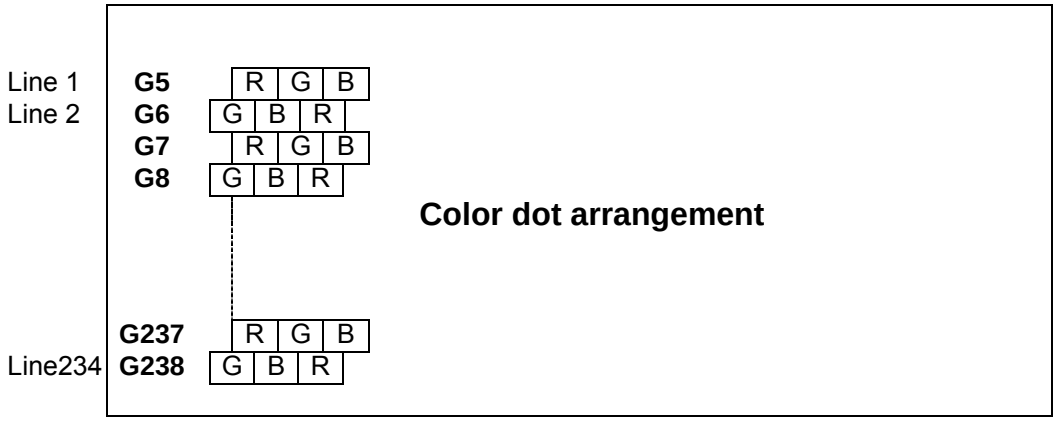
Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

8. PIN CONNECTIONS

Pin no	Symbol	I/O	Description
1	VCOM	I	Common electrode driving voltage
2	NC	--	No Connection
3	Vgoff_L	PO	Negative low power supply for gate driver output: -12.5V
4	C4P	C	Pins to connect capacitance for power circuitry
5	C4M	C	Pins to connect capacitance for power circuitry
6	VGH	PO	Positive power supply for gate driver output: +12.5V
7	FRP	O	Frame polarity output for VCOM
8	VCAC	C	Define the amplitude of the VCOM swing
9	Vint3	P	Intermediate voltage for charge Pump
10	C3P	C	Pins to connect capacitance for power circuitry
11	C3M	C	Pins to connect capacitance for power circuitry
12	Vint2	P	Intermediate voltage for charge Pump
13	C2P	C	Pins to connect capacitance for power circuitry
14	C2M	C	Pins to connect capacitance for power circuitry
15	Vint1	P	Intermediate voltage for charge Pump
16	C1P	C	Pins to connect capacitance for power circuitry
17	C1M	C	Pins to connect capacitance for power circuitry
18	PGND	P	Charge Pump Power GND
19	PVDD	P	Charge Pump Power VDD
20	DRV	PO	Gate signal for the power transistor of the boost converter
21	LED Anode	I	For Led Anode voltage
22	GND	P	Digital GND
23	FB	P	Main boost regulator feedback input
24	AVDD	P	Analog power supply
25	GND	P	Digital GND
26	VCC	P	Digital power supply
27	CS	I	Serial communication chip select
28	SDA	I	Serial communication data input
29	SCL	I	Serial communication clock input
30	HSYNC	I	Horizontal sync input
31	VSYNC	I	Vertical sync input
32	DCLK	I	Clock Input:
33	D7	I	Data input :MSB
34	D6	I	Data input
35	D5	I	Data input
36	D4	I	Data input
37	D3	I	Data input
38	D2	I	Data input
39	D1	I	Data input
40	D0	I	Data input: LSB

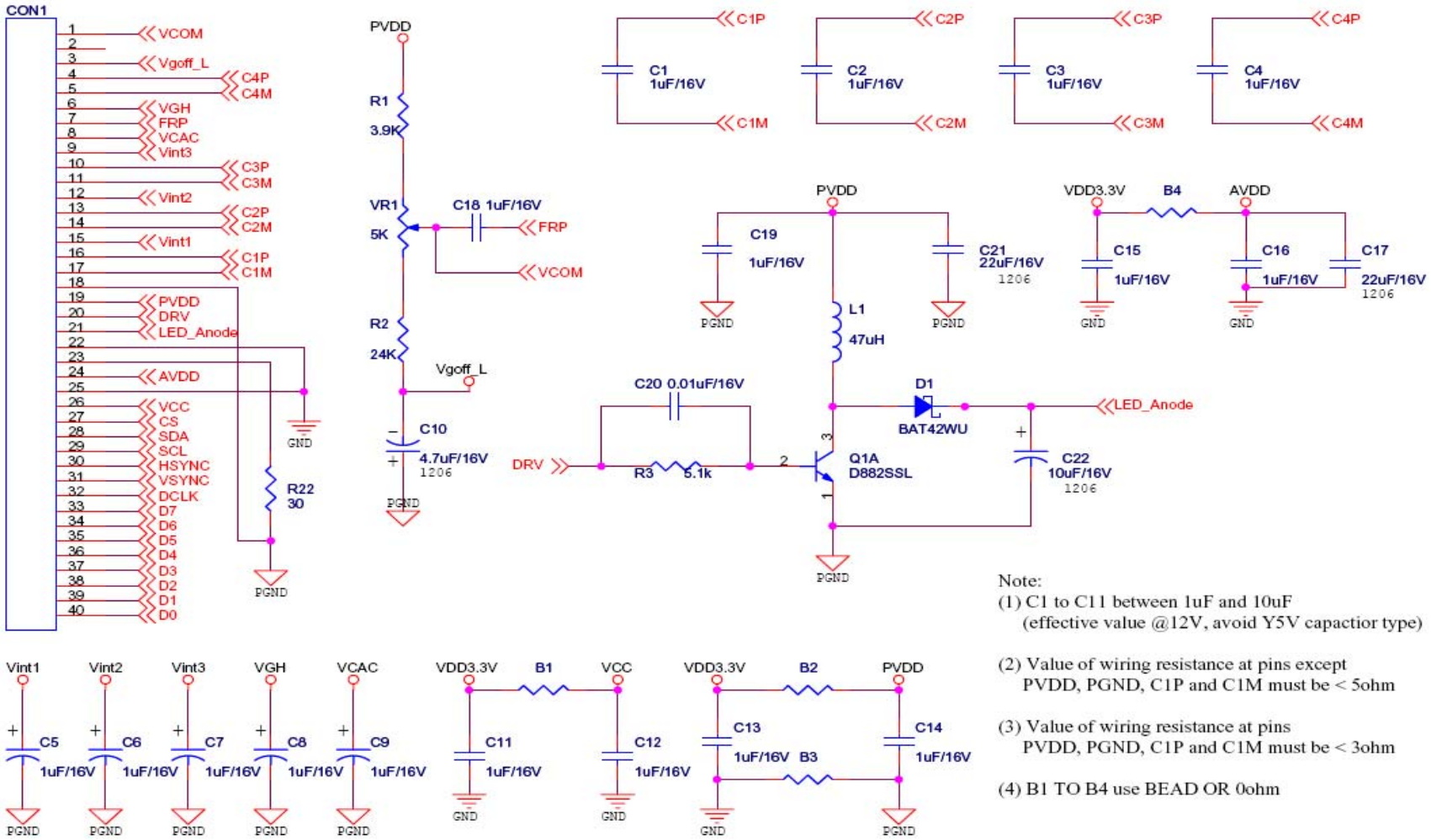
9. BLOCK DIAGRAM





9.1 Application Circuit

9.1.2 With LED Backlight Driving Circuit, FPC, Power connection and LED Backlight Driving Circuit



Note:

(1) C1 to C11 between 1uF and 10uF
(effective value @12V, avoid Y5V capactior type)

(2) Value of wiring resistance at pins except PVDD, PGND, C1P and C1M must be < 5ohm

(3) Value of wiring resistance at pins PVDD, PGND, C1P and C1M must be < 3ohm

(4) B1 TO B4 use BEAD OR 0ohm

10. QUALITY ASSURANCE

Test Condition

10.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : 20 ± 5°C
Humidity : 65 ± 5%

10.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

10.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

10.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

10.1.5 Test Method

No.	Reliability Test Item & Level	Test Level	Remark
1	High Temperature Storage Test	T=80°C,240hrs	IEC68-2-2
2	Low Temperature Storage Test	T=-30°C,240hrs	IEC68-2-1
3	High Temperature Operation Test	T=70°C,240hrs	IEC68-2-2
4	Low Temperature Operation Test	T=-20°C,240hrs	IEC68-2-1
5	High Temperature and High Humidity Operation Test	T=60°C,95% RH,240hrs	IEC68-2-3
6	Thermal Cycling Test (No operation)	-30°C → +25°C → +80°C,50 Cycles 30 min 5min 50 min	IEC68-2-14
7	Vibration Test (No operation)	Frequency:10 ~ 55 Hz Amplitude:1.0 mm Sweep Time:11min Test Period:6 Cycles for each Direction of X,Y,Z	IEC68-2-6
8	Shock Test (No operation)	100G, 6ms Direction：± X,± Y,± Z Cycle：3 times	IEC68-2-27
9	Electrostatic Discharge Test (No operation)	150pF,330Ω Air:± 15KV;Contact: ± 8KV 10 times/point;4 points/panel face	IEC-61000-4-2

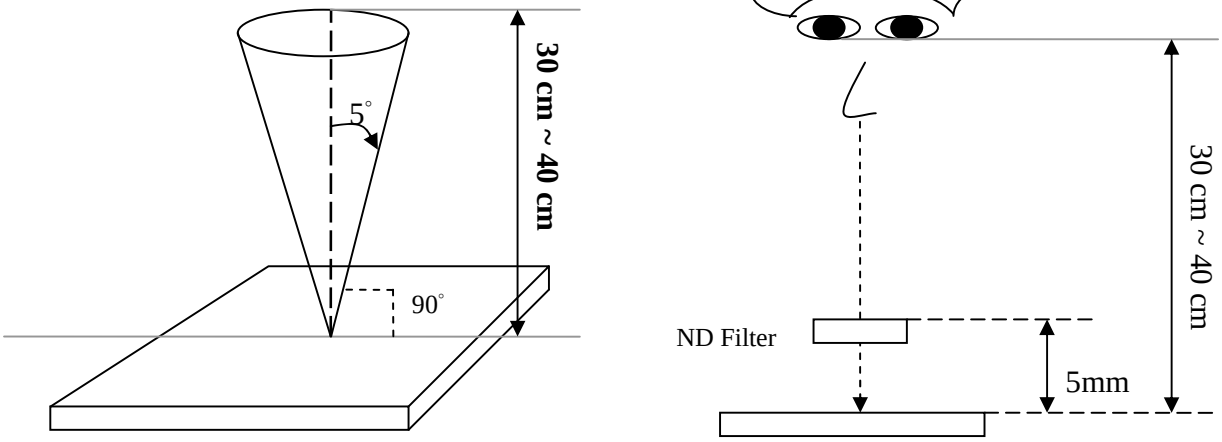
11. APPEARANCE SPECIFICATION

11.1 Inspection condition

11.1.1 Inspection conditions

11.1.1.1 Inspection Distance : 35 ± 5 cm

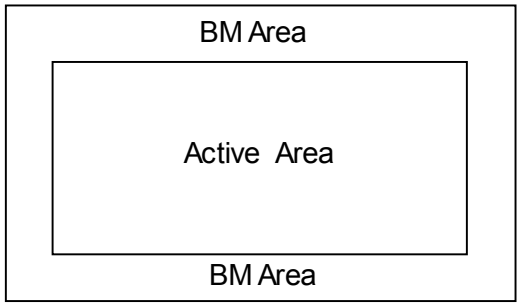
11.1.1.2 View Angle : Inspection under test condition : ±5°



11.1.2 Environment conditions :

Ambient Temperature :		**25±5℃**
Ambient Humidity :		**65±5%**
Ambient Illumination	Functional Inspection	**300~ 500 lux**

11.1.3 Definition of applicable Zones



11.1.3 Inspection Parameters

<table>
<tr><th>No.</th><th>Parameter</th><th>Criteria</th></tr>
<tr><td rowspan="6">1</td><td rowspan="6">Operating</td><td>Display function: No Display malfunction (Major)</td></tr>
<tr><td>Line Defect: No obvious Vertical and Horizontal line defect in bright, dark and colored. (Major) (Note:1)</td></tr>
<tr><td>Point Defect (Red, green, blue, dark): Active area ≤4dots (Minor)(Note:1)
<table>
<tr><th>Item</th><th>Acceptable number</th><th>Total</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>Bright</td><td>2</td><td rowspan="2">4</td><td rowspan="4">Minor</td><td rowspan="4">1.5</td></tr>
<tr><td>Dark</td><td>3</td></tr>
<tr><td>Adjacent Bright</td><td>1</td><td>1</td></tr>
<tr><td>Adjacent Dark</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>Non-uniformity:
Visible through 2%ND filter white, R, G, B and gray 50%pattern. (Minor)</td></tr>
<tr><td>Foreign material in Black or White spots shape (W>1/4L) (Note: 5)
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>D ≤ 0.3</td><td>*</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>0.3 < D ≤0.5</td><td>3</td></tr>
<tr><td>D> 0.5</td><td>0</td></tr>
</table>
D = (Long + Short) / 2 ＊: Disregard</td></tr>
<tr><td>Foreign Material in Line or spiral shape (W≤1/4L) (Note: 4)
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>W>0.1mm,L>5mm</td><td>0</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>L≦5mm,0.05mm<W≦0.1mm</td><td>3</td></tr>
<tr><td>L≦5mm,W<0.05mm</td><td>*</td></tr>
</table>
L : Length W : Width ＊: Disregard</td></tr>
<tr><td rowspan="3">2</td><td rowspan="3">External Inspection (non-operating)</td><td>Dimension: Outline (Major)</td></tr>
<tr><td>Bezel appearance: uneven (Minor)</td></tr>
<tr><td>Scratch on the polarize: (Note:2)
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>W>0.1mm,L>5mm</td><td>0</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>L≦5mm,0.05mm<W≦0.1mm</td><td>3</td></tr>
<tr><td>L≦5mm,W<0.05mm</td><td>*</td></tr>
</table>
L : Length W : Width ＊: Disregard
Dent and spots shape on the polarize (Note:2): (Note: 5)
<table>
<tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr>
<tr><td>D ≤ 0.3</td><td>*</td><td rowspan="3">Minor</td><td rowspan="3">1.5</td></tr>
<tr><td>0.3 < D ≤0.5</td><td>3</td></tr>
<tr><td>D> 0.5</td><td>0</td></tr>
</table>
D = (Long + Short) / 2 ＊: Disregard</td></tr>
<tr><td></td><td></td><td>Polarizer flaw or leak out resin : Defect is defined as the active area.</td></tr>
</table>

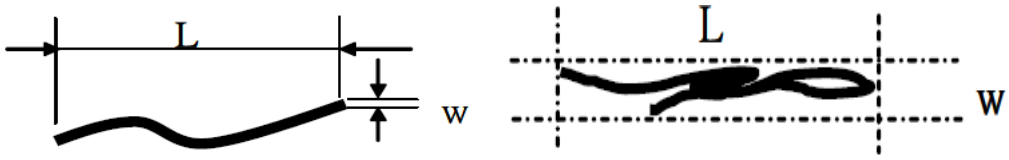
Class of defects	**Major**	AQL 0.65%	**Definition** It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.
	Minor	AQL 1.5%	It is a defect that will not result in functioning problem with deviation classified.

Note:1.(a)Bright point defect is defined as point defect of R,G,B with area >1/2 dot respectively
(b)Dark point defect is defined as visible in full white pattern.
(c)Definition of distribution of point defect is as follows:
-minumum separation between dark point defects should be larger than 5mm.
-minumum separation between bright point defects should be larger than 5mm.
(d)Definition of joined bright point defect and joined dark point defect are as follows:
-Two or more joined bright point defects must be nil.
-Three joined dark point defects must be nil.
-Coupling of one dark and one bright point in junction is counted as one dark and bright spot with 1 pair maxmum.

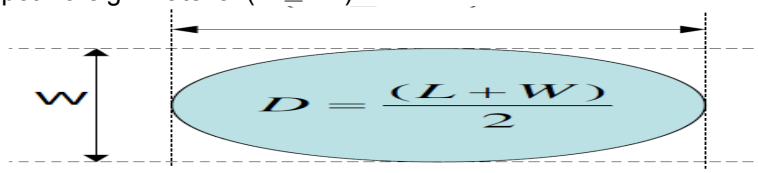
Note:2 The external inspection should be conducted at the distance 35± 5cm between the eyes of inspctor and the panel .

Note:3 Luminance measurement for contrast ratio is at the distance 50± 5cm between the detective head and the panel with ambient illuminance less than 1 lux. Contrast ratio is obtained at optimum view angle.

Note:4 W-Width in mm , L-length of Max.(L1,L2) in mm.



Note:5 Spot Foreign Material (W≧L/4)

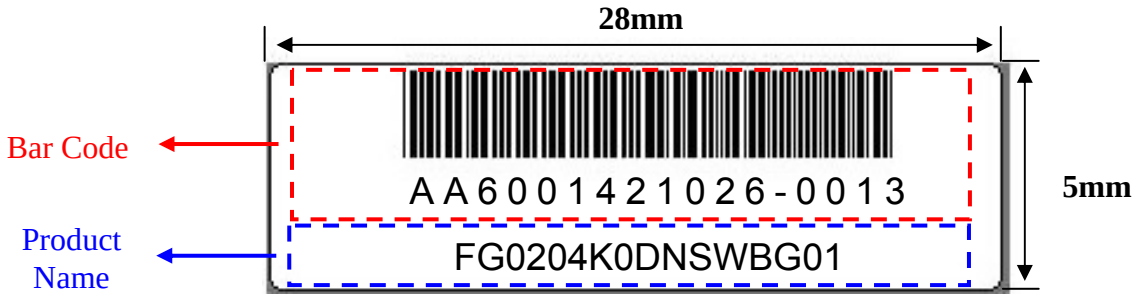


11.2 Sampling Condition

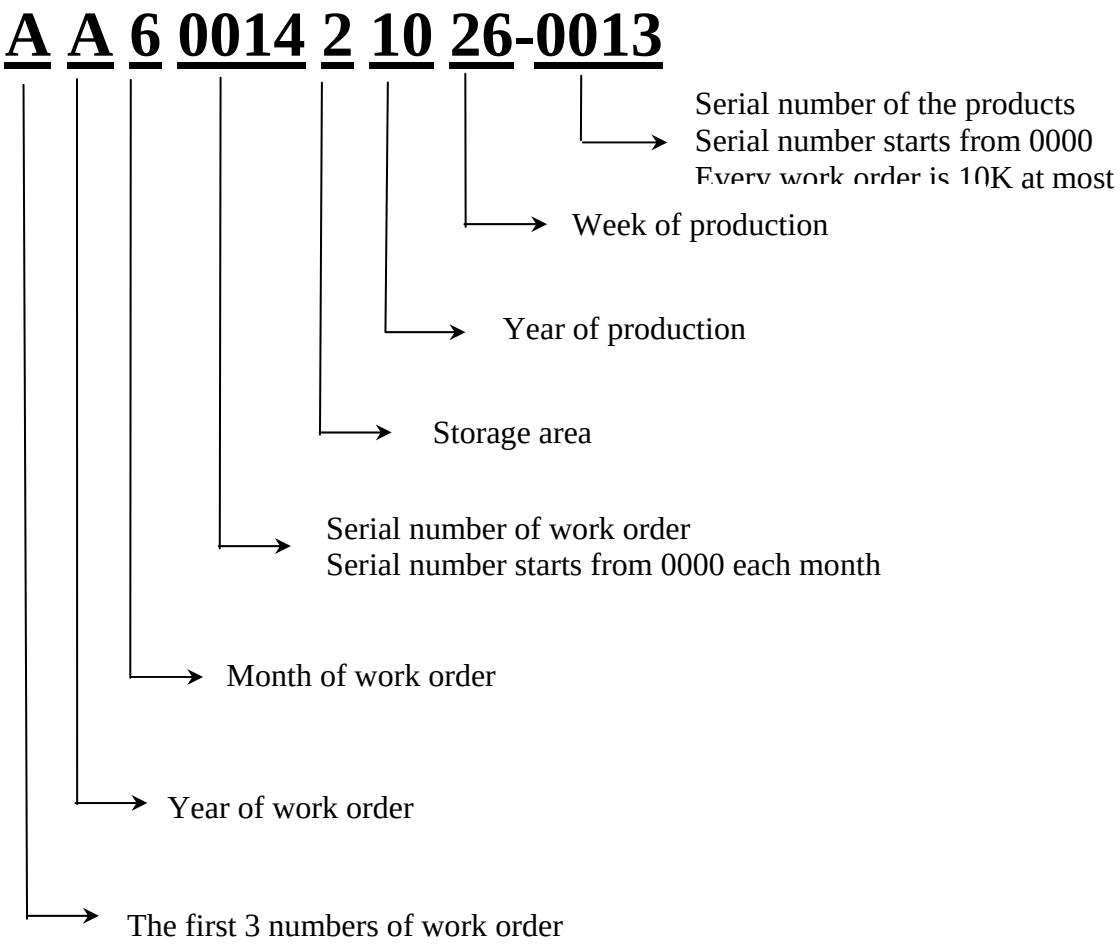
Unless otherwise agree in written, the sampling inspection shall be applied to the incoming inspection of customer.
Lot size: Quantity of shipment lot per model.
Sampling type: normal inspection, single sampling
Sampling table: MIL-STD-105E
Inspection level: Level II

12. LCM PRODUCT LABEL DEFINE

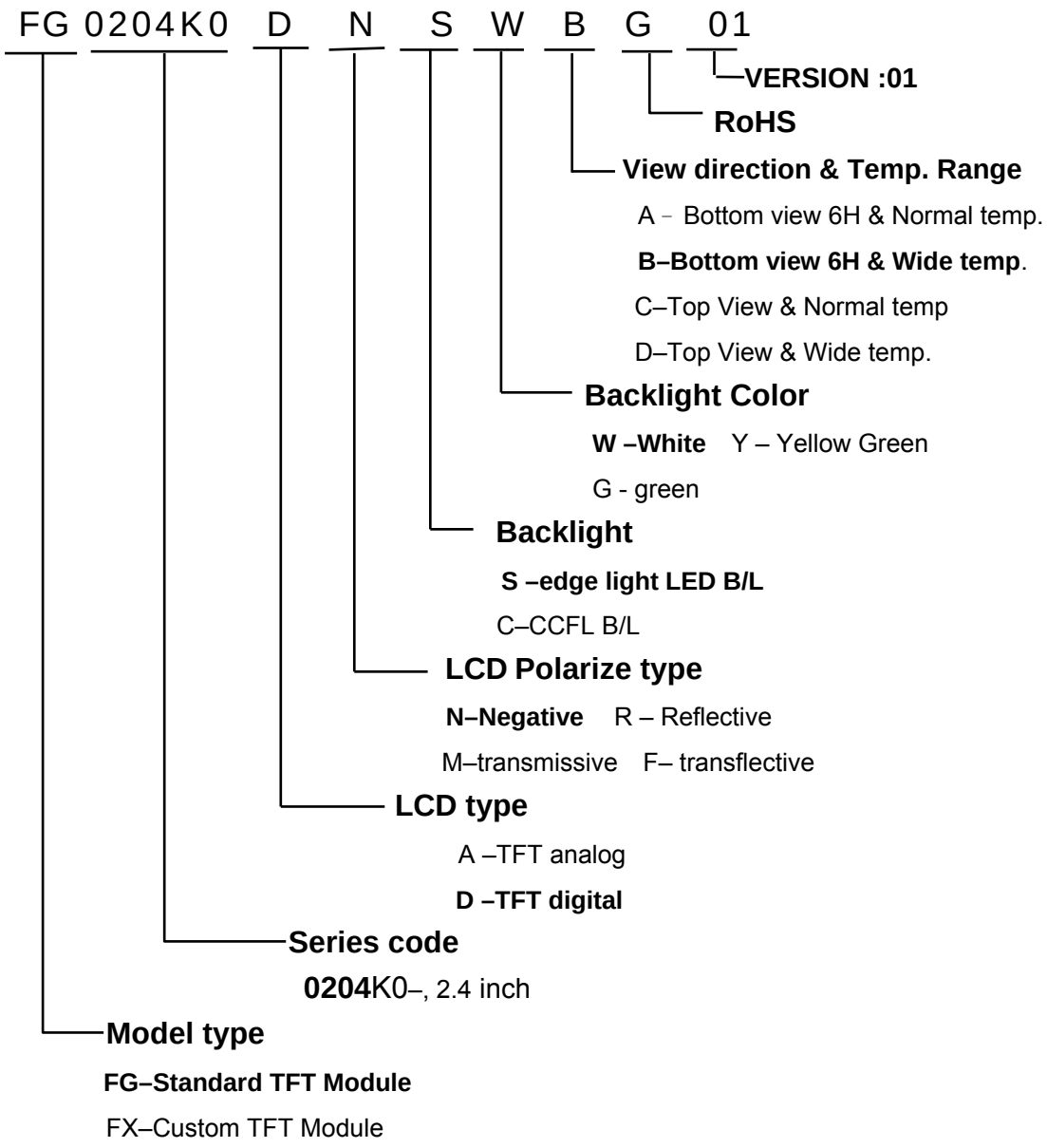
Product Label style:



BarCode Define:



Product Name Define:

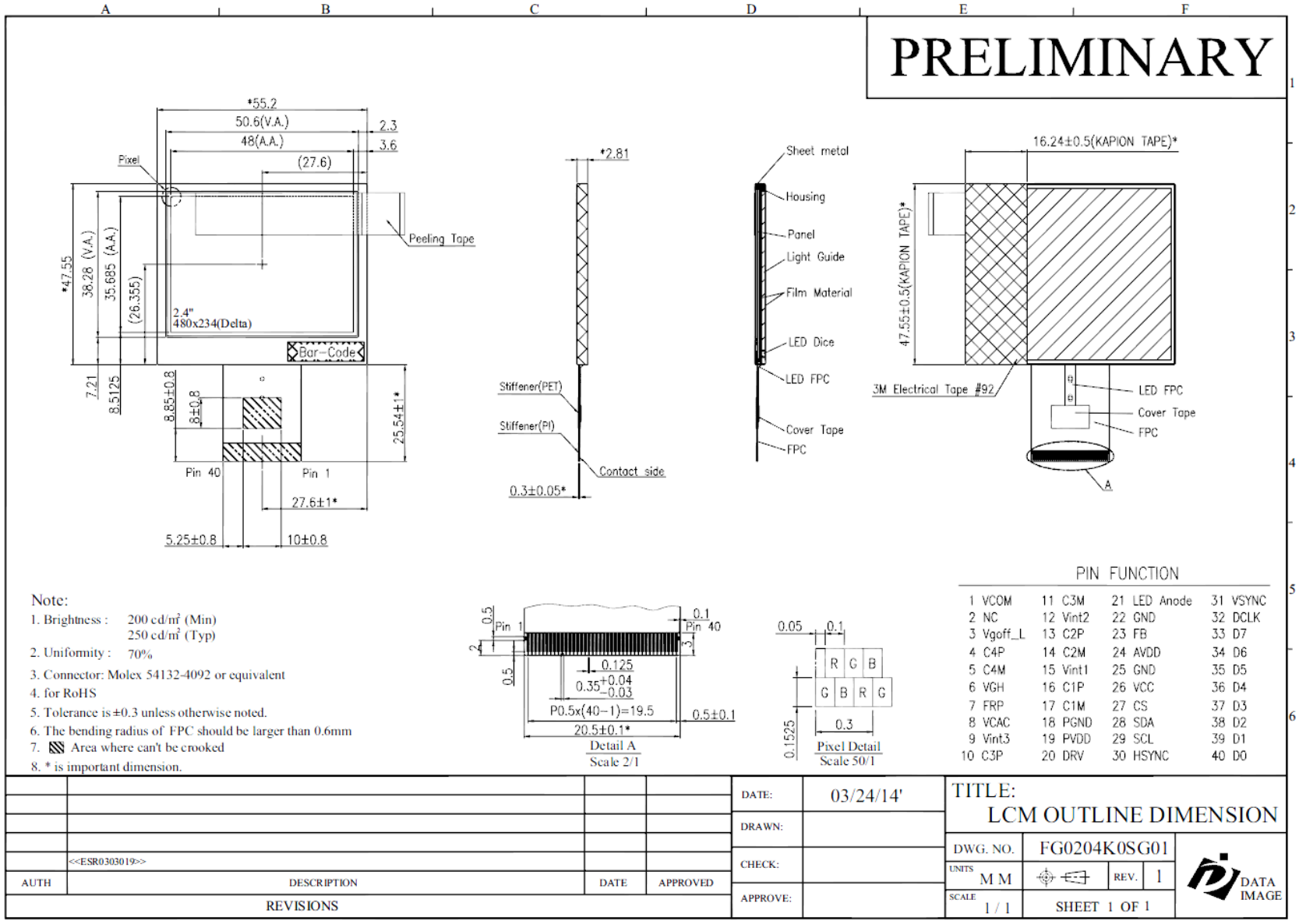


13. PRECAUTION FOR USING LCM

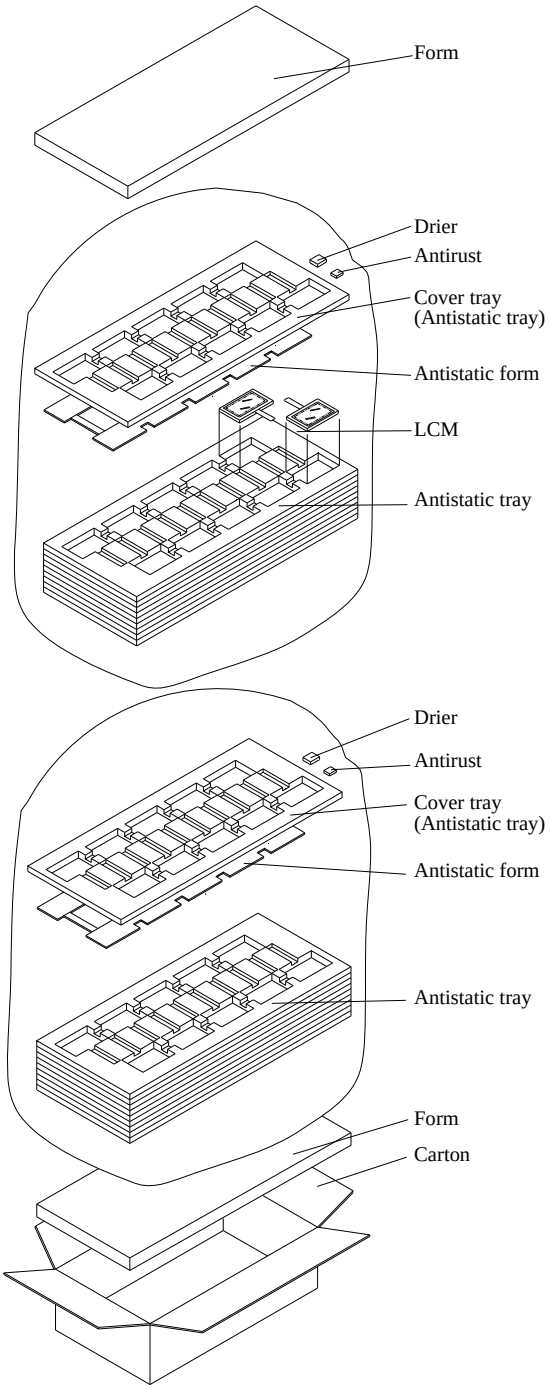
1. ASSEMBLY PRECAUTIONS
   (1) You must mount a module using holes arranged in four corners or four sides.
   (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
   (3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
   (4) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
   (5) Do not open the case because inside circuits do not have sufficient strength.
   (6) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
   (7) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
   (8) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.
2. OPERATING PRECAUTIONS
   (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
   (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification
   (3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
   (4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
   (5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
   (6) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
3. ELECTROSTATIC DISCHARGE CONTROL
   (1) The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such the copper leads on the PCB and the interface terminals with any parts of the human body.
   (2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
   (3) Only properly grounded soldering irons should be used.
   (4) If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.
   (5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended
   (6) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.
4. STORAGE PRECAUTIONS
   (1) When you store LCDs for a long time, it is recommended to keep the temperature between 0°C-40°C without the exposure of sunlight and to keep the humidity less than 90%RH.
   (2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C 90%RH
   (3) Please do not leave the LCDs in the environment of low temperature; below -20°C.
5. OTHERS
   (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays
   (2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
   (3) For the packaging box, please pay attention to the followings:
      a. Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
      b. Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
      c. Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)
6. LIMITED WARRANTY

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events.

14. OUTLINE DRAWING



15. PACKAGE INFORMATION



Material

1 Carton + 2 Anti-static bag + 2 Form(35mm) + 20Anti-static tray + 2 Drier + 2 Antirust

Total pcs

1 Antistatic tray =10panel pcs

1 Anti-static bag = 9 Anti-static tray + cover tray =9*10 +1 = 90pcs

1 Carton = 2 Anti-static bag = 2*90 = 180pcs

1 Carton = 180 pcs

Carton size : 465L x 380W x 395H (mm)

Total Weight ≒5kgw